CSE Computer Science

Logic Circuits

Score Board

EXPLORING THE CONCEPT, DESIGN, AND IMPLEMENTATION

Core Objectives

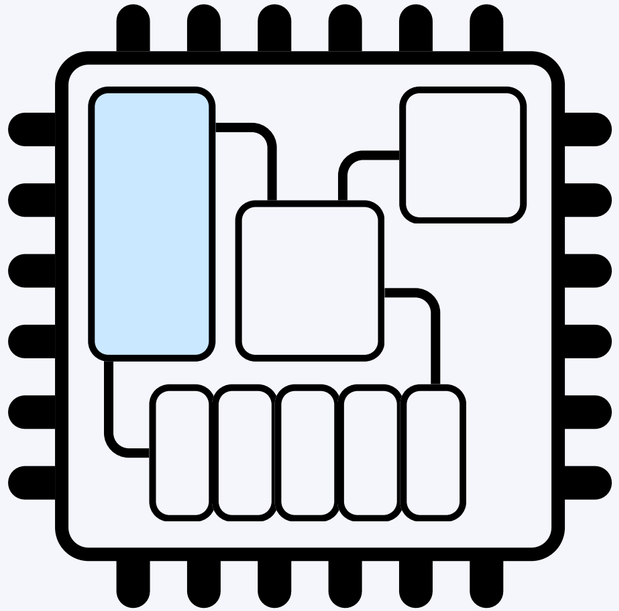
To Create an Interactive Scoreboard: The primary aim is to develop a digital scoreboard that can seamlessly add or subtract points based on game events.

To Leverage Flip-Flop Technology: Utilizing JK Flip-Flops allows for effective state management in binary counting, which is ideal for this application.

To Provide a Visual Display of Scores: The project will incorporate a Seven-Segment Display to visually represent the scores, making it user-friendly and easy to read.

Overview of the 74HC191

- Features of 74HC191:
  - Synchronous 4-bit Up/Down Counter
  - Supports both Up and Down counting modes
  - Uses JK Flip-Flops for state transitions
  - Binary counting with external control for counting direction.



Why Use JK Flip-Flops Instead of T or D Flip-Flops in Counters

1. **Full Toggle Capability**
   - **JK Flip-Flops** can toggle between states (0 and 1) effectively with both J and K inputs.
   - **T Flip-Flops** only toggle when T=1, which limits flexibility in more complex counting applications.

2. **Control Over Output**
   - **JK Flip-Flops** allow for both setting and resetting (J=1, K=0 for set; J=0, K=1 for reset), providing more control over output states.
   - **D Flip-Flops**, on the other hand, simply pass the input state to output, limiting their utility in counters.

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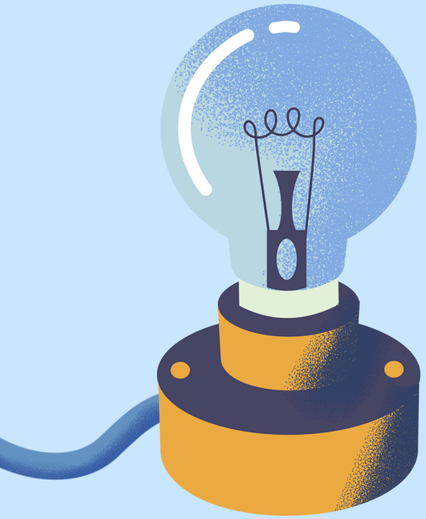
3. **Asynchronous Reset Functionality**
   - **JK Flip-Flops** typically include asynchronous preset and clear inputs, facilitating immediate state changes without clock pulses.
   - While D Flip-Flops can have similar features, T Flip-Flops generally do not, making JK Flip-Flops more versatile in counter designs.

4. **Extended Functions**
   - **JK Flip-Flops** allow for more complex configurations, enabling features like up/down counting via logic inputs.
   - T Flip-Flops primarily offer a simple toggle functionality, and D Flip-Flops focus solely on data storage.

How Does It work



Step 1: Counting Mechanism	Operation: Composed of flip-flops that count clock pulses applied to their CK input. Each flip-flop toggles based on the previous one, resulting in a binary output that represents the count. Up and Down Counting: Modifying connections allows the counter to count up or down. However, asynchronous counters can be unreliable at high speeds due to clock ripple effects, where delays in signal propagation cause incorrect output states.
Step 2: Control Features	Both types of counters can include control features such as enable/disable inputs, presetting, and clearing. For example, in synchronous counters, the Count Enable (CTEN) input can halt counting while retaining the current state. Additionally, preset inputs allow loading a specific binary value into the counter, enabling flexible operation for various applications.
Steps 3 : Output Representation	The outputs of the counters represent the current count in binary form. For a 4-bit counter, the outputs Q0,Q1,Q2,Q3*Q*0,*Q*1,*Q*2,*Q*3 correspond to binary values from 00000000 (0) to 11111111 (15). In BCD counters, specific logic gates are used to reset the count after reaching 9, allowing the counter to cycle through decimal values effectively. These steps highlight the fundamental operation of digital counters, showcasing their counting mechanism, control features, and output representation.

CK	Q3	Q2	Q1	Q0	Next State (Q3,Q2,Q1,Q0)
0	0	0	0	0	1111
1	0	0	0	1	1110
2	0	0	1	0	1101
3	0	0	1	1	1100
4	0	1	0	0	1011
5	0	1	0	1	1010
6	0	1	1	0	1001
7	0	1	1	1	1000

CK	**Q3**	**Q2**	Q1	Q0	Next State (Q3,Q2,Q1,Q0)
8	1	0	0	0	0111
9	1	0	0	1	0110
10	1	0	1	0	0101
11	1	0	1	1	0100
12	1	1	0	0	0011
13	1	1	0	1	0010
14	1	1	1	0	0001
15	1	1	1	1	0000

Karnaugh Map for J and K Inputs

For J3

For K3

Q3Q2\Q1Q0	00	01	11	10
00	1	1	0	0
01	1	0	0	1
11	0	1	1	0
10	0	0	1	1

Functions:

JK Flip-Flop Functions:

The JK flip-flop has two inputs, J and K, which control the state changes based on the current state of the flip-flop and the clock input :

- J = 1, K = 0: Set the output to 1 (toggle to high).
- J = 0, K = 1: Reset the output to 0 (toggle to low).
- J = 1, K = 1: Toggle the output (change state).
- J = 0, K = 0: No change in output.
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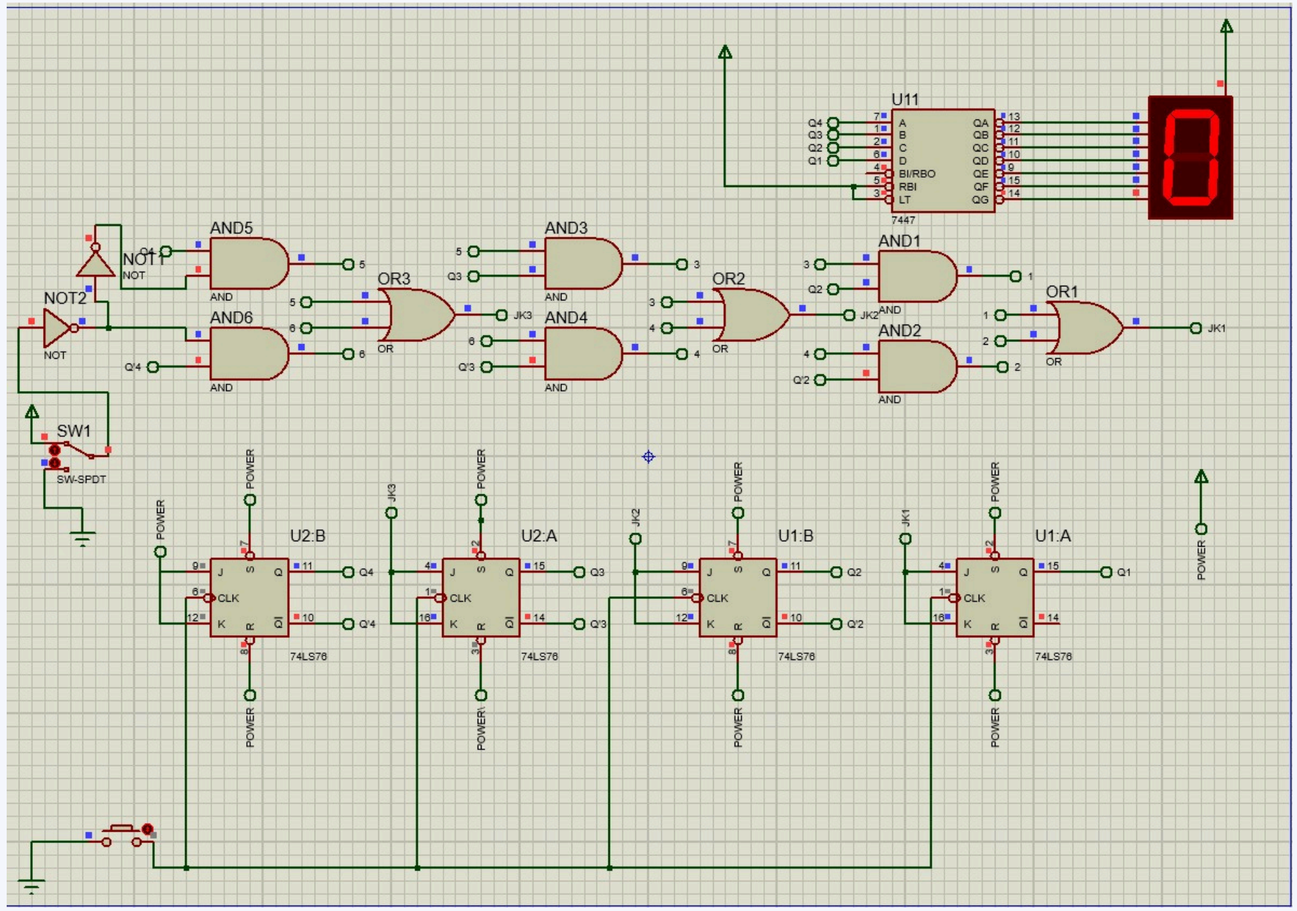
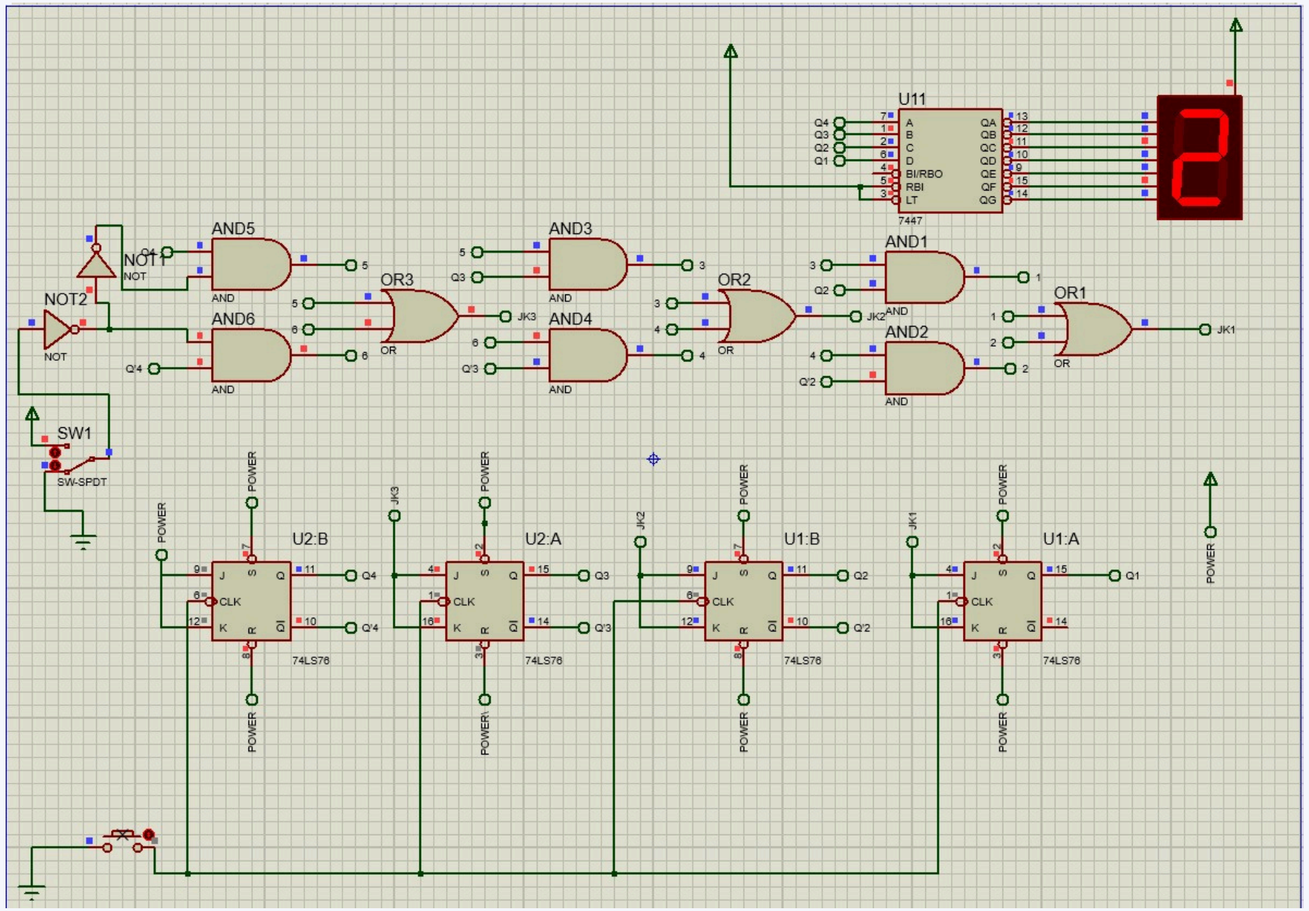
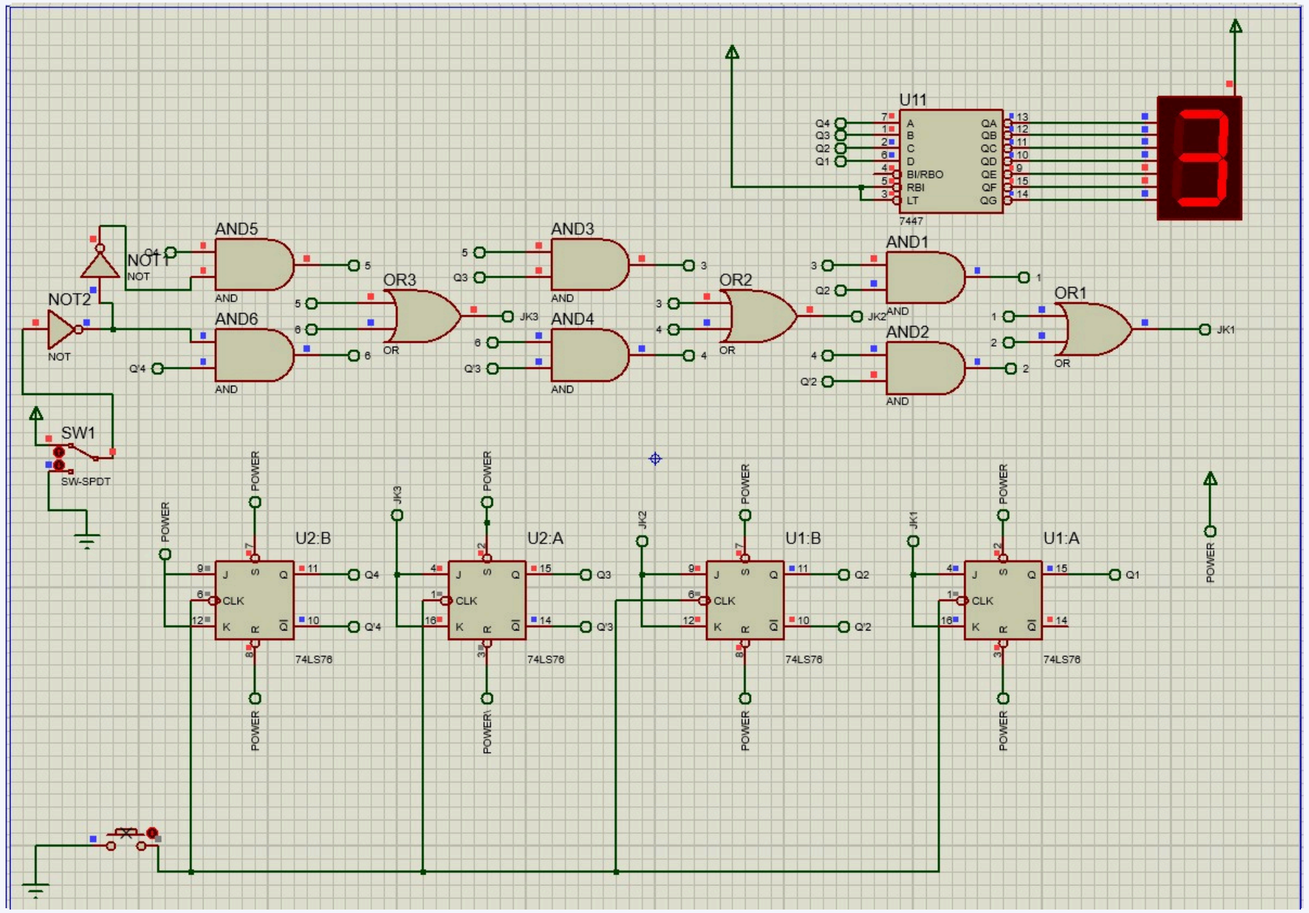
Simulation:


U11
7447
NOT1
NOT2
SW1
SW-SPDT
AND5
AND6
AND3
AND4
AND1
AND2
OR3
OR2
OR1
JK3
JK2
JK1
U2:B
U2:A
U1:B
U1:A
74LS76
POWER

Simulation:


U11
7447
AND5
AND6
AND3
AND4
AND1
AND2
OR3
OR2
OR1
NOT1
NOT2
SW1
SW-SPDT
U2:B
U2:A
U1:B
U1:A
74LS76
POWER
JK3
JK2
JK1

Simulation:


U11
7447
Q4
Q3
Q2
Q1
A
B
C
D
BI/RBO
RBI
LT
QA
QB
QC
QD
QE
QF
QG
NOT1
NOT2
NOT
AND5
AND6
AND3
AND4
AND1
AND2
AND
OR3
OR2
OR1
OR
JK3
JK2
JK1
Q'4
Q'3
Q'2
SW1
SW-SPDT
POWER
U2:B
U2:A
U1:B
U1:A
74LS76
J
S
Q
CLK
K
R
Q'

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