Lab 3: Combinational Logic Circuit

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Purpose

The purpose of this lab session is to make a functional logic circuit by using a breadboard, jumper wires and never-before used electronic equipment such as a 4-bit counter and logic gates. The purpose of this experiment could be interpreted as expanding on our practical and theoretical knowledge of building electrical circuits that we started gaining in lab 1.

Design Specifications

This experiment requires the designing and building of a basic logic circuit with a recommendation of using at least 2 types of gates. With this objective in mind, I will be implementing a 4-input 1-output setup that utilizes 2 “AND” gates and one “OR” gate. Inputs will be hooked up to the 4-bit counter and the output will be displayed through either an oscilloscope or an LED. The inputs will also have the ability to be connected to a LED. These LEDs will be in contact with a resistor to prevent damage to circuit components. As for the physical components, a single quad 2-input AND gate (74LS/HC08) will be used for the two specified AND gates and a single Quad 2-input OR gate(74LS/HC32) will be used for the single or gate. The AND gate will receive four sequential inputs from a 4-bit counter(74HC/HTC163), the two outputs will be the inputs of the OR gate. Green LEDs will be used to represent the inputs and a signal red LED will represent the output of the OR gate. The circuit will run on 5 Volts and resistors of 1KOhm will be used with LEDs when necessary to prevent the circuit from suffering damage.

out_1 <= (in1 AND in2) OR (in3 AND in4)

(see Figure 1 in Appendices for visual representation)

Truth Table (Theoretical) :

in_1	in_2	in_3	in_4	in_1 AND in_2	in_3 AND in_4	out_1
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	1	1
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	1	1
1	1	0	0	1	0	1
1	1	0	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	1	1	1

Table 1: Theoretical truth table for the circuit

Methodology

While this lab consists of a singular objective and TA check, the process can be divided into sequential steps for ease of implementation. These are as follows:

Step 1: Install the 4-bit counter on the breadboard and connect the corresponding pins to positive/ground via jumper wires. Connect the circuit to the function generator and the DC power supply. Check if the signal outputs are given sequentially with green LEDs and resistors.

Step 2: Install the AND gate and connect the 4 output pins of the counter to the AND gate.

Step 3: Connect the two output pins of the AND gate to the OR gate. Install the red LED to the output pin of the OR gate to see if it works. Compare the signal outputs with the theoretical data from the truth table.

Step 4: Hook the circuit up to the oscilloscope via the probe and observe the signals.

Steps 3 and 4 require a check from the TA.

Results

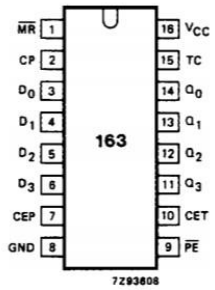

Figure 2.1: Pin layout of the counter

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L (1)
count	h	↑	h	h	h	X	count	(1)
hold (do nothing)	h h	X X	l X	X l	h h	X X	q_n q_n	(1) L

Figure 2.3: Function table

The first step of the objective was to successfully install the 4-bit signal counter to the breadboard and connect the corresponding pins to the positive/ground strips found on the side of the breadboard. To accomplish this task, the 74HC/HCT163 data sheet was utilized to connect each pin to its required position. After the pin was installed on the breadboard, the pin configuration diagram in the data sheet(Figure 2.1) was checked with respect to what the symbols meant on the description table(Figure 2.2) found above the diagram. With these two tables in mind, I moved on to connecting the jumper wires. Since I wanted to run the 4-bit signal counter in the “clock” operating mode, I utilized the given function table(figure 2.3) to connect the corresponding pins to their receiving ends. These are as follows: Pin 1(MR) > HIGH, Pin 2(CP) > Clock input, Pin 3-to-6 (Dn’s) > LOW (don’t care), Pin 7(CEP) > HIGH, Pin 8(Ground) > Ground, Pin 9(PE) > HIGH, Pin 10(CET) > HIGH, Pin 11-to-14(Qn’s) > Outputs, Pin 15(TC) > LOW, Pin 16(Vcc) > Positive Supply Voltage. Pins labeled as HIGH were connected to the positive strip of the breadboard and ones labeled as Ground and LOW were connected to the ground strip and the CP pin was connected to the positive end of the function generator. In order to test if the signal counter was working as intended, four green LEDs were hooked up sequentially to each output pin with a 1KOhm resistor to prevent potential damage. Long positive arms of the LED were connected to the resistors and their short arms were grounded. Pins were connected from the most to least significant figure in the following sequence: Q3-Q2-Q1-Q0. Once these were set up, the DC power supply was connected to the positive and ground strips of the breadboard and a 5V pk-pk 1Hz square wave was generated by the function generator. It was observed that the 4-bit counter was counting sequentially from 0 to 15 in binary, which meant everything was working as intended (Figures 3.1 to 3.3). If desired, the counting rate can be increased by increasing the frequency of the function generator. The voltage was shut off before further work on the circuit commenced.

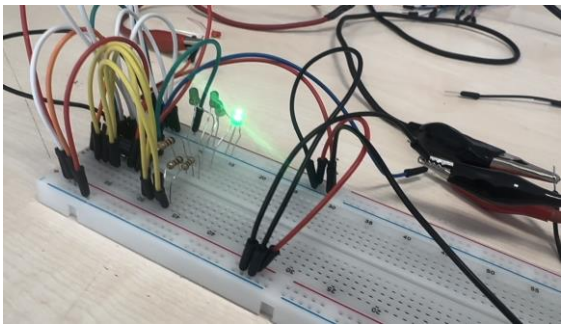

Figure 3.1: Signal 1 "0001"

For the second step of this lab session, the AND gate was connected to the breadboard. In order to connect Q3 through Q0, an online diagram of that specific type of AND gate was utilized(Figure 4). Vcc was connected to the positive strip and the GND was connected to the ground via jumper wires. As for the signal outputs from the 4-bit counter: Q3 was connected to pin A3, Q2 was connected to B3, Q1 was connected to B1 and Q0 was connected to A1. Corresponding outputs for Q3-Q2 and Q1-Q0 were Y3 and Y1 respectively.

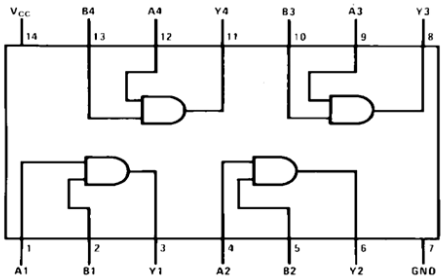

Figure 4: 74LS/HC08 diagram [1]

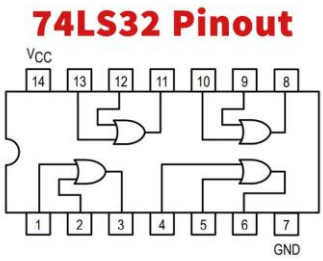

Figure 5: 74LS/HC32 diagram [2]

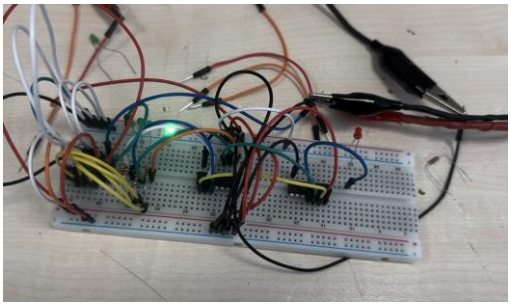

Figure 6.1: in "0001", out "0"

For the third step of this experiment, an OR gate was placed on the breadboard and another online diagram(Figure 5) was utilized to connect the jumper wires to their respective pins. Vcc was connected to the positive strip and GND was connected to the ground via jumper wires. By using more jumper wires, pin Y3 of the AND gate was connected to B4 (Pin 13) and Y1 to A4 (Pin 12) [2]. The output from C4 (Pin 11) was connected to a red LED from its long positive arm and its short negative arm was grounded. A resistor for this specific LED was omitted because, with a resistor, the LED would get too dim for the camera. Possible reasons for this phenomenon will be discussed in the conclusion. Once the red LED became operational, the Voltage was increased back to 5V at 1Hz, and sequential outputs were observed (Figure 6.1 to 6.3). Observed outputs were recorded in a notebook in the form of a truth table (Figure 7).

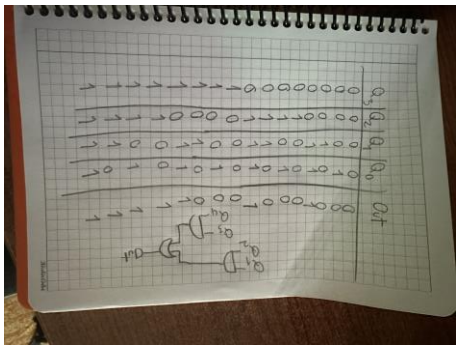

Figure 7: Observed Truth Table

This truth table matches the theoretical one we made in the “Design Specifications” section (Table 1). This means that the circuit is functioning as intended without any observable logical errors.

For the fourth step of the experiment, the circuit was hooked up to an oscilloscope. The ground clip of the oscilloscope probe was attached to the ground strip of the breadboard and the hook was connected to the positive leg of the red output LED. On the oscilloscope screen (Figure 8), the outputs of the LED were observable and match the truth table from the previous step (Figure 7). The peaks indicate when LED had current running through it which means it was turned on and was indicating a binary output of “1”. The system was running at 5V with a frequency of 1 Hz, which means the binary input values were increasing by “+1” at the end of each second.

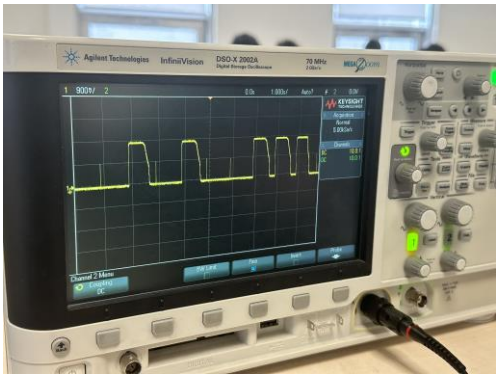

Figure 8: Oscilloscope Screen

Conclusion

This lab was conducted with the objective of designing a logic circuit by using a breadboard and physical electronic components such as logic gates and a 4-bit counter. Throughout the experiment, I planned a logic circuit in the design specifications section, implemented it in multiple sequential steps and observed how it functioned by writing down both theoretical and observed truth tables and comparing them. These two tables match each other which means the designed logic circuit functions as intended. These tables were confirmed by an oscilloscope also. Considering the defined purpose of this experiment was accomplished, this experiment can be considered successful. There was not any significant observable error throughout the experiment outside of the lack of need for a resistor for the red output LED. This could potentially be due to one of the jumper wires being loose, a damaged component having increased the resistance due to prolonged use alongside the possibility of the resistance from the two logic gates being a factor. Throughout the lab, I did not experience any issues related to circuit burnouts or damaged components. However, one thing I struggled with was the abundance of jumper wires used in the circuit. Due to overlapping wires restricting access to the other wires, it was sometimes challenging to keep working on the circuit due to the risk of tampering with an overlapping wire. This potential liability could be resolved by using a tool of some kind to plug wires in and out of narrow gaps, maybe something similar to a tweezer.

Appendices

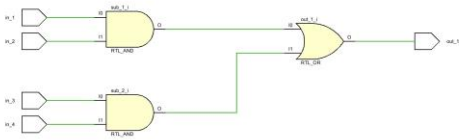

Figure 1: A logic gate diagram of the circuit made with Vivado

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

Figure 2.2: Pin description table

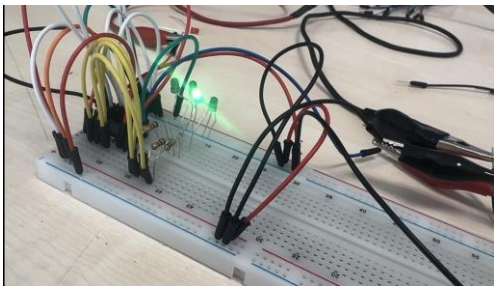

Figure 3.2: Signal 2 "0010"

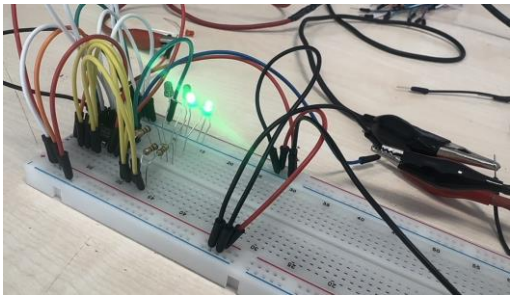

Figure 3.3: Signal 3 "0011"

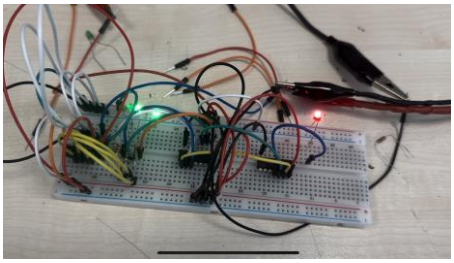

Figure 6.2: in "0011", out "1"

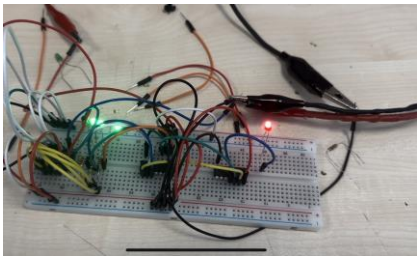

Figure 6.3: in "0111", out "1"

References

1) "74LS08 – Quadruple Two Input and Gate." Components101, components101.com/ics/74ls08-and-gate-ic-pinout-datasheet. Accessed 29 Feb. 2024.

2) Joseph, David. "74LS32 Quad 2-Input or Gate." Datasheet Hub, 17 June 2022, www.datasheethub.com/74ls32-quad-2-input-or-gate/.