Hacettepe University Computer Science Department

BBM233 – Verilog Assignment 1 (Section 3)

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Here are my source files and waveform obtained from the simulation.

1 – lab1.v

```
1  `timescale 1ns / 1ps
2
3  module lab1(F, A, B, C);
4     output F;
5     input A,B,C;
6     wire and_wire, or_wire;
7
8     and a1(and_wire, A, B);
9     or o1(or_wire, and_wire, B);
10    or o2(F, or_wire, C);
11
12 endmodule
13
```

lab1.v* | lab1_testbench.v*

2- lab1_testbench.v

```
1  `timescale 1ns / 1ps
2  module lab1_testbench;
3     reg A,B,C;
4     wire F;
5
6     lab1 uut (
7        .A(A),
8        .B(B),
9        .C(C),
10       .F(F)
11    );
12    initial begin
13       assign A = 0;
14       assign B = 0;
15       assign C = 0; #100;
16       assign C = 1; #100;
17       assign B = 1;
18       assign C = 0; #100;
19       assign C = 1; #100;
20       assign A = 1;
21       assign C = 0;
22       assign C = 0; #100;
23       assign C = 1; #100;
24       assign B = 1;
25       assign C = 0; #100;
26       assign C = 1; #100;
27       $finish;
28    end
29 endmodule
```

3- Waveform of the simulator for 8 different inputs.