Hacettepe University Computer Science Department

BBM 233 - Logic Design Lab.

Verilog Experiment 3 - Report

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Subject: Implementing a bcd to segment 7 in verilog.

Here are my verilog files and the output as a waveform:

bcd2segment7.v

```
`timescale 1ns / 1ps
module getA(input A, input B, input C, input D, output a);
      assign a = ( B & ~D) | ~(A | B | C | ~D);
endmodule

module getB(input A, input B, input C, input D, output b);
      assign b = (B & ~C & D) | (B & C & ~D);
endmodule

module getC(input A, input B, input C, input D, output c);
      assign c = (~B & C & ~D);
endmodule
```

```
module getD(input A, input B, input C, input D, output d);
     assign d = (~B & ~C & D) | (B & ~C & ~D) | (B & C & D);
endmodule

module getE(input A, input B, input C, input D, output e);
     assign e = D |(B & ~C);
endmodule

module getF(input A, input B, input C, input D, output f);
     assign f = (~B & C) | (C & D) | (~A & ~B & D);
endmodule

module getG(input A, input B, input C, input D, output g);
     assign g = (~A & ~B & ~C) | (B & C & D);
endmodule


module bin2segment7(
    input A,
    input B,
    input C,
    input D,
    output a,
    output b,
    output c,
    output d,
    output e,
```

```
    output f,
    output g
    );

       getA f1(A, B, C, D, a);
       getB f2(A, B, C, D, b);
       getC f3(A, B, C, D, c);
       getD f4(A, B, C, D, d);
       getE f5(A, B, C, D, e);
       getF f6(A, B, C, D, f);
       getG f7(A, B, C, D, g);
endmodule
```

testbench.v

```
`timescale 1ns / 1ps
module testbench;

      // Inputs
      reg A;
      reg B;
      reg C;
      reg D;

      // Outputs
      wire a;
      wire b;
      wire c;
```

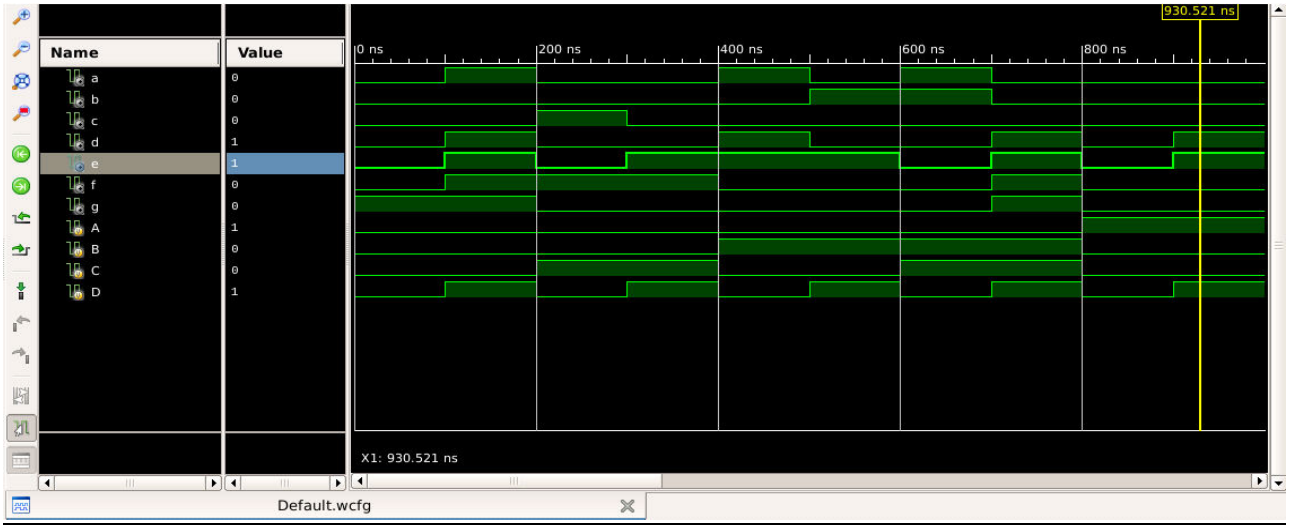
```
wire d;
wire e;
wire f;
wire g;

// Instantiate the Unit Under Test (UUT)
bin2segment7 uut (
	.A(A),
	.B(B),
	.C(C),
	.D(D),
	.a(a),
	.b(b),
	.c(c),
	.d(d),
	.e(e),
	.f(f),
	.g(g)
);

initial begin
	// Initialize Inputs
	A = 0; B = 0;C = 0;D = 0;
	#100;
	A = 0; B = 0;C = 0;D = 1;
	#100;
	A = 0; B = 0;C = 1;D = 0;
```

```
        #100;
        A = 0; B = 0;C = 1;D = 1;
        #100;
        A = 0; B = 1;C = 0;D = 0;
        #100;
        A = 0; B = 1;C = 0;D = 1;
        #100;
        A = 0; B = 1;C = 1;D = 0;
        #100;
        A = 0; B = 1;C = 1;D = 1;
        #100;
        A = 1; B = 0;C = 0;D = 0;
        #100;
        A = 1; B = 0;C = 0;D = 1;
        #100;
        // Add stimulus here
    end
endmodule
```

output


Name
Value
a
b
c
d
e
f
g
A
B
C
D
0
0
0
1
1
0
0
1
0
0
1
0 ns
200 ns
400 ns
600 ns
800 ns
930.521 ns
X1: 930.521 ns
Default.wcfg