EEL 5764 Computer Architecture Fall 2021

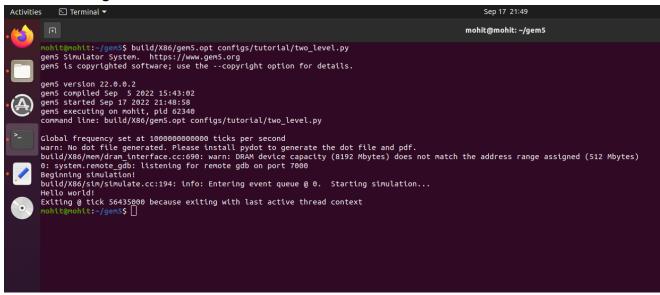
Department of Electrical and Computer Engineering

University of Florida

Lab 3

Student Name: Mohit Palliyil Sathyaseelan

Part A - Adding L1 and L2 caches to the X86 architecture



Part B 1 – Create, compile, and run matmult.c in the new architecture

1496 1562 1628 1694 1760 1826 1892 1958 2004 2156 2222 2288 2354 2420 2486 2552 2618 2618 2750 2816 282 2948 3014 3080 3146 3212 3278 3344 3410 3476 3542 3608	1250 1304 1358 1412 1466 1520 1574 1628 1682 1736 1736 1790 1844 1898 1952 2006 2014 2168 2222 2776 2330 2384 2438 2492 2546 2600	1004 1046 1088 1130 1172 1214 1256 1298 1340 1382 1424 1466 1508 1550 1592 1634 1676 1718 1760 1802 1844 1886 1970 2012	758 788 818 848 878 908 938 968 1058 1058 1118 1148 1178 1208 1238 1298 1358 1358 1418 1418	512 530 548 566 584 602 620 638 656 674 692 710 728 746 764 782 800 818 836 854 872 890 908	266 272 278 284 290 296 302 308 314 320 336 332 338 344 350 356 362 368 374 386 392 398	20 14 8 2 -4 -10 -16 -22 -28 -34 -46 -52 -58 -64 -70 -76 -82 -88 -94 -100 -106 -112	- 226 - 244 - 262 - 280 - 298 - 316 - 334 - 352 - 370 - 388 - 406 - 424 - 442 - 460 - 478 - 496 - 514 - 532 - 550 - 556 - 604	-472 -502 -532 -562 -592 -622 -652 -682 -712 -742 -772 -802 -832 -862 -892 -952 -952 -982 -1012 -1042 -11072	-718 -760 -802 -844 -886 -928 -970 -1012 -1054 -1096 -1138 -1180 -1222 -1264 -1306 -1348 -1390 -1432 -1474 -1516 -1558 -1600	mohit@mohit: ~/ge
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3278 3344 3410 3476 3542 3608	2654	2096	1538	980	422	-136	-694	-1252	-1810	
3344 3410 3476 3542 3608	2708	2138	1568	998	428	-142	-712	-1282	-1852	
3410 3476 3542 3608	2762	2180	1598	1016	434	-148	-730	-1312	-1894	
3476 3542 3608	2816	2222	1628	1034	440	-154	-748	-1342	-1936	
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3608	2924	2306	1688	1070	452	-166	-784	-1402	-2020	
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3674	3032	2390	1748	1106	464	-178	-820	-1462	-2104	
3740	3086	2432	1778	1124	470	-184	-838	-1492	-2146	
3806	3140	2474	1808	1142	476	-190	-856	-1492	-2188	
3872	3194	2516	1838	1142	482	-196 -196	-850 -874	-1522	-2188	
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4004	3302	2600	1898	1176	494	-202	-910	-1612	-2314	
4070	3356	2642	1928		500	-208 -214	-910	-1612 -1642	-2356	
4136	3410	2684	1928	1214 1232	506	-214	-926 -946	-1672	-2398	
4202	3410	208 4 2726	1988	1252	512	-226	-946 -964	-1072	-2440	
4268	3518	2768	2018	1268	518	-232	-982	-1732	-2482	
4334	3572	2810	2048	1286	524	-238	-1000	-1762	-2524	
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Part B 2 - Using simple.py (i.e., without the L1 and L2 caches), run the matmult program

1496	1250	1004	758	512	266	20	226	-472	-718	
1562	1304	1004	738 788	530	272	20 14	-226 -244	- 502	-718 -760	
1628	1358	1046	818	548	278	8	-262	-532	- 802	
1694	1412	1130	848	566	284	2	-280	-562	-844	
1760	1466	1172	878	584	290	-4	-298	-592	-886	
1826	1520	1214	908	602	296	-10	-316	-622	-928	
		1256	938	620	302	-16	-310	-652	-970	
1 Text E	ditor 7	1298	968	638	308	-22	-352	-682	-1012	
2024	1682	1340	998	656	314	-28	-370	-712	-1054	
2090	1736	1382	1028	674	320	-34	-388	-742	-1034	
2156	1790	1424	1058	692	326	-40	-406	-772	-1138	
2222	1844	1466	1088	710	332	-46	-424	-802	-1180	
2288	1898	1508	1118	728	338	-52	-442	-832	-1222	
2354	1952	1550	1118	746	344	-58	-460	-862	-1264	
2420	2006	1592	1178	764	350	-64	-478	-892	-1204	
2486	2060	1634	1208	782	356	- 70	-496	-922	-1348	
2552	2114	1676	1238	800	362	-76	-514	-952	-1348	
2618	2168	1718	1268	818	368	-82	-532	-982	-1432	
2684	2222	1760	1298	836	374	-88	- 550	-1012	-1474	
2750	2276	1802	1328	854	380	-94	- 568	-1012	-1516	
2816	2330	1844	1358	872	386	-100	- 586	-1072	-1558	
2882	2384	1886	1388	890	392	-106	-604	-1102	-1600	
2948	2438	1928	1418	908	398	-112	-622	-1132	-1642	
3014	2492	1970	1448	926	404	-118	-640	-1162	-1684	
3080	2546	2012	1478	944	410	-124	-658	-1192	-1726	
3146	2600	2054	1508	962	416	-130	-676	-1222	-1768	
3212	2654	2096	1538	980	422	-136	-694	-1252	-1810	
3278	2708	2138	1568	998	428	-142	-712	-1282	-1852	
3344	2762	2180	1598	1016	434	-148	-730	-1312	-1894	
3410	2816	2222	1628	1034	440	-154	-748	-1342	-1936	
3476	2870	2264	1658	1052	446	-160	-766	-1372	-1978	
3542	2924	2306	1688	1070	452	-166	-784	-1402	-2020	
3608	2978	2348	1718	1088	458	-172	-802	-1432	-2062	
3674	3032	2390	1748	1106	464	-178	-820	-1462	-2104	
3740	3086	2432	1778	1124	470	-184	-838	-1492	-2146	
3806	3140	2474	1808	1142	476	-190	-856	-1522	-2188	
3872	3194	2516	1838	1160	482	-196	-874	-1552	-2230	
3938	3248	2558	1868	1178	488	-202	-892	-1582	-2272	
4004	3302	2600	1898	1196	494	-208	-910	-1612	-2314	
4070	3356	2642	1928	1214	500	-214	-928	-1642	-2356	
4136	3410	2684	1958	1232	506	-220	-946	-1672	-2398	
4202	3464	2726	1988	1250	512	-226	-964	-1702	-2440	
4268	3518	2768	2018	1268	518	-232	-982	-1732	-2482	
4334	3572	2810	2048	1286	524	-238	-1000	-1762	-2524	
4400	3626	2852	2078	1304	530	-244	-1018	-1792	-2566	
*****	*****	*****	*****	*****	*****	*****				

Part B 3 -In the cache.py script, vary L1Cache data_latency from 1, 2, 4, 8

Exiting @ tick 4841867000 because exiting with last active thread context L1Cache data_latency - 1

Exiting @ tick 4841867000 because exiting with last active thread context L1Cache data_latency - 2

Exiting @ tick 9099418000 because exiting with last active thread context L1Cache data_latency - 4

Exiting @ tick 17613411000 because exiting with last active thread context L1Cache data_latency - 8

Comparing the ticks of 1 and 2 L1Cache data latency they are similar, although for 4 and 8 the ticks are much higher than for 1 and 2 data latency.

PART C

[system.cpu.dcache.replacement_policy] type=LRURP eventq_index=0

[system.cpu.dcache.tags] type=BaseSetAssoc children=indexing_policy power_state assoc=2 block_size=64 clk domain=system.clk domain entry size=64 eventq_index=0 indexing policy=system.cpu.dcache.tags.indexing policy power model= power state=system.cpu.dcache.tags.power state replacement policy=system.cpu.dcache.replacement policy sequential_access=false size=65536 system=system tag latency=2 warmup_percentage=0

[system.cpu.dcache.tags.indexing_policy] type=SetAssociative assoc=2 entry_size=64 eventq_index=0 size=65536

[system.cpu.icache.replacement_policy] type=LRURP eventq_index=0

[system.cpu.icache.tags]
type=BaseSetAssoc
children=indexing_policy power_state
assoc=2
block_size=64
clk_domain=system.clk_domain
entry_size=64
eventq_index=0
indexing_policy=system.cpu.icache.tags.indexing_policy
power_model=
power_state=system.cpu.icache.tags.power_state
replacement_policy=system.cpu.icache.replacement_policy
sequential_access=false
size=16384

system=system tag_latency=2 warmup_percentage=0

[system.cpu.icache.tags.indexing_policy] type=SetAssociative assoc=2 entry_size=64 eventq_index=0 size=16384

[system.l2cache.replacement_policy] type=LRURP eventq_index=0

[system.l2cache.tags] type=BaseSetAssoc children=indexing_policy power_state assoc=8 block_size=64 clk_domain=system.clk_domain entry size=64 eventq_index=0 indexing_policy=system.l2cache.tags.indexing_policy power model= power_state=system.l2cache.tags.power_state replacement policy=system.l2cache.replacement policy sequential_access=false size=262144 system=system tag_latency=20 warmup_percentage=0

[system.l2cache.tags.indexing_policy] type=SetAssociative assoc=8 entry_size=64 eventq_index=0 size=262144