

# **EEL 5764 Computer Architecture Fall 2021**

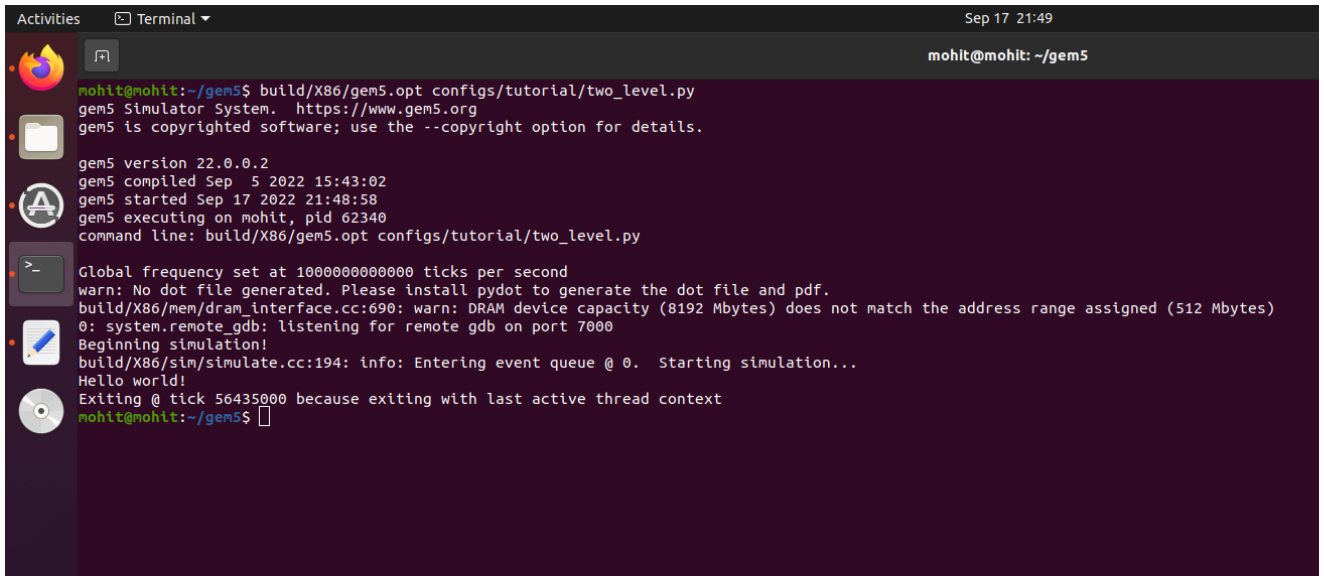
**Department of Electrical and Computer Engineering**

**University of Florida**

**Lab 3**

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## Part A – Adding L1 and L2 caches to the X86 architecture



The screenshot shows a terminal window titled "Terminal" with a dark background. The user "mohit" is logged in at "mohit@mohit: ~/gem5". The terminal displays the output of running the command `build/X86/gem5.opt configs/tutorial/two_level.py`. The output includes version information, compilation details, and simulation logs. The simulation starts with a global frequency of 1000000000000 ticks per second and a warning about the dot file. It then begins the simulation, prints "Hello world!", and exits at tick 56435000.

```
mohit@mohit:~/gem5$ build/X86/gem5.opt configs/tutorial/two_level.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Sep  5 2022 15:43:02
gem5 started Sep 17 2022 21:48:58
gem5 executing on mohit, pid 62340
command line: build/X86/gem5.opt configs/tutorial/two_level.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 56435000 because exiting with last active thread context
mohit@mohit:~/gem5$
```

## Part B 1 – Create, compile, and run matmult.c in the new architecture

```
Activities Terminal Sep 17 23:05 mohit@mohit: ~/gem5

1496 1250 1004 758 512 266 20 -226 -472 -718
1562 1304 1046 788 530 272 14 -244 -502 -760
1628 1358 1088 818 548 278 8 -262 -532 -802
1694 1412 1130 848 566 284 2 -280 -562 -844
1760 1466 1172 878 584 290 -4 -298 -592 -886
1826 1520 1214 908 602 296 -10 -316 -622 -928
1892 1574 1256 938 620 302 -16 -334 -652 -970
1958 1628 1298 968 638 308 -22 -352 -682 -1012
2024 1682 1340 998 656 314 -28 -370 -712 -1054
2090 1736 1382 1028 674 320 -34 -388 -742 -1096
2156 1790 1424 1058 692 326 -40 -406 -772 -1138
2222 1844 1466 1088 710 332 -46 -424 -802 -1180
2288 1898 1508 1118 728 338 -52 -442 -832 -1222
2354 1952 1550 1148 746 344 -58 -460 -862 -1264
2420 2006 1592 1178 764 350 -64 -478 -892 -1306
2486 2060 1634 1208 782 356 -70 -496 -922 -1348
2552 2114 1676 1238 800 362 -76 -514 -952 -1390
2618 2168 1718 1268 818 368 -82 -532 -982 -1432
2684 2222 1760 1298 836 374 -88 -550 -1012 -1474
2750 2276 1802 1328 854 380 -94 -568 -1042 -1516
2816 2330 1844 1358 872 386 -100 -586 -1072 -1558
2882 2384 1886 1388 890 392 -106 -604 -1102 -1600
2948 2438 1928 1418 908 398 -112 -622 -1132 -1642
3014 2492 1970 1448 926 404 -118 -640 -1162 -1684
3080 2546 2012 1478 944 410 -124 -658 -1192 -1726
3146 2600 2054 1508 962 416 -130 -676 -1222 -1768
3212 2654 2096 1538 980 422 -136 -694 -1252 -1810
3278 2708 2138 1568 998 428 -142 -712 -1282 -1852
3344 2762 2180 1598 1016 434 -148 -730 -1312 -1894
3410 2816 2222 1628 1034 440 -154 -748 -1342 -1936
3476 2870 2264 1658 1052 446 -160 -766 -1372 -1978
3542 2924 2306 1688 1070 452 -166 -784 -1402 -2020
3608 2978 2348 1718 1088 458 -172 -802 -1432 -2062
3674 3032 2390 1748 1106 464 -178 -820 -1462 -2104
3740 3086 2432 1778 1124 470 -184 -838 -1492 -2146
3806 3140 2474 1808 1142 476 -190 -856 -1522 -2188
3872 3194 2516 1838 1160 482 -196 -874 -1552 -2230
3938 3248 2558 1868 1178 488 -202 -892 -1582 -2272
4004 3302 2600 1898 1196 494 -208 -910 -1612 -2314
4070 3356 2642 1928 1214 500 -214 -928 -1642 -2356
4136 3410 2684 1958 1232 506 -220 -946 -1672 -2398
4202 3464 2726 1988 1250 512 -226 -964 -1702 -2440
4268 3518 2768 2018 1268 518 -232 -982 -1732 -2482
4334 3572 2810 2048 1286 524 -238 -1000 -1762 -2524
4400 3626 2852 2078 1304 530 -244 -1018 -1792 -2566
*****

Exiting @ tick 4841867000 because exiting with last active thread context
mohit@mohit:~/gem5$
```

## Part B 2 - Using simple.py (i.e., without the L1 and L2 caches), run the matmult program

```
Activities Terminal Sep 1
mohit@m

1496 1250 1004 758 512 266 20 -226 -472 -718
1562 1304 1046 788 530 272 14 -244 -502 -760
1628 1358 1088 818 548 278 8 -262 -532 -802
1694 1412 1130 848 566 284 2 -280 -562 -844
1760 1466 1172 878 584 290 -4 -298 -592 -886
1826 1520 1214 908 602 296 -10 -316 -622 -928
1892 1574 1256 938 620 302 -16 -334 -652 -970
1958 1628 1298 968 638 308 -22 -352 -682 -1012
2024 1682 1340 998 656 314 -28 -370 -712 -1054
2090 1736 1382 1028 674 320 -34 -388 -742 -1096
2156 1790 1424 1058 692 326 -40 -406 -772 -1138
2222 1844 1466 1088 710 332 -46 -424 -802 -1180
2288 1898 1508 1118 728 338 -52 -442 -832 -1222
2354 1952 1550 1148 746 344 -58 -460 -862 -1264
2420 2006 1592 1178 764 350 -64 -478 -892 -1306
2486 2060 1634 1208 782 356 -70 -496 -922 -1348
2552 2114 1676 1238 800 362 -76 -514 -952 -1390
2618 2168 1718 1268 818 368 -82 -532 -982 -1432
2684 2222 1760 1298 836 374 -88 -550 -1012 -1474
2750 2276 1802 1328 854 380 -94 -568 -1042 -1516
2816 2330 1844 1358 872 386 -100 -586 -1072 -1558
2882 2384 1886 1388 890 392 -106 -604 -1102 -1600
2948 2438 1928 1418 908 398 -112 -622 -1132 -1642
3014 2492 1970 1448 926 404 -118 -640 -1162 -1684
3080 2546 2012 1478 944 410 -124 -658 -1192 -1726
3146 2600 2054 1508 962 416 -130 -676 -1222 -1768
3212 2654 2096 1538 980 422 -136 -694 -1252 -1810
3278 2708 2138 1568 998 428 -142 -712 -1282 -1852
3344 2762 2180 1598 1016 434 -148 -730 -1312 -1894
3410 2816 2222 1628 1034 440 -154 -748 -1342 -1936
3476 2870 2264 1658 1052 446 -160 -766 -1372 -1978
3542 2924 2306 1688 1070 452 -166 -784 -1402 -2020
3608 2978 2348 1718 1088 458 -172 -802 -1432 -2062
3674 3032 2390 1748 1106 464 -178 -820 -1462 -2104
3740 3086 2432 1778 1124 470 -184 -838 -1492 -2146
3806 3140 2474 1808 1142 476 -190 -856 -1522 -2188
3872 3194 2516 1838 1160 482 -196 -874 -1552 -2230
3938 3248 2558 1868 1178 488 -202 -892 -1582 -2272
4004 3302 2600 1898 1196 494 -208 -910 -1612 -2314
4070 3356 2642 1928 1214 500 -214 -928 -1642 -2356
4136 3410 2684 1958 1232 506 -220 -946 -1672 -2398
4202 3464 2726 1988 1250 512 -226 -964 -1702 -2440
4268 3518 2768 2018 1268 518 -232 -982 -1732 -2482
4334 3572 2810 2048 1286 524 -238 -1000 -1762 -2524
4400 3626 2852 2078 1304 530 -244 -1018 -1792 -2566
*****

Exiting @ tick 113862084000 because exiting with last active thread context
mohit@mohit:~/gen5$
```

**Part B 3 -In the cache.py script, vary L1Cache data\_latency from 1, 2, 4, 8**

**Exiting @ tick 4841867000 because exiting with last active thread context**  
L1Cache data\_latency - 1

**Exiting @ tick 4841867000 because exiting with last active thread context**  
L1Cache data\_latency - 2

**Exiting @ tick 9099418000 because exiting with last active thread context**  
L1Cache data\_latency - 4

**Exiting @ tick 17613411000 because exiting with last active thread context**  
L1Cache data\_latency - 8

Comparing the ticks of 1 and 2 L1Cache data latency they are similar, although for 4 and 8 the ticks are much higher than for 1 and 2 data latency.

## PART C

[system.cpu.dcache.replacement\_policy]  
type=LRURP  
eventq\_index=0

[system.cpu.dcache.tags]  
type=BaseSetAssoc  
children=indexing\_policy power\_state  
assoc=2  
block\_size=64  
clk\_domain=system.clk\_domain  
entry\_size=64  
eventq\_index=0  
indexing\_policy=system.cpu.dcache.tags.indexing\_policy  
power\_model=  
power\_state=system.cpu.dcache.tags.power\_state  
replacement\_policy=system.cpu.dcache.replacement\_policy  
sequential\_access=false  
size=65536  
system=system  
tag\_latency=2  
warmup\_percentage=0

[system.cpu.dcache.tags.indexing\_policy]  
type=SetAssociative  
assoc=2  
entry\_size=64  
eventq\_index=0  
size=65536

[system.cpu.icache.replacement\_policy]  
type=LRURP  
eventq\_index=0

[system.cpu.icache.tags]  
type=BaseSetAssoc  
children=indexing\_policy power\_state  
assoc=2  
block\_size=64  
clk\_domain=system.clk\_domain  
entry\_size=64  
eventq\_index=0  
indexing\_policy=system.cpu.icache.tags.indexing\_policy  
power\_model=  
power\_state=system.cpu.icache.tags.power\_state  
replacement\_policy=system.cpu.icache.replacement\_policy  
sequential\_access=false  
size=16384

system=system  
tag\_latency=2  
warmup\_percentage=0

[system.cpu.icache.tags.indexing\_policy]  
type=SetAssociative  
assoc=2  
entry\_size=64  
eventq\_index=0  
size=16384

[system.l2cache.replacement\_policy]  
type=LRURP  
eventq\_index=0

[system.l2cache.tags]  
type=BaseSetAssoc  
children=indexing\_policy power\_state  
assoc=8  
block\_size=64  
clk\_domain=system.clk\_domain  
entry\_size=64  
eventq\_index=0  
indexing\_policy=system.l2cache.tags.indexing\_policy  
power\_model=  
power\_state=system.l2cache.tags.power\_state  
replacement\_policy=system.l2cache.replacement\_policy  
sequential\_access=false  
size=262144  
system=system  
tag\_latency=20  
warmup\_percentage=0

[system.l2cache.tags.indexing\_policy]  
type=SetAssociative  
assoc=8  
entry\_size=64  
eventq\_index=0  
size=262144