EEL 5764 Computer Architecture Fall 2021

Department of Electrical and Computer Engineering

University of Florida

Lab 2

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Part#: Name	CPU model	CPU clock frequency	Memory model	Exit tick#
Part1(a): 1GHz	TimingSimpleCPU	1 GHz	DDR3_1600_8X8	454646000
Part1(b): 2GHz	TimingSimpleCPU	2GHz	DDR3_1600_8X8	406055500
Part1(b): 4GHz	TimingSimpleCPU	4GHz	DDR3_1600_8X8	379133750
Part1(c): DDR4	TimingSimpleCPU	1GHZ	DDR4_2400_8X8	450198000
Part1(c): DDR3	TimingSimpleCPU	1GHZ	DDR3_2133_8X8	437364000
Part1(c): HBM	TimingSimpleCPU	1GHZ	HBM_1000_4H_1X64	470718000
Part 1(d): O3CPU	O3CPU	1GHZ	DDR3_1600_8X8	76822000
Part 2:" MyHello	TimingSimpleCPU	1GHZ	DDR3_1600_8X8	941012000

The Exit ticks decreases as we increase the CPU Clock Frequency while having the CPU Model as TimingSimpleCPU, which means the simulation was done faster. Changing between DDR3 and DDR4 or other models made the performance better and faster than DDR3 while keeping the CPU model as TimingSimpleCPU and CPU clock frequency as 1 GHz. Using HBM memory model is slower than DDR3 and DDR4. Using O3CPU model made the execution a lot faster than using TimingSimpleCPU.

Part 1(a)

```
mo@mo:~/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Aug 26 2022 16:13:49
gem5 started Sep  3 2022 16:51:37
gem5 executing on mo, pid 3744
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 454646000 because exiting with last active thread context
```

Part 1(b)1

```
mo@mo:~/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Aug 26 2022 16:13:49
gem5 started Sep  3 2022 16:57:46
gem5 executing on mo, pid 4305
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 406055500 because exiting with last active thread context
```

Part 1(b)2

```
mo@mo:~/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Aug 26 2022 16:13:49
gem5 started Sep  3 2022 17:00:44
gem5 executing on mo, pid 4317
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 379133750 because exiting with last active thread context
```

Part 1(c)1

```
mo@mo:~/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Aug 26 2022 16:13:49
gem5 started Sep  3 2022 17:01:54
gem5 executing on mo, pid 4332
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (16384 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 450198000 because exiting with last active thread context
```

Part 1(c)2

```
mo@mo:~/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Aug 26 2022 16:13:49
gem5 started Sep  3 2022 17:03:14
gem5 executing on mo, pid 4342
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 437364000 because exiting with last active thread context
```

Part 1(c)3

```
mo@mo:~/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Aug 26 2022 16:13:49
gem5 started Sep  3 2022 17:04:13
gem5 executing on mo, pid 4348
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (256 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 470718000 because exiting with last active thread context
```

Part 1(d)

```
mo@mo:~/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Aug 26 2022 16:13:49
gem5 started Sep  3 2022 17:06:10
gem5 executing on mo, pid 4364
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address
range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 76822000 because exiting with last active thread context
```

Part 2

```
mo@mo:~/gem5$ cd
mo@mo:~$ cd gem5/configs/tutorial/part1/my_hello/
mo@mo:~/gem5/configs/tutorial/part1/my_hello$ gcc -O0 -ggdb3 -std=c99 -static -o hellomohit hello.c
mo@mo:~/gem5/configs/tutorial/part1/my_hello$ cd
mo@mo:~$ cd gem5
mo@mo:~/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Aug 26 2022 16:13:49
gem5 started Sep  3 2022 17:18:57
gem5 executing on mo, pid 4633
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range
assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
build/X86/sim/mem_state.cc:443: info: Increasing stack size by one page.
build/X86/sim/syscall_emul.hh:1015: warn: readlink() called on '/proc/self/exe' may yield unexpected results in
 various settings.
      Returning '/home/mo/gem5/configs/tutorial/part1/my_hello/hellomohit'
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
Mohit Palliyil Sathyaseelan says hello!
Exiting @ tick 941012000 because exiting with last active thread context
mo@mo:~/gem5$
```

1. This statement, system.clk_domain.clock = '1GHz',is specified in simple.py. Which statement(s) in the config.ini file contain the corresponding information?
Answer: In [system.clk_domain], the statement ‘clock=1000’ specifies that system clock is 1GHz (1000 ticks).

2. This statement, system.cpu = TimingSimpleCPU(), is specified in simple.py. Which statement(s) in the config.ini file contain the corresponding information?
Answer: in [system.cpu], the statement ‘type=BaseTimingSimpleCPU’ specifies the CPU type.

3. The following statements are founded in the config.ini file, defining the “children” SimObjects for the system SimObject (i.e., defining the component of this system).
[system]
type=System
children=clk_domain cpu dvfs_handler mem_ctrl membus workload
Which of these SimObject components are defined in the simple.py configuration script? (Note: the rest of the “children” SimObjects are defaults).
Answer: clk_domain, cpu, mem_ctrl, membus and workload

4. After you executed the simply.py script, some of the summary statistics are shown in the terminal:
(a) “Global frequency set at 1000000000000 ticks per second”
In the stats.txt file, what line number is this statistics displayed?
Answer: Line 6, simFreq
(b) “Exiting @ tick 454646000 because exiting with last active thread context”

In the stats.txt file, list all the line numbers in which this tick number is displayed, not just the summary lines (4 and 5).

Answer:

Lines 4(simTicks)

5 (finalTick)

108 (cpu.mmu.dtb.walker.power_state.pwrStateResidencyTicks::UNDEFINED)

113 (cpu.mmu.itb.walker.power_state.pwrStateResidencyTicks::UNDEFINED)

114 (cpu.power_state.pwrStateResidencyTicks::ON)

374 (mem_ctrl.dram.power_state.pwrStateResidencyTicks)

413 (mem_ctrl.power_state.pwrStateResidencyTicks)

440 (membus.power_state.pwrStateResidencyTicks)