EEL 5764 Computer Architecture Fall 2021

Department of Electrical and Computer Engineering

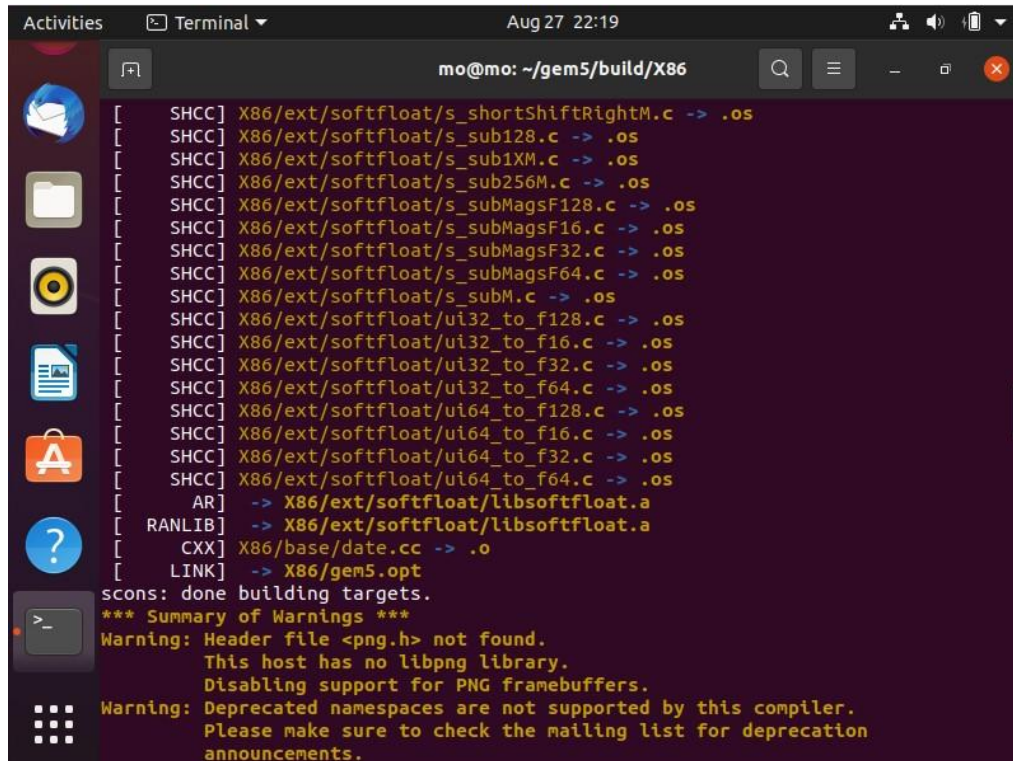# University of Florida

Lab 1

Student Name : Mohit Palliyil Sathyaseelan
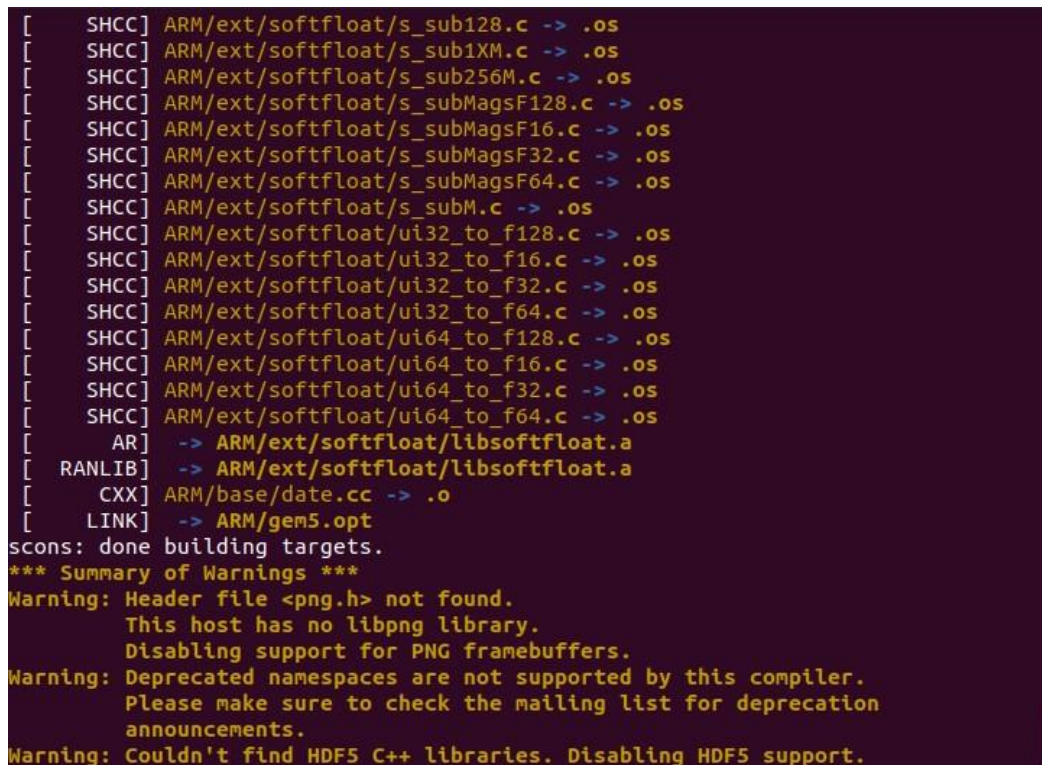
1.Scons build/X86/gem5.opt -j9 (using 8 cores)
Username is mo

2. Scons build/ARM/gem5.opt -j9 (using 8 cores)

3.

```
mo@mo: ~/gem5/build/X86
m  Thunderbird Mail  d build
mo@mo:~/gem5/build$ cd X86/
mo@mo:~/gem5/build/X86$ ls -l
total 596888
drwxrwxr-x 11 mo mo       4096 Aug 26 15:48 arch
drwxrwxr-x  7 mo mo       4096 Aug 26 16:13 base
drwxrwxr-x  2 mo mo       4096 Aug 26 15:40 config
drwxrwxr-x 10 mo mo       4096 Aug 26 15:48 cpu
drwxrwxr-x  2 mo mo      24576 Aug 26 16:12 debug
drwxrwxr-x 18 mo mo       4096 Aug 26 15:23 dev
drwxrwxr-x  2 mo mo       4096 Aug 26 16:11 enums
drwxrwxr-x 13 mo mo       4096 Aug 26 14:04 ext
drwxrwxr-x  3 mo mo       4096 Aug 26 16:15 gem5.build
-rwxrwxr-x  1 mo mo 607749120 Aug 26 16:15 gem5.opt
-rwxrwxr-x  1 mo mo    595832 Aug 26 14:04 gem5py
-rwxrwxr-x  1 mo mo   2726088 Aug 26 14:15 gem5py_m5
drwxrwxr-x  2 mo mo       4096 Aug 26 14:31 gpu-compute
drwxrwxr-x  4 mo mo       4096 Aug 26 15:39 kern
drwxrwxr-x  3 mo mo       4096 Aug 26 14:04 learning_gem5
drwxrwxr-x  7 mo mo      12288 Aug 26 15:49 mem
drwxrwxr-x  2 mo mo      20480 Aug 26 16:12 params
drwxrwxr-x  2 mo mo       4096 Aug 26 15:42 proto
drwxrwxr-x  6 mo mo       4096 Aug 26 14:57 python
lrwxrwxrwx  1 mo mo         28 Aug 26 14:04 SConscript -> /home/mo/gem5/src/SCon
script
drwxrwxr-x  5 mo mo      12288 Aug 26 16:10 sim
drwxrwxr-x  2 mo mo       4096 Aug 26 14:16 sst
drwxrwxr-x 12 mo mo       4096 Aug 26 15:44 systemc
mo@mo:~/gem5/build/X86$
```

4.

```
mo@mo: ~/gem5/build/ARM
mo@mo:~/gem5/build/X86$ cd
mo@mo:~$ cd gem5//build/ARM/
mo@mo:~/gem5/build/ARM$ ls -l
total 698504
drwxrwxr-x 11 mo mo       4096 Aug 27 15:35 arch
drwxrwxr-x  7 mo mo       4096 Aug 27 15:53 base
drwxrwxr-x  2 mo mo       4096 Aug 27 13:59 config
drwxrwxr-x 10 mo mo       4096 Aug 27 15:35 cpu
drwxrwxr-x  2 mo mo      28672 Aug 27 15:48 debug
drwxrwxr-x 18 mo mo       4096 Aug 27 15:35 dev
drwxrwxr-x  2 mo mo       4096 Aug 27 15:46 enums
drwxrwxr-x 13 mo mo       4096 Aug 27 12:11 ext
drwxrwxr-x  3 mo mo       4096 Aug 27 15:55 gem5.build
-rwxrwxr-x  1 mo mo 711755976 Aug 27 15:54 gem5.opt
-rwxrwxr-x  1 mo mo    595832 Aug 27 12:12 gem5py
-rwxrwxr-x  1 mo mo   2768376 Aug 27 12:22 gem5py_m5
drwxrwxr-x  2 mo mo       4096 Aug 27 15:35 gpu-compute
drwxrwxr-x  4 mo mo       4096 Aug 27 15:35 kern
drwxrwxr-x  3 mo mo       4096 Aug 27 12:11 learning_gem5
drwxrwxr-x  7 mo mo      12288 Aug 27 15:35 mem
drwxrwxr-x  2 mo mo      20480 Aug 27 15:47 params
drwxrwxr-x  2 mo mo       4096 Aug 27 15:35 proto
drwxrwxr-x  6 mo mo       4096 Aug 27 15:35 python
lrwxrwxrwx  1 mo mo         28 Aug 27 15:35 SConscript -> /home/mo/gem5/src/SCon
script
drwxrwxr-x  5 mo mo      12288 Aug 27 15:45 sim
drwxrwxr-x  2 mo mo       4096 Aug 27 15:35 sst
drwxrwxr-x 12 mo mo       4096 Aug 27 15:35 systemc
mo@mo:~/gem5/build/ARM$
```
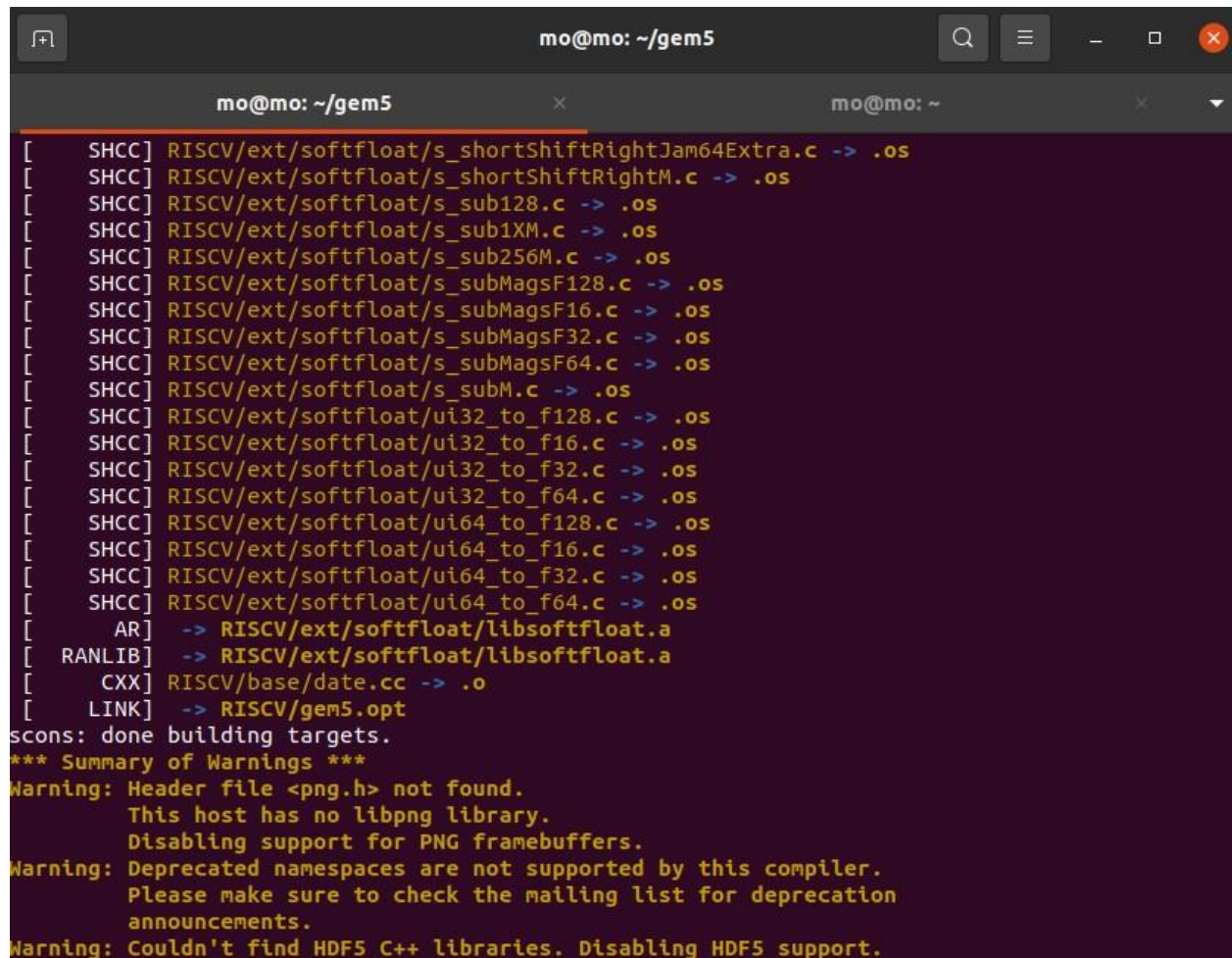
5. Does gem5 support the RISC-V CPU? If yes, then what is the command to build it?

Yes, gem5 supports RISC-V.
http://resources.gem5.org/resources/riscv-fs (The last section has steps to build RISCV)

We can just run this command to build RISCV
python3 `which scons` build/RISCV/gem5.opt -j9


```
                                        mo@mo: ~/gem5                          Q    ≡   _   □   ✕

              mo@mo: ~/gem5                    ✕           mo@mo: ~              ✕        ▾
[    SHCC] RISCV/ext/softfloat/s_shortShiftRightJam64Extra.c -> .os
[    SHCC] RISCV/ext/softfloat/s_shortShiftRightM.c -> .os
[    SHCC] RISCV/ext/softfloat/s_sub128.c -> .os
[    SHCC] RISCV/ext/softfloat/s_sub1XM.c -> .os
[    SHCC] RISCV/ext/softfloat/s_sub256M.c -> .os
[    SHCC] RISCV/ext/softfloat/s_subMagsF128.c -> .os
[    SHCC] RISCV/ext/softfloat/s_subMagsF16.c -> .os
[    SHCC] RISCV/ext/softfloat/s_subMagsF32.c -> .os
[    SHCC] RISCV/ext/softfloat/s_subMagsF64.c -> .os
[    SHCC] RISCV/ext/softfloat/s_subM.c -> .os
[    SHCC] RISCV/ext/softfloat/ui32_to_f128.c -> .os
[    SHCC] RISCV/ext/softfloat/ui32_to_f16.c -> .os
[    SHCC] RISCV/ext/softfloat/ui32_to_f32.c -> .os
[    SHCC] RISCV/ext/softfloat/ui32_to_f64.c -> .os
[    SHCC] RISCV/ext/softfloat/ui64_to_f128.c -> .os
[    SHCC] RISCV/ext/softfloat/ui64_to_f16.c -> .os
[    SHCC] RISCV/ext/softfloat/ui64_to_f32.c -> .os
[    SHCC] RISCV/ext/softfloat/ui64_to_f64.c -> .os
[      AR]  -> RISCV/ext/softfloat/libsoftfloat.a
[  RANLIB]  -> RISCV/ext/softfloat/libsoftfloat.a
[     CXX] RISCV/base/date.cc -> .o
[    LINK]  -> RISCV/gem5.opt
scons: done building targets.
*** Summary of Warnings ***
Warning: Header file <png.h> not found.
         This host has no libpng library.
         Disabling support for PNG framebuffers.
Warning: Deprecated namespaces are not supported by this compiler.
         Please make sure to check the mailing list for deprecation
         announcements.
Warning: Couldn't find HDF5 C++ libraries. Disabling HDF5 support.
```