EEL 5764 Computer Architecture Fall 2021

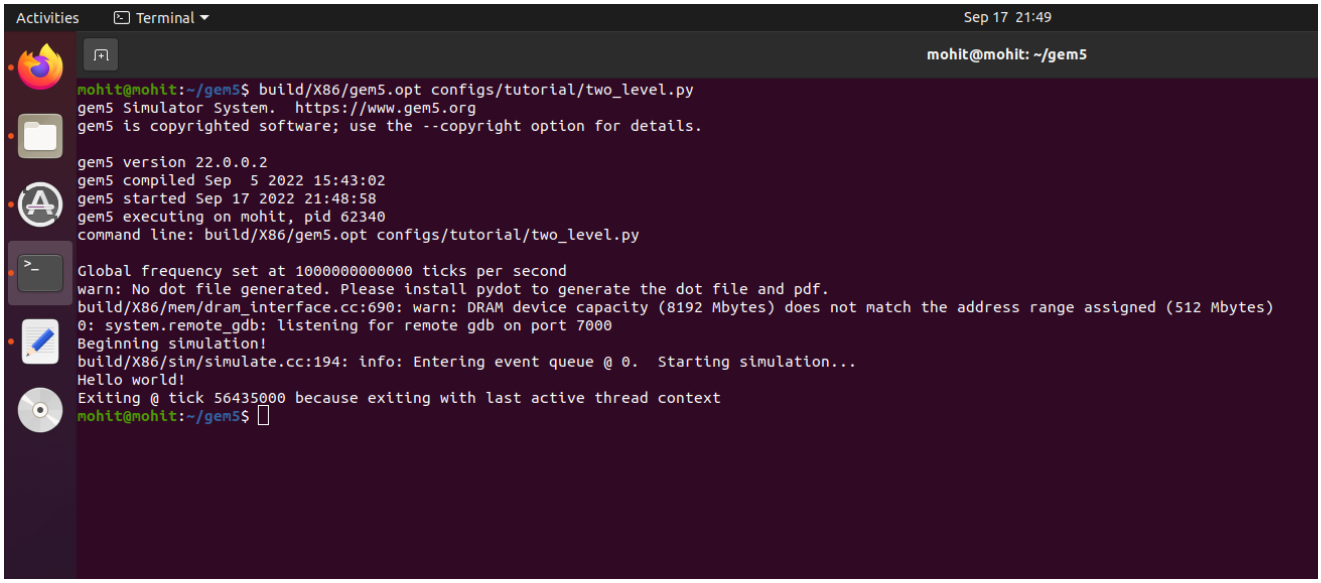
Department of Electrical and Computer Engineering

University of Florida

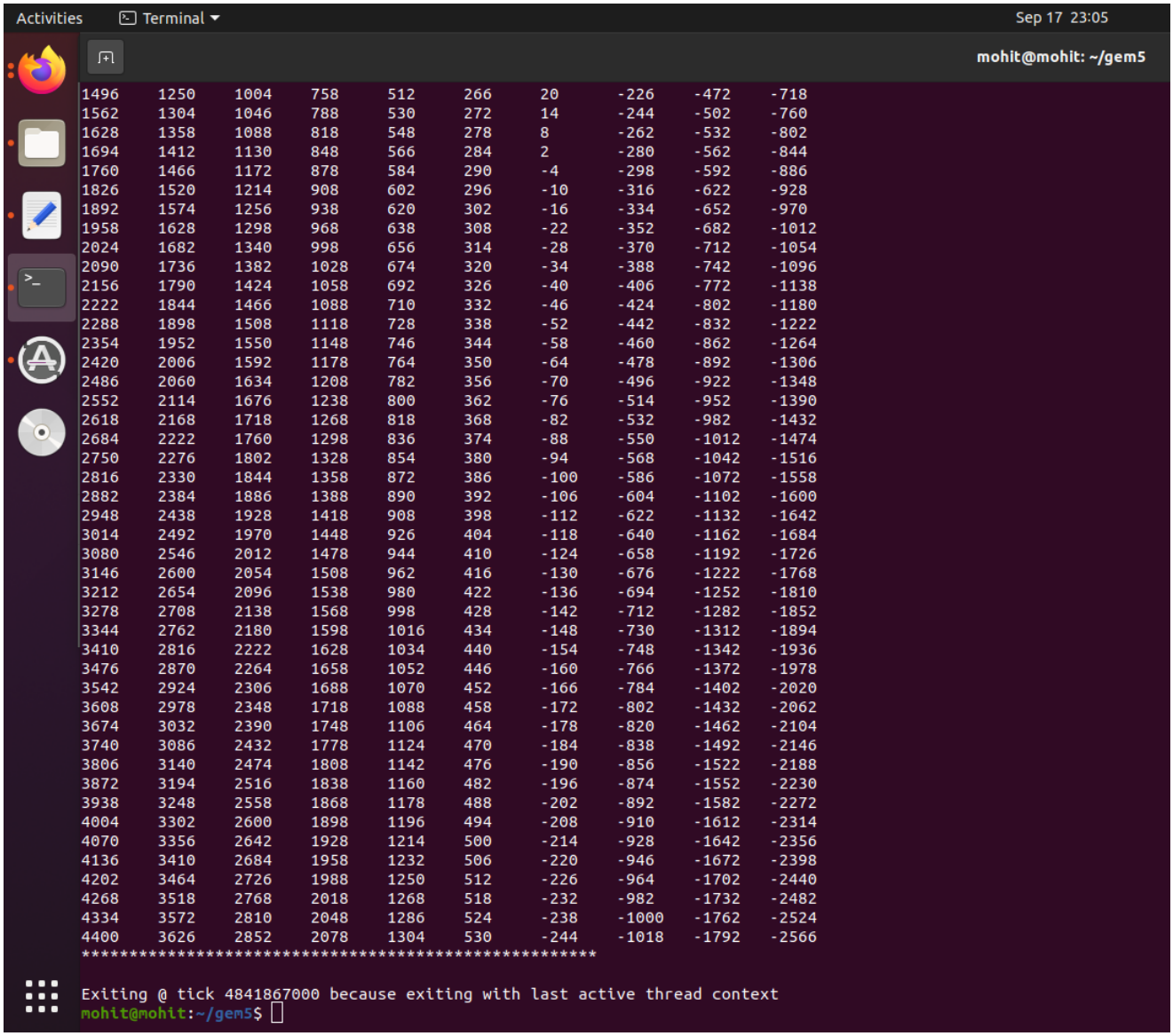
Lab 3

Student Name : Mohit Palliyil Sathyaseelan

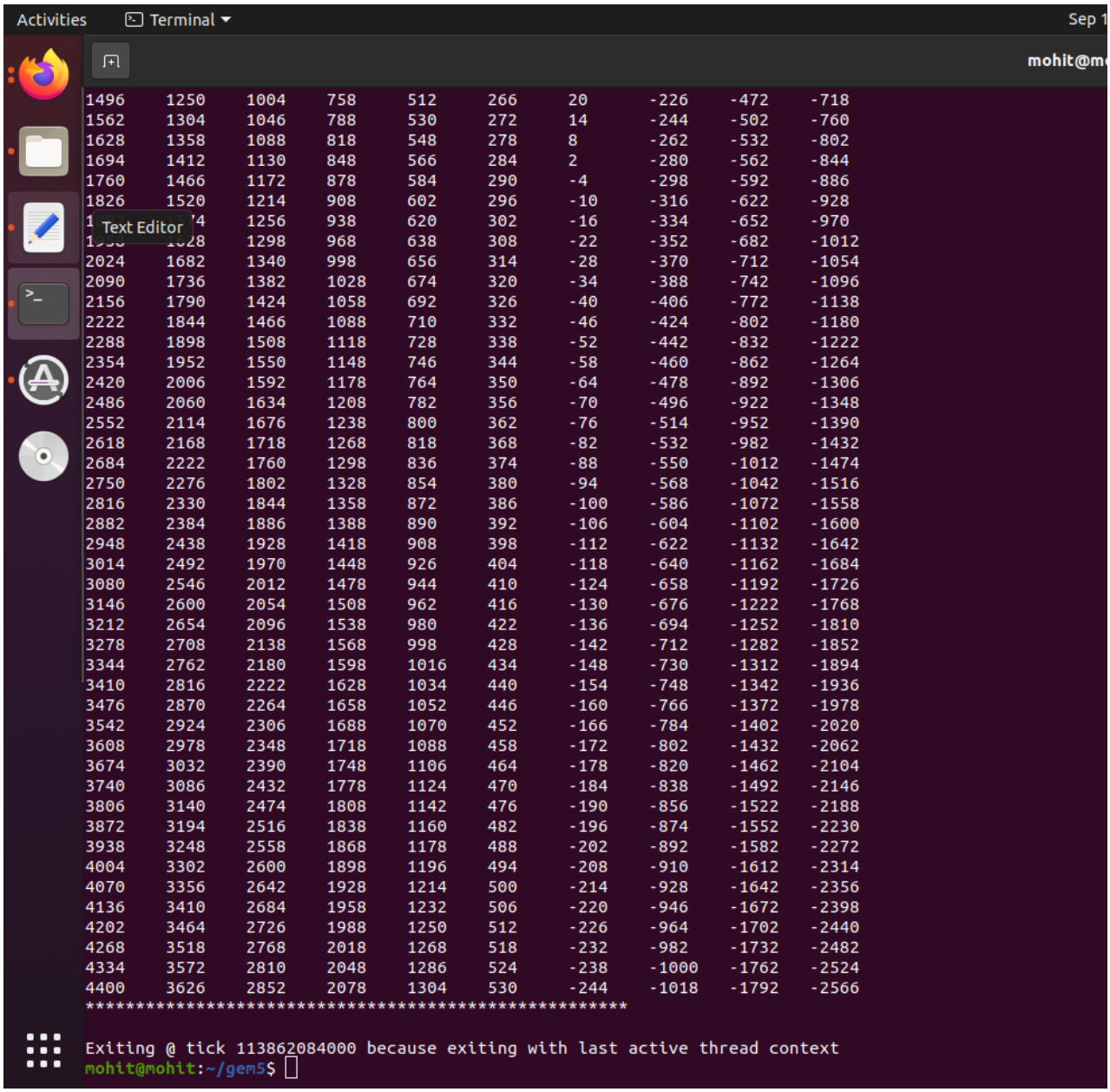
Part A – Adding L1 and L2 caches to the X86 architecture



Part B 1 – Create, compile, and run matmult.c in the new architecture



Part B 2 - Using simple.py (i.e., without the L1 and L2 caches), run the matmult program



Part B 3 -In the cache.py script, vary L1Cache data_latency from 1, 2, 4, 8

Exiting @ tick 4841867000 because exiting with last active thread context
L1Cache data_latency - 1

Exiting @ tick 4841867000 because exiting with last active thread context
L1Cache data_latency - 2

Exiting @ tick 9099418000 because exiting with last active thread context
L1Cache data_latency - 4

Exiting @ tick 17613411000 because exiting with last active thread context
L1Cache data_latency - 8

Comparing the ticks of 1 and 2 L1Cache data latency they are similar, although for 4 and 8 the ticks are much higher than for 1 and 2 data latency.

PART C

```
[system.cpu.dcache.replacement_policy]
type=LRURP
eventq_index=0

[system.cpu.dcache.tags]
type=BaseSetAssoc
children=indexing_policy power_state
assoc=2
block_size=64
clk_domain=system.clk_domain
entry_size=64
eventq_index=0
indexing_policy=system.cpu.dcache.tags.indexing_policy
power_model=
power_state=system.cpu.dcache.tags.power_state
replacement_policy=system.cpu.dcache.replacement_policy
sequential_access=false
size=65536
system=system
tag_latency=2
warmup_percentage=0

[system.cpu.dcache.tags.indexing_policy]
type=SetAssociative
assoc=2
entry_size=64
eventq_index=0
size=65536


[system.cpu.icache.replacement_policy]
type=LRURP
eventq_index=0

[system.cpu.icache.tags]
type=BaseSetAssoc
children=indexing_policy power_state
assoc=2
block_size=64
clk_domain=system.clk_domain
entry_size=64
eventq_index=0
indexing_policy=system.cpu.icache.tags.indexing_policy
power_model=
power_state=system.cpu.icache.tags.power_state
replacement_policy=system.cpu.icache.replacement_policy
sequential_access=false
size=16384
```

system=system
tag_latency=2
warmup_percentage=0

[system.cpu.icache.tags.indexing_policy]
type=SetAssociative
assoc=2
entry_size=64
eventq_index=0
size=16384

[system.l2cache.replacement_policy]
type=LRURP
eventq_index=0

[system.l2cache.tags]
type=BaseSetAssoc
children=indexing_policy power_state
assoc=8
block_size=64
clk_domain=system.clk_domain
entry_size=64
eventq_index=0
indexing_policy=system.l2cache.tags.indexing_policy
power_model=
power_state=system.l2cache.tags.power_state
replacement_policy=system.l2cache.replacement_policy
sequential_access=false
size=262144
system=system
tag_latency=20
warmup_percentage=0

[system.l2cache.tags.indexing_policy]
type=SetAssociative
assoc=8
entry_size=64
eventq_index=0
size=262144