

Introduction to JTAG



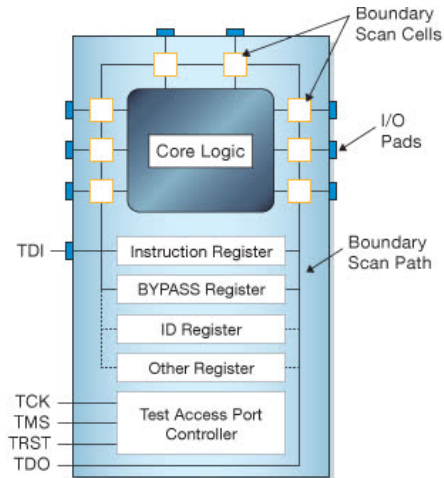
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Boundary Scan
JTAG Intro
JTAG Architecture

- ▶ Allows you to debug individual IO pins of a chip in an assembled PCB (without physical access)
- ▶ Uses extra circuitry (called *wrapper*), one “test cell” attached to each pin
- ▶ These test cells provide a way to capture/update data
- ▶ All test cells are “daisy chained” (think a single big shift register)
- ▶ We essentially need a serial data i/p pin and an o/p pin to shift-in and shift-out bits from all the pins
- ▶ The *wrapper* lies dormant (invisible) during normal operation

- ▶ JTAG, the IEEE 1149.1 standard, was formalized
- ▶ Also called the *boundary scan standard*
- ▶ A standardized way to do *boundary scan*

- ▶ Originally that was its purpose, but it turned out to be much more versatile!
- ▶ Not just single chips, any number of chips can be debugged in a board (again, daisy chained)
- ▶ And not just the “boundary”, internal system logic can also be debugged
- ▶ Further, can also be used for programming chips! (like FPGAs)

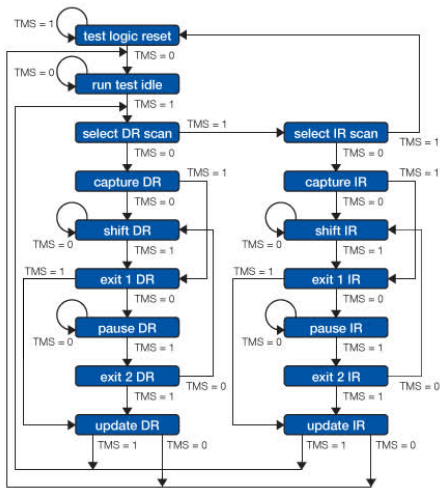


The JTAG port or Test Access Port (TAP) requires only 5 pins:

- ▶ TDI: Test Data Input (Serial Data in)
- ▶ TDO: Test Data Output (Serial Data out)
- ▶ TCK: Test Clock
- ▶ TMS: Test Mode Select (Change states in JTAG state machine)
- ▶ TRST: Test Reset (Optional, to reset JTAG state machine)

- ▶ Standard specifies one Instruction Register (IR) and various Data Registers (DR) to select from
- ▶ Mandatory Data registers:
 - ▶ Boundary Scan Register (BSR) - the *wrapper*
 - ▶ Bypass Register (BYPASS) - one bit register
- ▶ Optional Data Registers:
 - ▶ Device ID Register (IDCODE)
 - ▶ Various Device specific registers
- ▶ The register which is selected will shift-in bits from TDI and shift-out bits from TDO

- ▶ Contains the *JTAG/TAP State Machine*
- ▶ Also the Instruction Register and Instruction Decoder
- ▶ According to the current state in the state machine, one of the data register or instruction register will be selected/scanned/captured/updated
- ▶ Which data register is selected will depend on the instruction passed



- ▶ Mandatory instructions:
 - ▶ BYPASS (111...) - Use BYPASS Register (Passthrough)
 - ▶ EXTEST (000...) - Use BSR (Capture-DR -i Shift-DR -i Update-DR)
 - ▶ SAMPLE/PRELOAD - Use BSR (when device in normal mode)
- ▶ Optional instructions:
 - ▶ IDCODE - Use IDCODE register
 - ▶ INTEST - Use BSR (test internal core-logic)
 - ▶ Various other design specific instructions

- ▶ Boundary Scan Description Language (BSDL) is a subset of VHDL
- ▶ A BSDL file is needed for each JTAG enabled chip
- ▶ Contains all implementation details, like size of registers, number of registers, associated pins etc.
- ▶ A JTAG Debugger software can read this file to understand how to communicate with the device through JTAG