Cluster Innovation Centre, University of Delhi, Delhi-110007

Examination : **End Semester Examination – 2021**
Name of the Course : **B.Tech (Information Technology and Mathematical Innovations)**
Name of the Paper : **(Understanding Computing Systems Architecture)**
Paper Code : **32861104**
Semester : **I**
Duration : **3 Hours**
Maximum Marks : **75**
Instructions:
This question paper contains six questions, out of which any four are to be attempted. Each question carries equal marks.

---

1. Simplify the function f (a,b,c,d)= ∑ (1,3,5,13) with don't care conditions d (a,b,c)= ∑ (5,7,9,14) and design the truth table and a logic circuit for the simplified expression.

2. Given two binary numbers X=1001100 and Y= 10110011, perform the subtraction Y-X using 2's complement. Order the numbers $(1.011)_2$, $(1.12)_{10}$, $(110110)_{16}$, $(BCBB)_{16}$, $(58)_5$, $(34)_7$ and $(0.5)_{16}$ from smallest to largest. How many flip-flops will be complemented in a 10-bit binary counter to reach the next count after 1011101111?

3. Design a simplified traffic-light controller that switches traffic lights on a crossing where a north-south (NS) street intersects an east-west (EW) street. The input to the controller is the WALK button pushed by pedestrians who want to cross the street. The outputs are two signals NS and EW that control the traffic lights in NS and EW directions. When NS or EW are 0, the red light is on and when they are 1, the green light is on. When there are no pedestrians, NS=0 and EW=1 for 1 minute, followed by NS=1 and EW=0 for 1 minute and so on. When a WALK button is pushed, NS and EW both come 1 for a minute when the present minute expires. After that the NS and EW signals continue alternating. For the traffic-light controller:

Develop a state diagram and state/output table. Minimize the number of states. Encode the states. Draw a schematic diagram using JK flip flops

4. Explain the importance of different addressing modes in computer architecture with suitable examples. An instruction is stored at location 800 with its address field at location 801. The address field has the value 810. A processor register R1 contains the number 118. Evaluate the effective address if the addressing mode of the instruction is (i) Direct (ii) Immediate (iii) Relative (iv) Register indirect (v) Index with R1 as the index register.

5. A memory has a capacity of 16 K × 8. How many data input and data output lines does it have? How many address lines does it have? And a digital computer has a

common bus system for 16 registers of 64 bits each. The bus is constructed with multiplexers. How many selection inputs are there in each multiplexer? What sizes of multiplexers are needed? How many multiplexers are there in the bus?

6. How Call and Return instructions for a subroutine are handled in a computer? What are the various sets of micro-operations that will be performed in the common fetch cycle of 32 bits instruction size for both direct and indirect addressing mode ? Assume a suitable set of available registers.