Cluster Innovation Centre, University of Delhi, Delhi-110007

Examination	**: Semester Examination – March 2022**
Name of the Course	**: B.Tech (Information Technology and Mathematical Innovations)**
Name of the Paper	**: Understanding Computing Systems Architecture**
Paper Code	**: 32861104**
Semester	**: I**
Duration	**: 3 Hours**
Maximum Marks	**: 75**

Instructions:

This question paper contains six questions, out of which any four are to be attempted. Each question carries equal marks.

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1. Simplify the function f(a,b,c,d)= ∑ (1,2,3,10,14), Don't care conditions D(a,b,c,d)= ∑ (0,5,11,12) and design a logic circuit for the simplified expression into POS and SOP both the forms.

2. A sequential circuit has two JK flip-flops, A and B; two inputs, x and y; and one output, z. The flip-flop input functions and the circuit output function are as follows:

$J_A = Bx + B'y'$ $K_A = B'x'y'$ $J_B = A'x$

$K_B = A + xy'$ $z = Axy + Bx'y'$

Draw the logic diag. of the circuit
Tabulate the state table
Derive the next state equations for A and B.

3. Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. When the binary input is 0, 2, 4, or 6, the binary output is one greater than the input. When the binary input is 1, 3, 5, or 7, the binary output is one less than the input. Also design 3 input NAND gate using minimum numbers of 2 input NAND Gates.

4. Differentiate Hardwired control unit Vs Micro-programmed control unit. What is a multiplexer ? Explain how a 16 x 1 multiplexer can be designed using two 4 x 1 multiplexers.

5. What are the differences between circular and logical shift micro-operations? Explain the fetch cycle and execute cycle for an additional instruction. What are the various micro-operations that will be performed in sequence to fetch an instruction from the memory to an Instruction Register (IR)? Assume a suitable set of available registers.

6. An instruction is stored at location 400 with its address field at location 401. The address field has the value 700. A processor register R1 contains the number 120. Evaluate the effective address if the addressing mode of the instruction is (i). Direct (ii). Immediate (iii). Relative (iv). Register indirect (v). Index with R1 as the index register