Hacettepe University

Computer Engineering Department

BM233 Logic Design Lab - 2021 Fall

Verilog Assignment 1

December 5, 2021

Student name:
Metin Eren Oktay

Student Number:
2210356137

1 Problem Definition

We are required to create a combinational circuit using a 2x4 decoder and a 4x1 MUX in Verilog to learn basics of Verilog and Vivado.

2 Verilog Code Solutions

2.1 Decoder 2x4

```
module decoder_2x4(
    input[1:0] A,
    output[3:0] D
    );
    assign D[3] = (A[0]) && (A[1]);
    assign D[2] = (!(A[0])) && (A[1]);
    assign D[1] = (A[0]) && (!(A[1]));
    assign D[0] = (!(A[0])) && (!(A[1]));
endmodule
```

2.2 Mux 4x1

```
module mux_4x1(
    input[3:0] i,
    input[1:0] s,
    output F
);
    wire s1neg, s0neg, T1, T2, T3, T4;

    not (s0neg, s[0]), (s1neg, s[1]);
    and (T1, i[0], s0neg, s1neg);
    and (T2, i[1], s0neg, s1);
    and (T3, i[2], s0, s1neg);
    and (T4, i[3], s0, s1);
    or(F, T1, T2, T3, T4);
endmodule
```

3 Testbench Waveforms

3.1 Decoder 2x4 TB

```
module decoder_2x4_tb;
    reg [1:0] A;
    wire [3:0] D;
    decoder_2x4 UUT(.A(A), .D(D));
    initial begin
        A[1] = 1'b0; A[0] = 1'b0;
        #10 A[1] = 1'b0; A[0] = 1'b0;
        #10 A[1] = 1'b0; A[0] = 1'b1;
        #10 A[1] = 1'b1; A[0] = 1'b0;
        #10 A[1] = 1'b1; A[0] = 1'b1;
        #10 $finish;
    end
endmodule
```

3.2 MUX 4x1 TB

```
module mux_4x1_tb;
    reg [3:0] i;
    reg [1:0] s;
    wire F;
    mux_4x1 UUT(.i(i), .s(s), .F(F));
    initial begin
        s[1]=1'b0; s[0]=1'b0; i[3]=1'b0; i[2]=1'b0; i[1]=1'b0; i[0]=1'b0;
        #10 s[1]=1'b0; s[0]=1'b0; i[3]=1'b0; i[2]=1'b0; i[1]=1'b0; i[0]=1'b1;
        #10 s[1]=1'b0; s[0]=1'b0; i[3]=1'b1; i[2]=1'b1; i[1]=1'b1; i[0]=1'b0;
        #10 s[1]=1'b0; s[0]=1'b0; i[3]=1'b0; i[2]=1'b0; i[1]=1'b1; i[0]=1'b0;
        #10 s[1]=1'b0; s[0]=1'b0; i[3]=1'b1; i[2]=1'b1; i[1]=1'b0; i[0]=1'b1;
        #10 s[1]=1'b0; s[0]=1'b0; i[3]=1'b0; i[2]=1'b1; i[1]=1'b0; i[0]=1'b0;
        #10 s[1]=1'b0; s[0]=1'b0; i[3]=1'b1; i[2]=1'b0; i[1]=1'b1; i[0]=1'b1;
        #10 s[1]=1'b0; s[0]=1'b0; i[3]=1'b1; i[2]=1'b0; i[1]=1'b0; i[0]=1'b0;
        #10 s[1]=1'b0; s[0]=1'b0; i[3]=1'b0; i[2]=1'b1; i[1]=1'b1; i[0]=1'b1;
        #10 $finish;
    end
endmodule
```

References

- My reference