EE 143: Microfabrication Technology

Lab Report 2 (Spring 2023)

Due Date: 11:59pm Friday, May 5, 2023 on bCourses

Report Specifications

- This report should be written in the form of a research paper, meaning complete sentences and paragraphs (or tables of information).
- Each group should create a single report together.
    - You may NOT consult anyone outside your group, with the exception of EE 143 GSIs.
- Each group should attach the academic honesty form and have all members sign it.
    - It is ok if different members sign on a separate copy. Attach all signed copies of the form to the paper copy of the report.
- Submit 1 pdf electronic copy per group on bCourses.
    - Files will be checked for plagiarism against each other and lab reports from previous semesters.

Report Outline

Your paper should follow the outline given below. Please clearly indicate the beginning of each major section of your report with appropriate formatting.

EE 143 Lab Report 2 Academic Honesty Form

Spring 2023

In signing below, I attest to the fact that I have read and have adhered to the policies and guidelines discussed in the EECS Departmental Policy on Academic Dishonesty, as found at: https://eecs.berkeley.edu/resources/students/academic-dishonesty

Group Member:_____

Signature:_____

Date:_____

Group Member:_____

Signature:_____

Date:_____

Group Member:_____

Signature:_____

Date:_____

Title Page

Include course name and number, semester, lab section and group number, member names, lab GSI's name, and professor's name.

Contributions

In this section, you should list how each member contributed to each section of the report. Each group member should have at least some contribution to every section.

Summary/Abstract (1 paragraph) [5 points]

Summarize the main results of device characterization. What was the purpose of characterization? What did you measure? What worked, and what didn't?

Devices & Procedures [10 points]

For each device type listed in the following Measured Data section of this report, please provide the following:

1. A top-down schematic of the device labeling layers and important dimensions. You may choose to use the drawings in the chip layout folder on bCourses, though these may need additional labels added.
2. A brief description of the device structure explaining how it is constructed from its layers, and its intended purpose and method of operation.
3. A brief description of the probe/stimulus setup and what measurements were taken at each of the contact pads, noting different arrangements if multiple measurements were performed on one device (i.e., for MOSFET Id-Vd and Id-Vg).

MOSFETs 8a-d, 9a-c, and 10 can be combined into one diagram and description. All other devices should have their own diagram and description.

Measured Data [40 points]

For each of the devices below, plot the requested results of your measurements of the device. Every graph should have meaningful axis labels and units. If there were issues with a particular device or irregularities in the graph, please plot whatever data you do have. For all graphs, briefly describe what you expected, what worked or not, and possible explanations for any problems.

- 4-Point Resistors (2a and 2b)
  - I vs ΔV, where ΔV is the difference between your measured voltages
- Contact-chain resistors (2c and 2d)
  - I vs V
- MOS Capacitors (3, 4, 5)
  - C vs V (for the gate oxide capacitor, provide graphs with light on and off)

- Diode (7)
    - I vs V curve in forward bias
    - I vs V curve showing breakdown in reverse bias
- MOSFETs of varying length (8a, 8b, 8c, 8d)
    - Id vs Vd, varying Vg
    - Id vs Vg, varying Vb
    - Log(Id) vs Vg, varying Vb
- MOSFETs of varying width (9a, 9b, 9c)
    - Id vs Vd, varying Vg
    - Id vs Vg, varying Vb
    - Log(Id) vs Vg, varying Vb
- Other MOSFETs (10, 11)
    - Id vs Vd, varying Vg
    - Id vs Vg, varying Vb
    - Log(Id) vs Vg, varying Vb
- Inverter
    - Vout vs Vin, varying Vdd

Data Analysis and Calculations [40 points]

Using data from the previous section and from Lab Report 1 as need be, make the following calculations for each device.

- 4-Point Resistors (2a and 2b)
    - Extract a resistance value for each structure from your IV-curve.
    - Using the ideal dimensions from the device layout, as well as overetch, junction depth, and polysilicon thickness values from Lab Report 1, what are the dimensions of the measured resistive areas?
    - Using the previous values, what is the bulk resistivity of the active area and polysilicon?
    - Using the previous value, what are the dopant densities in the active area and polysilicon? Comment on how this compares to what you might expect from Lab Report 1.
- Contact-chain resistors (2c and 2d)
    - Extract a resistance value for each structure from your IV-curve.
    - For each structure, compute the resistance of a single contact.
        - Use your previously computed values for active area and polysilicon resistivity, as well as metal sheet resistance from Lab Report 1.
        - You can assume the resistance of the probes is negligible.
- MOS Capacitors (3, 4, 5)
    - Extract a single capacitance value from each C-V plot.
    - Using the known geometry of the capacitors, and the oxide thicknesses from Lab Report 1, compute the expected capacitance of each capacitor. How close was this to the measured value?
    - For the gate oxide capacitor, extract a threshold voltage from the C-V plot. This is another way of measuring the transistor threshold voltage.
- Diode (7)
    - Extract the turn-on voltage from the I-V curve.
    - Extract the breakdown voltage from the I-V curve.

- MOSFETs (8a-8d, 9a-9c, 10, 11)
    - Extract the on current, Ion, from the Log(Id)-Vg plot. Ion is the current through the transistor at maximum Vg with Vb=0.
    - Extract the off current, Ioff, from the Log(Id)-Vg plot. Ioff is the current through the transistor with Vg=0 and Vb=0.
    - Compute the on/off ratio, Ion/Ioff. This is a common figure of merit.
    - Extract the threshold voltage, Vt, from the Id-Vg plot.

Conclusion (1 paragraph) [5 points]

Briefly summarize what lessons could come out of the work you did in the lab. What did you learn about device characterization? What are some of the most critical factors to pay attention to? Knowing how to characterize devices, could you make any improvements to the fabrication process?

Appendix (as needed)

References (as needed)

If you use any outside references to support your explanations or calculations, please cite your sources and include a list of references here.