CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 2

Project Teams Group #: _SecB_02_____

Team Members: ___Eli von Nordheim_____

___Sam Forde_____

___Kaden Berger_____

___Joseph Metzen_____

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Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members. Examples may include:*

- *learn everything about computer architecture*
- *know enough to understand security risks posed by hardware primitives*
- *get an A/B/C/Pass in the course*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *prepare myself to be able to do research involving FPGAs*
- *be able to explain the workings of a stored-program computer from gates to C*

Team Expectations:

- **Conduct:** *What are the expectations for personal conduct of group members?*
  Work is expected to be completed in a timely manner or any obstacles quickly communicated
- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*
  Most communication will happen over text, responses should be within an hour during reasonable time with exception for extraneous circumstances and unavailable hours. Unavailable hours should be communicated.

- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*

  Files should be named using underscores in place of spaces, all lowercase. Testbenches should begin with tb_, test benches should exhaust at minimum a few typical cases as well as target edge cases. For version control, GitHub will be used. Comments should be thorough at the level of functional components of the code (entity, process, etc.) and by line in difficult to read snippets.
- **Meetings:** *Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person). Examples of other issues to consider include:*
  - Monday: 10:00-12:00PM
  - Friday: 10:00-12:00PM
  - *Focus on integration during in-person meeting time, work separately as time permits.*
- **Peer Evaluation Criteria:** *Now that you have experience working on a 381 lab with a team, please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.*
  - Timeline adhesion
  - Communication effectiveness
  - Debugging contribution/code quality
  - Lab attendance

Role Responsibilities: *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

Lab Part		Estimated Time	Design		Test	
			Lead	Deadline	Lead	Deadline
Software-Scheduled Pipeline	Control Signals	0.5 hr	Joseph	11/8/24	Eli	11/8/24
	Datapath	3 hr	Eli	11/8/24	Sam	11/8/24
	Testing	3 hr	Kaden	11/11/24	Sam	11/11/24
	Synthesis (human effort)	0.5 hr	Sam	11/11/24	Eli	11/11/24
Hardwa	Pipeline Register Update	1 hr	Joseph	11/18/24	Kaden	11/18/24

Data Hazard Avoidance	4 hr	Joseph	11/19/24	Sam	11/19/24
Control Hazard Avoidance	2-6 hr based on group size	Eli	11/19/24	Sam	11/19/24
Integration (Hardware-Schedule Pipeline)	3 hr	Sam	11/19/24	Kaden	11/19/24
Testing	3 hr	Kaden	11/19/24	Joseph	11/19/24
Synthesis	0.5 hr	Eli	11/21/24	Joseph	11/21/24

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Please note that to be done properly, the test programs will require significant time investment, but will result in a much stronger final design.*

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature ___Eli von Nordheim_____ **Date** _10/30/2024____

Student Signature ___Sam Forde_____ **Date** 10/30/2024_

Student Signature ___Kaden Berger_____ **Date** 10/30/24____

Student Signature __Joseph Metzen_____ **Date** _10/30/24____

Student Signature _____ **Date** _____

Student Signature _____ **Date** _____