Introduction to the RISC-V Instruction Set Architecture

Alejandro Rusi

GsoC

RISC-V

Figure 1: Risc-V Logo

RISC-V is an open standard instruction set architecture (ISA) based on established reduced instruction set computer (RISC) principles. Unlike most other ISA designs, the RISC-V ISA is provided under open source licenses that do not require fees to use. RISC-V is:

- Open Standard and Open Source
- Modular
- Extendible

Format

32-bit RISC-V instruction formats

Format	Bit																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register/register	funct7							rs2					rs1					funct3			rd					opcode					
Immediate	imm[11:0]												rs1					funct3			rd					opcode					
Upper immediate	imm[31:12]																				rd					opcode					
Store	imm[11:5]							rs2					rs1					funct3			imm[4:0]					opcode					
Branch	[12]	imm[10:5]						rs2					rs1					funct3			imm[4:1]				[11]	opcode					
Jump	[20]	imm[10:1]										[11]	imm[19:12]								rd					opcode					

- **opcode (7 bits):** Partially specifies which of the 6 types of *instruction formats*.
- **funct7, and funct3 (10 bits):** These two fields, further than the *opcode* field, specify the operation to be performed.
- **rs1 (5 bits):** Specifies, by index, the register containing first operand (i.e., source register).
- **rs2 (5 bits):** Specifies the second operand register.
- **rd (5 bits):** Specifies the destination register to which the computation result will be directed.

Figure 2: ISA Format

Extensions

Multiplication and Division

Allows for the usage of **multiplication** and **division** operations.
Assumes that there are registers with 64-bits.

Atomic Instructions

Consistent access to memory.

Bit Manipulation

Still unapproved, but will aid support for common cryptographic, graphic and mathematical bit operations.