ECE-111 Advanced Digital Design Project

Homework-1:

Synthesize 2to1 Multiplexer (MUX) SystemVerilog

- Read and understand 2to1 MUX systemverilog behavioral level, dataflow level and gatelevel code provided in Labs1.zip folder.
- Synthesize each of these representations of 2to1 MUX using Altera Quartus Prime
- Using Netlist viewer in Quartus Altera review RTL Viewer and Post technology mapping and fitting schematics.
- Review Resource Usage Summary table under Analyze and Synthesis and see how many ALUT (Adaptive Look Up Tables are utilized and number of inputs to ALUT used to implement Boolean function)
- Simulate using Modelsim-Altera and mux testbench provided. Review MUX waveform to confirm the behavior of multiplexer.
- Review resource usage summary and simulation waveform of all three implementations of MUX (gate level, dataflow and behavioral)
- Same mux_2x1_testbench.sv provided in Lab1.zip folder can be used to simulate mux_2x1_gate.sv, mux_2x1_dataflow.sv and mux_2x1_behavioral.sv implementations.

Lab1.zip folder has mux, decoder and fulladder systemverilog code and testbench files which is made available on ECE-111 class canvas webpage.

Repeat above mentioned steps for decoder and fulladder SystemVerilog code which is provided in Lab1.zip folder.

Homework Report Submission Requirements :

Submit report to gradescope using canvas in pdf format which should include following mentioned :

- For all three (behavioral, dataflow, gatelevel) representation of Mux, decoder and fulladder provide snapshot of RTL and post-mapping schematics generated from Altera Quartus Prime.
- Provide number ALUT's used, number of Boolean functions used for each design including number of input pins to ALUT used. Explain why 2 or 3 or N number ALUT's are used, why 2 or 3 or N number of Boolean functions implemented and why 2 or 3 or N number inputs to ALUT.
- Provide snapshot of simulation waveform generated from Modelsim, explaining decoder, mux and fulladder behavior.
  Note : For each design (MUX, decoder, FullAdder) only one waveform snapshot is sufficient since gate level / behavioral and dataflow models of each design has same functional behavior.