

Project Navigator

Files

Files

abc

../ECE284FA25Project/Part1/verilog/SFP/sfp.v

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../ECE284FA25Project/Part1/verilog/MAC_PE/mac_tile.v

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../ECE284FA25Project/Part1/verilog/MAC_PE/mac_array.v

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../ECE284FA25Project/Part1/verilog/MAC_PE/mac.v

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../ECE284FA25Project/Part1/verilog/L0/I0.v

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../ECE284FA25Project/Part1/verilog/FIFO/ofifo.v

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../ECE284FA25Project/Part1/verilog/FIFO/fifo_mux_16_1.v

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../ECE284FA25Project/Part1/verilog/FIFO/fifo_mux_8_1.v

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../ECE284FA25Project/Part1/verilog/FIFO/fifo_mux_2_1.v

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../ECE284FA25Project/Part1/verilog/FIFO/fifo_depth64.v

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../ECE284FA25Project/Part1/verilog/FIFO/fifo_depth8.v

abc

../ECE284FA25Project/Part1/verilog/corelet.v

Analysis & Synthesis Summary

<<Filter>>

Analysis & Synthesis Status	Successful - Tue Dec 2 14:03:3
Quartus Prime Version	25.1std.0 Build 1129 10/21/202
Revision Name	corelet
Top-level Entity Name	corelet
Family	Cyclone IV GX
Total logic elements	194
Total registers	129
Total pins	227
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0
Total GXB Receiver Channel PMA	0
Total GXB Transmitter Channel PCS	0
Total GXB Transmitter Channel PMA	0
Total PLLs	0

Flow Summary	
<<Filter>>	
Flow Status	Successful - Tue Dec 2 14:11:5
Quartus Prime Version	25.1std.0 Build 1129 10/21/202
Revision Name	corelet
Top-level Entity Name	corelet
Family	Cyclone IV GX
Device	EP4CGX150DF31I7AD
Timing Models	Final
Total logic elements	194 / 149,760 (< 1 %)
Total registers	129
Total pins	227 / 508 (45 %)
Total virtual pins	0
Total memory bits	0 / 6,635,520 (0 %)
Embedded Multiplier 9-bit elements	0 / 720 (0 %)
Total GXB Receiver Channel PCS	0 / 8 (0 %)
Total GXB Receiver Channel PMA	0 / 8 (0 %)
Total GXB Transmitter Channel PCS	0 / 8 (0 %)
Total GXB Transmitter Channel PMA	0 / 8 (0 %)
Total PLLs	0 / 8 (0 %)

Power Analyzer Summary	
<<Filter>>	
Power Analyzer Status	Successful - Tue Dec 2 14
Quartus Prime Version	25.1std.0 Build 1129 10/2
Revision Name	corelet
Top-level Entity Name	corelet
Family	Cyclone IV GX
Device	EP4CGX150DF31I7AD
Power Models	Final
Total Thermal Power Dissipation	189.26 mW
Core Dynamic Thermal Power Dissipation	2.30 mW
Core Static Thermal Power Dissipation	118.81 mW
I/O Thermal Power Dissipation	68.14 mW
Power Estimation Confidence	Low: user provided insuffi

Slow 1200mV 100C Model Fmax Summary			
<<Filter>>			
	Fmax	Restricted Fmax	Clock Name
1	281.21 MHz	250.0 MHz	clk

Analysis & Synthesis Resource Usage Summa		
<<Filter>>		
	Resource	Usage
1	I/O pins	227
2		
3	DSP block 9-bit elements	0
4		
5	Maximum fan-out node	reset~input
6	Maximum fan-out	137
7	Total fan-out	1166
8	Average fan-out	1.52