A Multistep Charge Extractions and Voltage Bias-Flip (MCEBF) Interface Circuit for Piezoelectric Energy Harvesting Enhancement

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***Abstract*— In piezoelectric energy harvesting (PEH), interface circuits using synchronous switch actions, including synchronized charge extraction (CE) and/or bias-flip (BF), can achieve much higher energy harvesting (EH) capability, compared with the standard energy harvesting (SEH) bridge rectifier. In this article, a multistep charge extraction and voltage bias-flip (MCEBF) interface circuit is proposed to further enhance the harvesting capability under weakly coupling conditions. The EH enhancement is realized by reducing the dissipation in CE with multiple CE actions and simultaneously enlarging the extracted energy with a BF action. MCEBF can also generate positive and negative voltage rails via buck-boost topology to supply power for double-rail devices. The optimal control method of MCEBF is theoretically derived. In our experiment, under constant deflection excitation, the best MCEBF case offers 487%, 95%, and 49% more harvested power, compared with SEH, synchronous electric charge extraction (SECE), and parallel synchronized switch harvesting on inductor (P-SSHI) interface circuits, respectively. MCEBF also keeps the benefit of load independence as SECE does under weakly coupling conditions.**

***Index Terms*— Kinetic energy harvesting, multistep interface circuit, piezoelectric devices.**

I. Introduction

THE emergence of more Internet of Things (IoT) devices beckons for low-power electronics and long-lasting power supply solutions. Energy harvesting (EH) technologies scavenge electrical energy from the ambiance in the forms of vibration, light, thermal, and so on [2]. Given the continuous reduction of IoT power consumption, they have gradually shown strong feasibility and potential for offering energy-self-sufficient solutions to distributed and portable electronics. More IoT devices might be self-powered or battery-free in the future, with the advancement of EH technologies.

The main challenge of vibration energy harvesting (VEH) is how to extract more mechanical vibration power into electrical form. A piezoelectric transducer is one of the most promising candidates for efficient VEH [3]. In the last two decades, researchers in mechanical engineering, material science, and electrical engineering have taken great efforts to improve the structure design, materials, and power conditioning circuits toward piezoelectric energy harvesting (PEH) enhancement. Piezoelectric transducers can convert the power associated with mechanical vibration into electric alternative current (ac) power. The ac output from a piezoelectric transducer cannot be directly used to power digital electronics. Thus, we need an interface circuit to convert the ac voltage output into a direct current (dc) voltage. The original and simplest PEH interface circuits have no active switch action. A simple full-bridge rectifier (FBR) is regarded as the benchmark standard energy harvesting (SEH) interface circuit [4], [5]. When the output voltage of a piezoelectric element is low, the voltage doubler (VD), as an SEH derivative, performs better [6], [7].

Later literature has shown that, under weakly coupling conditions, the harvested power can be increased by synchronously incorporating active switch actions. Based on such an idea, many synchronized switch solutions were developed. The most extensively studied cases are synchronized switch harvesting on inductor (SSHI) [8]–[10] and synchronous electric charge extraction (SECE) [11]–[13]. SSHI uses the bias-flip (BF) switch action to flip the voltage across the piezoelectric capacitor at each piezoelectric voltage peak. BF action can pre-bias the piezoelectric voltage for the next half-cycle to increase the voltage magnitude. SSHI can significantly enhance the EH capability compared with SEH. As for SECE, a switching action extracts all the electric charge from the piezoelectric capacitor to a storage capacitor. An inductor acts as the energy conveyor. SECE can isolate the load from the piezoelectric element, which means the operation point of the piezoelectric transducer is constant. In a weakly coupled PEH system, when using SECE, the harvested power is reluctant to load variation. Theoretically, under weakly coupling

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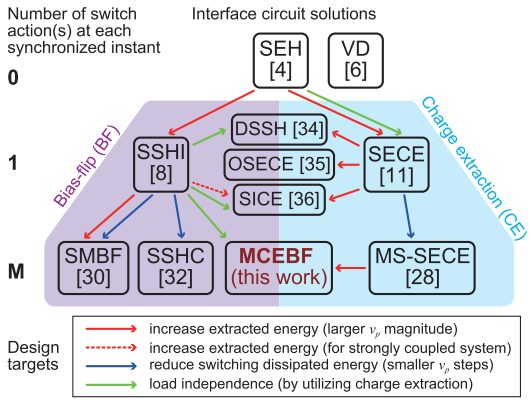


Fig. 1. Brief summary of the PEH interface circuits based on synchronized BF and/or charge-extraction (CE) actions for enhancement of harvesting capability.

conditions, SECE can give four times the output power compared with SEH. SECE and SSHI were also implemented on integrated circuit (IC) platforms for smaller size and higher power conversion efficiency [14], [15]. Some array interface circuits were also proposed to harvest energy from multiple piezoelectric transducers [16]–[18]. Besides the conventional SSHI and SECE, which take only one BF or CE action, respectively, at each synchronized instant, some following designs have been invented by combining the two kinds of switch actions.

Fig. 1 summarizes some typical designs utilizing the BF and CE synchronized switch actions. They are categorized based on the action type and the number of switch actions at each synchronized instant. It must be mentioned that Fig. 1 does not cover all interface circuits invented for PEH improvement. It only briefs the typical and most related cases toward harvesting capability enhancement. Harvesting capability can be quantified as the maximum harvested power ratio of a specific interface circuit with respect to SEH under zero backward (electrical to mechanical) coupling condition [19]. It is a pure circuit characteristic and irrelevant to the piezoelectric coupling condition. Recently, there are some interface circuit technologies derived from the conventional SSHI [20], [21] or SECE [22]–[26] for improving the off-resonance performance. These circuits require a relatively strong coupling condition to take effect. The off-resonance tuning issue is out of the focus of this article. Some review articles can refer to more rationale about those designs [27].

The SSHI and SECE designs have shown large enhancement compared with the benchmark SEH topology. On the other hand, the inductor current with a single switch action is usually high. Considerable energy might be dissipated on the equivalent series resistance (ESR) of the inductor and connecting wires. High current may also cause inductor saturation and further degrade the performance. To reduce such dissipation, multi-shot technology was developed. It divides the instantaneous voltage jump into several small steps. The circuit takes a BF or CE action with a smaller voltage change in each step. The multi-shot technology helps reduce energy dissipation by decreasing the peak inductor current. The multi-shot SECE (MS-SECE or MCE) [28], [29] can harvest up to 25% more energy compared with SECE. Multi-shot SSHI interface circuits realized with discrete devices [30] and integrated designs [31] have been introduced in recent years. Multi-shot SSHI can also be reconfigured into inductor-free designs [32], [33].

Besides multi-shot technologies, the combination of SSHI and SECE provides another possibility to improve the performance of the PEH interface circuit. Some hybrid solutions have been proposed, for example, the double synchronized switch harvesting (DSSH) circuit [34] and optimized synchronous electric charge extraction (OSECE) circuit [35]. The switch actions in DSSH and OSECE extract charges from the piezoelectric capacitor and pre-bias the piezoelectric voltage to some extent at the same time. The energy ratio of CE and BF is defined by the output voltage in OSECE and the device parameter in DSSH. Such a ratio cannot be tuned flexibly. The synchronous inversion and charge extraction (SICE) [36], [37] is another hybrid solution. SICE performs an interlaced combination of CE and BF actions. Some schemes also use BF actions to inverse the residual voltage after CEs [38]. The inductor in the SICE circuit operates in either the CE or BF mode at different synchronized voltage peaks.

The harvested power is the difference between the extracted power and dissipated power [39]. We can evaluate a PEH interface from three aspects as follows.

1) How much it can increase the energy extraction from the mechanical domain?
2) How much it can reduce the energy dissipation in power conditioning?
3) Whether it is load-independent or not?

For these purposes, a new interface circuit called multistep charge extractions and voltage bias-flip (MCEBF) is proposed in this article.

The following chapters are organized as follows. Section II reviews the technology of SECE and MCE. Section III discusses the circuit topology and operation phases of MCEBF. Section IV demonstrates the optimal control and its derivation. Section V studies the energy flow of the proposed MCEBF circuit. Section VI presents the experiments for optimal control and performance evaluation. Section VII concludes this article.

II. SECE and MCE Technologies

SECE and MCE technologies have set some fundamentals for the proposed MCEBF design. Fig. 2(a) shows the typical topology of SECE [11]. $i_{\rm eq}$ and C_p represent a piezoelectric transducer's equivalent current source and parallel capacitor, respectively. These two elements model the dynamics of a piezoelectric structure under weakly coupling conditions. Compared with the SEH interface circuit, SECE can enhance the harvested power to four-folds under the same vibration. Moreover, the harvested power of SECE is independent of the loading condition [11]. Such a feature gives more convenience to the following stage circuit design.

Fig. 2(b) and (c) shows the working waveform of SECE. In most of the vibration period, the piezoelectric element is in open-circuit (OC) condition [specified as OC phase

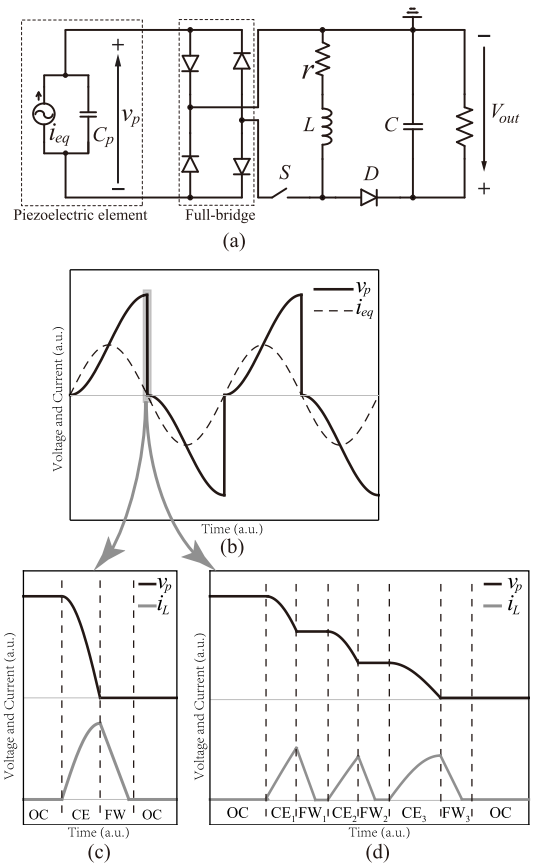


Fig. 2. Topology and waveform of SECE and MCE interface circuits. (a) Circuit topology. (b) Piezoelectric voltage and equivalent current waveform. (c) Enlarged view of a synchronized switch instant in SECE. (d) Enlarged view of a synchronized switch instant in 3CE.

in Fig. 2(c)]. The switch and diode are off during the OC phase, and the voltage across the piezoelectric plate rises until it reaches $2V_{\rm oc}$. $V_{\rm oc}$ is the nominal OC voltage of the piezoelectric element

$$V_{\rm oc} = \frac{I_{\rm eq}}{\omega C_p} \tag{1}$$

where $I_{\rm eq}$ is the magnitude of internal current source $i_{\rm eq}$ and ω is the vibration frequency. When the piezoelectric beam reaches its displacement extremes, the switch turns on. The circuit enters the CE phase. Piezoelectric capacitor C_p and the inductor L form an LC loop. A transient series oscillation happens through C_p and L. In conventional SECE, the CE phase lasts for a quarter of an LC cycle, that is, $\pi\sqrt{LC_p}/2$. After the CE phase, the voltage across the piezoelectric plate drops to zero, while the inductor current reaches its maximum value. As the switch turns off, the inductor current flows through the freewheeling (FW) diode. The circuit enters the FW phase and charges the output capacitor C. After the depletion of the inductor current, the FW diode is reversely shut down. The circuit returns to OC condition. In the switching and FW phases, ESR of the LC loop dissipates some energy, which is summarized by r in Fig. 2(a). r includes the series resistance of the piezoelectric element, inductor, and connecting wires. As a result, the ESR of the LC loop plays a non-negligible role in the efficiency improvement of the SECE interface circuit. The energy dissipation can be expressed as follows [40]:

$$E_{d,\rm switch} = 2(\gamma + 1)C_p V_{\rm oc}^2 \tag{2}$$

where γ is called the inversion factor or flipping factor in the SSHI studies [41]. γ is formulated as follows:

$$\gamma = -e^{-\frac{\pi}{2Q}} \tag{3}$$

and Q is the quality factor of the r-L-C_p loop

$$Q = \frac{1}{r}\sqrt{\frac{L}{C_p}}. \tag{4}$$

Given the same quality factor of r-L-C_p loop, the multi-shot charge extraction (MCE) technology [28], [29] can be applied to reduce the dissipation on ESR, so as to harvest more energy from the piezoelectric element. It can improve the harvesting capability by up to 25% according to [28]. MCE can be implemented on the same circuit configuration of SECE by modifying the switch control. It splits the CE and FW phases into multiple pairs. The voltage outer profile in MCE looks the same as that in the SECE circuit, except for the moments around the synchronized instants. Fig. 2(d) shows the enlarged view of the piezoelectric voltage and inductor current around a synchronized switch instant in 3CE (MCE with three extracting actions). The piezoelectric voltage drops in a downstairs shape with the alternate CE and FW phases. In the last step, the switch turns on for the duration of $\pi\sqrt{LC_p}/2$. All residual energy is extracted by the inductor and then further transferred to the output capacitor. In MCE, the inductor peak current is suppressed; therefore, the energy dissipation in ESR is reduced as well. Since the total extracted energy of SECE and MCE is the same, given the same outer voltage profile, by reducing the energy dissipation in power conditioning, MCE can scavenge more energy in one cycle, compared with SECE.

III. Multistep Charge Extractions and Voltage Bias-Flip (MCEBF)

MCE can increase the harvested energy by reducing dissipation. However, there is no energy increase from the mechanical domain. The dilemma can be handled by adding a BF action after multiple CE actions at each voltage peak across C_p. Given this idea, we propose the MCEBF interface circuit, whose topology is shown in Fig. 3. MCEBF is based on the buck-boost topology, which can isolate the piezoelectric source from the load. It discusses an organic fusion of multi-shot, CE, and zero-bias series-SSHI, as well as the optimal control sequence and timing, toward higher EH capability. As mentioned above, the ESR r summarizes the parasitic resistance of the piezoelectric element, the inductor L, and the connecting wires. D_x and S_x $(x = 1, 2, 3, 4)$ are diodes and MOSFETs working as switches, respectively. $C_{\rm lp}$ and $C_{\rm ln}$ are the positive and negative storage capacitors, respectively. They provide both positive and negative voltage rails for applications, which needs double voltage rails.

In MCEBF, the inductor L has two functions. One is CE to extract energy from the piezoelectric capacitor as SECE

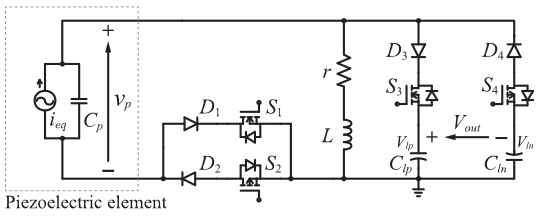


Fig. 3. Simplified schematic of the MCEBF circuit.

and MCE do. The other is BF to flip the residual charge after several rounds of extraction. The BF action is similar to that in SSHI.

A. Working Principle

Assuming the diodes are ideal and neglect the energy dissipation in FW phases, the operating principle of a half cycle in MCEBF can be analyzed as follows.

1) Open-Circuit (OC) Phase: In the OC phase, whose conducting branch and waveform are shown in Fig. 4(a)–(c), all switches turn off. The piezoelectric element is in the OC condition. Equivalent current in the piezoelectric element charges its internal capacitor C_p, until v_p rise for $2V_{\rm oc}$ and reach the voltage extremes.

2) Charge Extraction Phases ($CE_1, CE_2, \ldots, CE_M$): When v_p reaches its maximum or minimum value, the peak voltage triggers the peak detector. At the synchronized instant, as shown in Fig. 4(d)–(f), the piezoelectric capacitor C_p is shunted by the inductor L via MOSFET S_2 and diode D_2. As a result, the current through the inductor L rises according to the r-L-C_p transient response. The duration of each CE phase $T_{\rm CE}$ is set as a constant and satisfies $T_{\rm CE} \ll \pi\sqrt{LC_p}/2$. Since $T_{\rm CE}$ is much smaller than a quarter of an LC resonance period, the zero input response (ZIR) of the L-r-C_p can be simplified into the ZIR of an L-C_p loop. Thus, the peak of the inductor current in the mth CE phase can be formulated as follows:

$$I_m \approx V_{p,m-1}\sqrt{\frac{C_p}{L}}\sin\left(\frac{T_{\rm CE}}{\sqrt{LC_p}}\right) \approx T_{\rm CE}\frac{V_{p,m-1}}{L} \tag{5}$$

where $V_{p,m-1}$ is the voltage across C_p after the $(m-1)$th round of CE and FW phases. $V_{p,m-1}$ can be formulated as follows:

$$V_{p,m} = \left(1 - \frac{T_{\rm CE}^2}{2LC_p}\right)V_{p,m-1}. \tag{6}$$

Denoting the initial voltage as $V_{p,0}$, the expression of $V_{p,m}$ and I_m can be derived as follows:

$$V_{p,m} = V_{p,0}\left(1 - \frac{T_{\rm CE}^2}{2LC_p}\right)^m \tag{7}$$

$$I_m = \frac{T_{\rm CE}V_{p,0}}{L}\left(1 - \frac{T_{\rm CE}^2}{2LC_p}\right)^{m-1}. \tag{8}$$

3) Freewheeling Phases ($FW_1, FW_2, \ldots, FW_M$): In the FW phases, as shown in Fig. 4(g)–(i), switch S_2 turns off, and switch S_4 turns on. The energy stored in the inductor flows to the storage capacitor $C_{\rm ln}$, which generates a more negative output voltage. The storage capacitor is designed to be much larger than that of C_p. The slope of the inductor current drop can be regarded as a constant value. When the inductor current drops to zero, diode D_4 is reversely shut down. The FW process ends passively.

4) BF Phase: The BF phase is shown in Fig. 4(j)–(l). After M rounds of switching and FW phases, the residual charge in C_p is flipped by the inductor through a BF action. The end voltage of the flipping action $V_{p,m+1}$ can be expressed as follows:

$$V_{p,M+1} = \gamma\, V_{p,M}. \tag{9}$$

The flipping phase is a little longer than $\pi\sqrt{LC_p}$ to ensure that the BF action is complete. When the inductor current drops to zero, the branch is cut off by D_2.

After the falling edge BF, the circuit starts another half cycle. The operating principle is the same, while the inductor current is negative and generates a positive output voltage. At steady state, $V_{p,0}$ can be expressed as follows:

$$V_{p,0} = -V_{p,M+1} + 2V_{\rm oc} \tag{10}$$

by solving (7), (9), and (10), the initial voltage of each cycle $V_{p,0}$ can be obtained as follows:

$$V_{p,0} = \frac{2V_{\rm oc}}{\gamma\left(1 - \frac{T_{\rm CE}^2}{2LC_p}\right)^M + 1}. \tag{11}$$

Thus, the residual voltage and peak current in each phase can be expressed as follows:

$$V_{p,m} = \frac{2V_{\rm oc}\left(1 - \frac{T_{\rm CE}^2}{2C_pL}\right)^m}{\gamma\left(1 - \frac{T_{\rm CE}^2}{2LC_p}\right)^M + 1} \tag{12}$$

$$I_m = \frac{V_{p,m-1}}{L}T_{\rm CE} = \frac{2T_{\rm CE}V_{\rm oc}\left(1 - \frac{T_{\rm CE}^2}{2LC_p}\right)^{m-1}}{L\left[\gamma\left(1 - \frac{T_{\rm CE}^2}{2LC_p}\right)^M + 1\right]}. \tag{13}$$

The net harvested energy can be calculated as the difference between extracted energy from the piezoelectric element and dissipated energy in the ESR. The extracted energy in the mth switching phase can be formulated as follows:

$$\Delta E_m = \frac{1}{2}C_p\left(V_{p,m-1}^2 - V_{p,m}^2\right). \tag{14}$$

The energy dissipation in each CE phase is

$$E_{d,m} = \frac{1}{3}I_m^2 r T_{\rm CE} \tag{15}$$

thus, the total harvested power can be expressed as the sum of the series

$$P_h = 2f\sum_{m=1}^{M}\left(\Delta E_m - E_{d,m}\right) \tag{16}$$

where f is the vibration frequency.

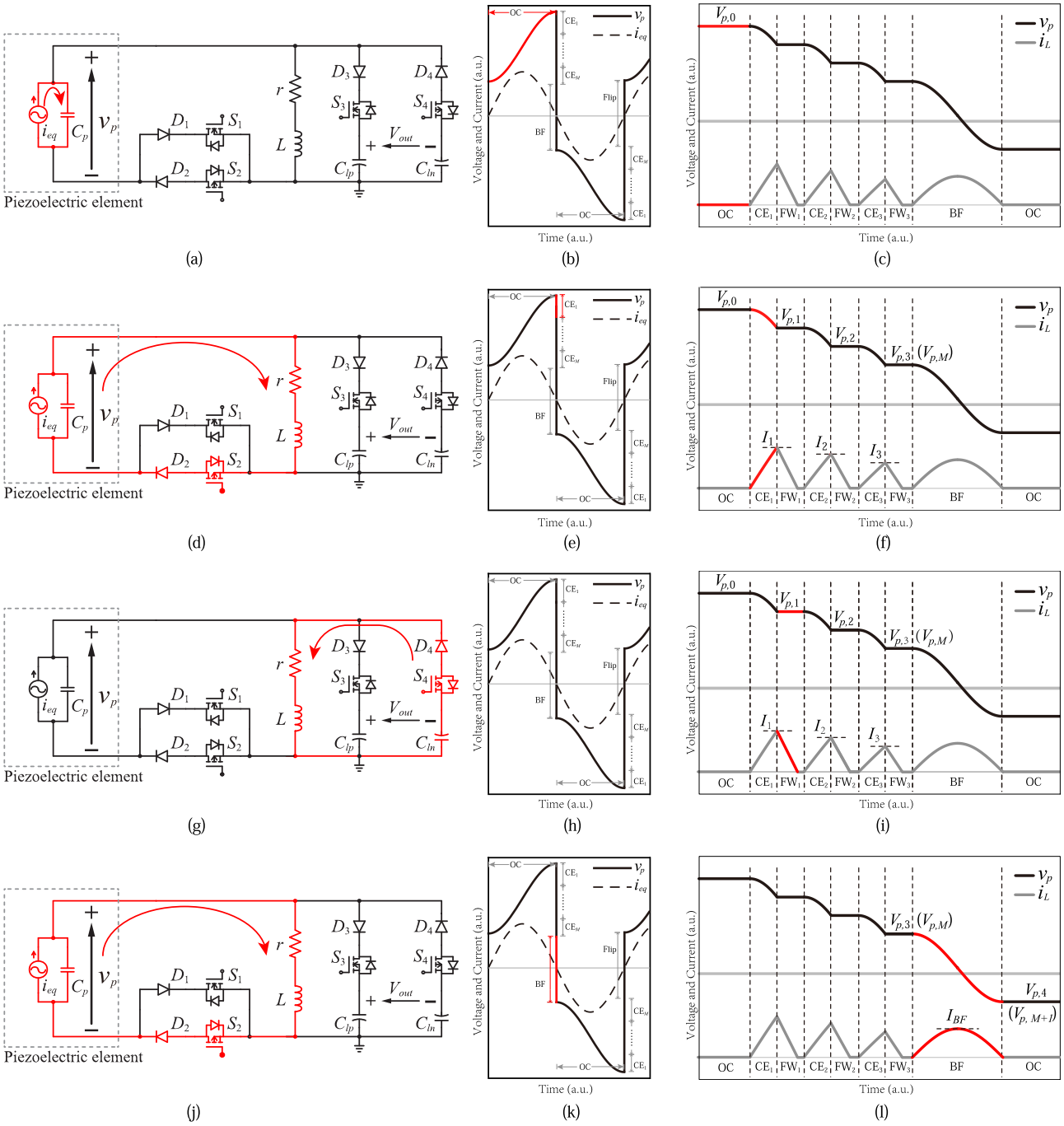


Fig. 4. Operating phases in the downstairs instant. (a), (d), (g), and (j) Conducting branches. (b), (e), (h), and (k) Waveform of the piezoelectric voltage during each phase. (c), (f), (i), and (l) Enlarged waveform of piezoelectric voltage and inductor current in the downstairs instant (a), (b), and (c) OC phase. (d), (e), and (f) One of the CE phases. (g), (h), and (i) One of the FW phases. (j), (k), and (l) BF phase.

B. Design Considerations

In the MCEBF circuit, there are four diodes (from D_1 to D_4) used for the current steering purpose. Although silicon or Schottky diodes introduce a voltage drop and dissipate some energy during the CE and FW phases, the application of diodes can simplify the control logic and circuit design. The CE, FW, and BF phases use the transient response of the r-L-C_p loop. After the inductor current crosses zero, the inductor tends to draw the current reversely. The reverse current can cause energy dissipation and produce high voltage to destroy the gate oxide of MOSFETs simultaneously. We can add a zero current detector (ZCD) [42] to solve such a problem or simply use diodes to passively block the reverse current. ZCD can be realized with high-speed and low-power comparators with CMOS technology. But for the discrete circuit, the delay of the discrete comparator and microcontroller causes a considerable reverse current in the FW and BF phases. Therefore, we choose the diode option to passively prevent the reverse current and protect the power MOSFETs as well. Since each power MOSFET (from S_1 to S_4) has an intrinsic body diode, they can

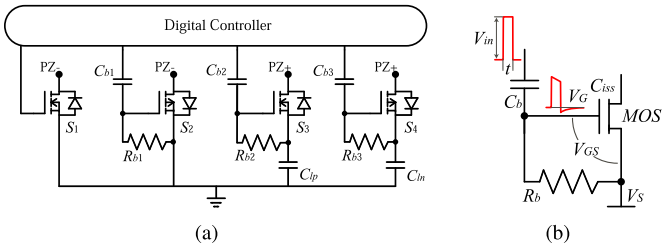


Fig. 5. (a) MOSFET's driver realized with RC bias-tee circuit. (b) Operating principle of the bias-tee circuit.

only block the current flow in a single direction. Adding those series diodes can also block the current in the other direction, that is, when the MOSFET body diode is forwardly biased.

Regular I/O ports cannot directly drive the switches S_2, S_3, and S_4. Some auxiliary driving circuits are needed. In MCEBF, due to the small duty cycle of the driving signals, such a function can be realized by the RC bias-tee circuits [42], as shown in Fig. 5(a). The source node of nMOS switch S_1 is connected to the ground; therefore, no driving circuit is needed. For the pMOS switch S_2, the source is grounded. A negative transient voltage is needed to turn on the device. The source nodes of the switches S_3 and S_4 are connected to the non-zero output voltages. Thus, three bias-tee structures are needed for S_2, S_3, and S_4. Fig. 5(b) shows an equivalent circuit of the bias-tee structure. The coupling capacitor C_b shares charge with the intrinsic input capacitor of MOSFET. Denoting the control voltage signal as V_{in}, the voltage applied to the gate node of the MOSFET is

$$V_{\text{GS0}} = \frac{C_b}{C_b + C_{\text{iss}}} V_{\text{in}} \tag{17}$$

where C_{iss} is the input capacitance of the gate node. To reduce the ON-state resistance, the MOSFET should be in the deep linear region when turned on, which requires sufficient overdrive voltage. According to (17), we should make $C_b \gg C_{\text{iss}}$. During the MOSFET ON-state, the bias resistor $R_{b,x}$ keeps discharging the capacitor and decreasing V_{GS}. Fast discharge may cause unexpected early shut-down. The drive voltage V_{GS} after the positive edge of the control signal can be expressed as follows:

$$V_{GS}(t) = V_{\text{GS0}} \exp\left[-\frac{t}{R_b(C_b + C_{\text{iss}})}\right] \tag{18}$$

where V_{GS0} is the initial voltage across the gate and source nodes of the MOSFET at the turn-on instant. According to (18), the value of R_b should be large enough to prevent unwanted early cutoff. Denoting the on-state interval as t_{ON} (e.g., the duration of BF phase), and 1-V overdrive voltage is needed to maintain the ON-state conductance, by solving (18), the resistance R_b should satisfy the inequality as follows:

$$R_b > \frac{t_{\text{on}}}{(C_b + C_{\text{iss}}) \ln \frac{V_{\text{GS0}}}{V_{\text{th}}+1}}. \tag{19}$$

IV. Optimal Control Strategy

Taking the number of shots M and the duration of each CE phase T_{CE} as variables, the larger M, the less dissipated power.

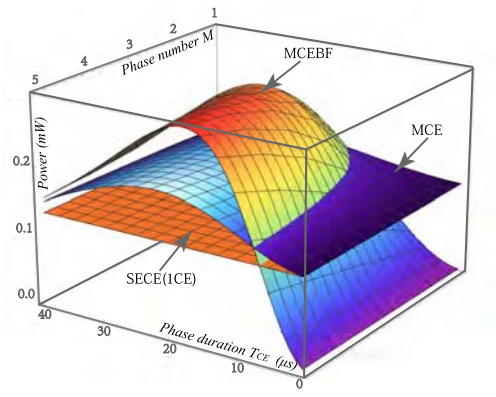


Fig. 6. Comparison of harvested power in MCEBF, MCE, and SECE.

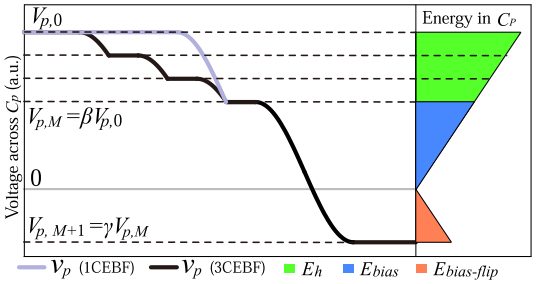


Fig. 7. Energy picture in each synchronized instant.

The harvested power of MCEBF as a function of T_{CE} and M are plotted in Fig. 6 based on the numerical result obtained with Wolfram Mathematica. The harvested power of MCE and SECE is also shown in Fig. 6 for comparison. The three surfaces stand for the power harvested via MCEBF, MCE, or SECE control with the same circuit configuration. MCEBF outperforms MCE and SECE around the optimal point of T_{CE}. The optimized value of T_{CE} cannot be directly obtained by solving the series. It can be obtained through energy analysis.

Neglecting the energy dissipation during the CE phases, which is more likely corrected to a large M value, the extracted energy during these CE phases equals the harvested energy. Under this assumption, the energy stored in C_p can be divided into two parts—the harvested part E_h and BF part E_{bias}, as shown in Fig. 7. In Fig. 7, the green region corresponds to the part of the extracted energy from the piezoelectric element. The blue region corresponds to the energy before the BF phase. The orange region is the energy after the BF action. We can find that the actions of multiple CEs only divide the extracted energy into several portions. It does not change the amount of energy, that is, the area of the green region in Fig. 7. The extracted portion relies on $V_{p,0}$ and $V_{p,M}$ values. The ratio between these two voltages determines the energy extraction of MCEBF. This voltage ratio can be defined as follows:

$$\beta = \frac{V_{p,M}}{V_{p,0}} \tag{20}$$

with β, the value of $V_{p,M+1}$, can be formulated as follows:

$$V_{p,M+1} = \gamma \beta V_{p,0}. \tag{21}$$

According to (11), the value of $V_{p,0}$ can be further simplified

$$V_{p,0} = \frac{2V_{\rm oc}}{1+\beta\gamma}. \tag{22}$$

The extracted energy in one cycle can be expressed as follows:

$$E_h = \frac{1}{2}C_p\left(V_{p,0}^2 - V_{p,M}^2\right). \tag{23}$$

Substituting (20) and (22) into (23), and taking the derivative of E_h with respect to β, we can have

$$\frac{dE_h}{d\beta} = -\frac{4(\beta+\gamma)C_pV_{\rm oc}^2}{(\beta\gamma+1)^3}. \tag{24}$$

The maximum value of E_h can be achieved when (24) equals zero. Consequently, we can have the optimal voltage ratio

$$\beta_{\rm opt} = -\gamma. \tag{25}$$

However, since β is not a direct variable for control implementation, we should figure out the optimal $T_{\rm CE}$ for timing control. Given an M value, according to (7) and (22), $V_{p,M}$ is expressed as follows:

$$V_{p,M} = \frac{2V_{\rm oc}\left(1-\frac{T_{\rm CE}^2}{2LC_p}\right)^M}{1-\gamma^2}. \tag{26}$$

With the optimal condition $\beta_{\rm opt} = -\gamma$, by solving (20), (22), and (26), the optimal value of $T_{\rm CE}$ toward the maximum harvested power can be formulated as follows:

$$T_{\rm CE,opt} = \frac{\sqrt{2\left[1-(-\gamma)^{\frac{1}{M}}\right]}}{\omega_{LC}} \tag{27}$$

where $\omega_{LC} = 1/\sqrt{LC_p}$ is the natural frequency of the L-C_p branch. The optimal CE duration $T_{\rm CE,opt}$ is a function of the piezoelectric capacitance C_p, inductance L, inversion factor γ, and number of CE phases M. All these variables are correlated with the intrinsic parameters of the harvesting circuit. They have relations with neither load conditions nor mechanical parameters (such as vibration frequency or OC voltage). Therefore, by setting M and its corresponding $T_{\rm CE,opt}$, the circuit can always work at optimal conditions, where the CE and BF phases realize the best allocation. A considerable power of the control overhead can be saved.

For a larger M value, as the peak current through the inductor decreases, the dissipation on ESR can be reduced. In non-ideal situations, the energy overhead (dissipation) in control, current steering, and so on should be more obvious for larger M. In practical implementations, the selection of M value needs to consider the tradeoff between less switch dissipation and extra overhead for carrying out MCE actions.

V. Energy Flow

To further compare the EH capabilities among SECE, MCE, and MCEBF, the analysis of energy flow is made by referring to the charge–voltage (Q–V) diagram [39]. Q–V diagram can intuitively illustrate the energy conversion in one vibration cycle. In the Q–V diagram, the area enclosed by the closed trajectory stands for the total electrical energy extracted from the mechanical domain. The trajectory can be divided into several phases.

In SECE, at each synchronized instant when $i_{\rm eq}$ crosses zero, the absolute voltage across C_p is $2V_{\rm oc}$, the stored energy in the piezoelectric capacitor is

$$E_{C_p,\rm SECE} = 2C_pV_{\rm oc}^2. \tag{28}$$

There are two synchronized instants in each vibration cycle. In each instant, only one CE action is carried out. Thus, the energy extracted from the mechanical domain is twice that in (28). The dissipation of SECE is formulated in (2). By referring to this formula, the Q–V diagram of SECE is shown in Fig. 8(a) [40]. The purple regions stand for the energy dissipation of ESR in SECE. The green region is the net harvested power. SECE can deplete all the electric charge stored in C_p in each synchronized instant. As (2) implies, the ESR in the PEH circuit can cause considerable energy dissipation, when γ is near zero.

MCE divides the energy extraction phase into several steps [five steps in the example of Fig. 8(b)]. The dissipated energy in each CE phase with the duration of $T_{\rm CE}$ was formulated in (15). The energy dissipation in the final step (from $V_{p,4}$ to 0) can be formulated with (2). The Q–V diagram of the whole MCE process is shown in Fig. 8(b). The total extracted energy ΔE is the same as that in SECE. Due to the multi-shot extraction technology, the energy dissipation represented by the purple region is divided into several parts. With the increase of CE steps, the peak current of the inductor is suppressed and the energy dissipation is reduced as well. As a result, MCE can harvest more energy from a piezoelectric structure by only reducing the energy dissipation of the ESR.

In MCEBF, it contains not only several CE actions, but also a BF action. Thus, the initial voltage $V_{p,0}$ is larger than $2V_{\rm oc}$. The expression of $V_{p,0}$ was given in (11). As a result, the energy extracted from the mechanical domain in each vibration cycle is formulated as follows:

$$\Delta E_{\rm MCEBF} = 4C_pV_{\rm oc}^2\frac{1+\gamma^2}{1-\gamma^2}. \tag{29}$$

In the Q–V diagram, the MCEBF trajectory encloses a larger parallelogram, as shown in Fig. 8(c). The formula of dissipated energy in CE actions is the same as (15) gives. The energy dissipation in the BF phase is expressed as follows:

$$E_{d,\rm BF} = \frac{1}{2}C_p\left(1-\gamma^2\right)V_{p,m}^2. \tag{30}$$

Under the optimal condition, (30) can be further simplified as follows:

$$E_{d,\rm BF,opt} = \frac{2C_pV_{\rm oc}^2\gamma^2}{1-\gamma^2}. \tag{31}$$

Combining (7), (20), and (25), the voltage of the mth CE phase can be expressed as follows:

$$V_{p,m} = V_{p,0}(-\gamma)^{\frac{m}{M}}. \tag{32}$$

According to (13) and (15), the total energy dissipation in M rounds of CE phases is

$$E_{d,\rm MCE} = \frac{rt_{\rm CE}^3\left(1-\gamma^2\right)}{3L^2\left[1-(-\gamma)^{\frac{2}{M}}\right]}V_{p,0}^2. \tag{33}$$

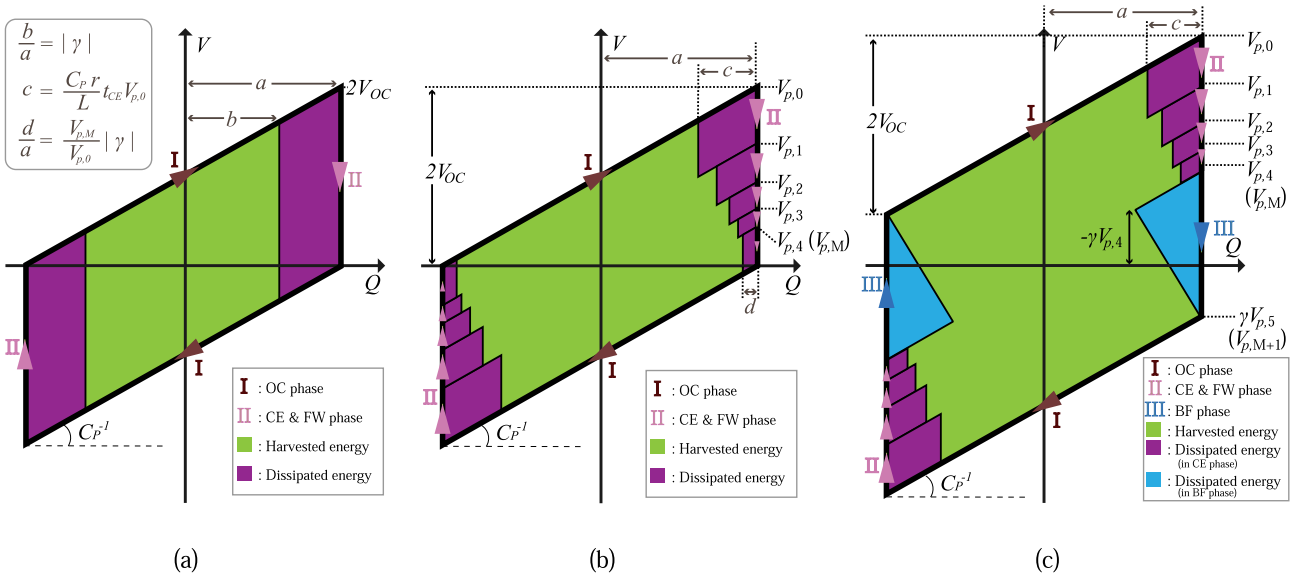


Fig. 8. Charge–voltage diagram of (a) SECE (1CE), (b) MCE, and (c) MCEBF.

TABLE I
CONVERSION EFFICIENCY UNDER DIFFERENT M (CE SHOTS)

M (CE shots)	1	2	3	4
Efficiency	43.3%	49.6%	52.3%	54.3%

The corresponding area of $E_{d,\mathrm{MCE}}$ is shown in Fig. 8(c) in purple. The larger M, the more reduction of dissipation during the CE phases (smaller total purple area). The conversion efficiency (from extracted power to harvested power) is evaluated in simulation to validate the benefit when M gets larger. The simulation parameters are listed in Table II. As Table I shows, the conversion efficiency gets higher under a larger M value. Compared with SECE and MCE, a BF action is added in MCEBF. The BF action introduces extra energy dissipation $E_{d,\mathrm{BF}}$ (as the blue region shows), but can bias an initial voltage for the next OC phase. The extra income of the extracted energy (larger enclosed area in Fig. 8) is greater than the extra dissipated energy introduced by the BF action (blue area). This can be qualitatively observed between the different Q–V plots of Fig. 8(b) and (c).

VI. EXPERIMENTAL

Experiments are carried out to measure the output voltage under different strengths of each CE scheme, in order to check the agreement between the derived optimal T_{CE} and the best timing in practice. The circuit of MCEBF can also be reprogrammed into SECE or MCE without any hardware modification. A fair comparison among MCEBF, MCE, and SECE is carried out based on the same prototype.

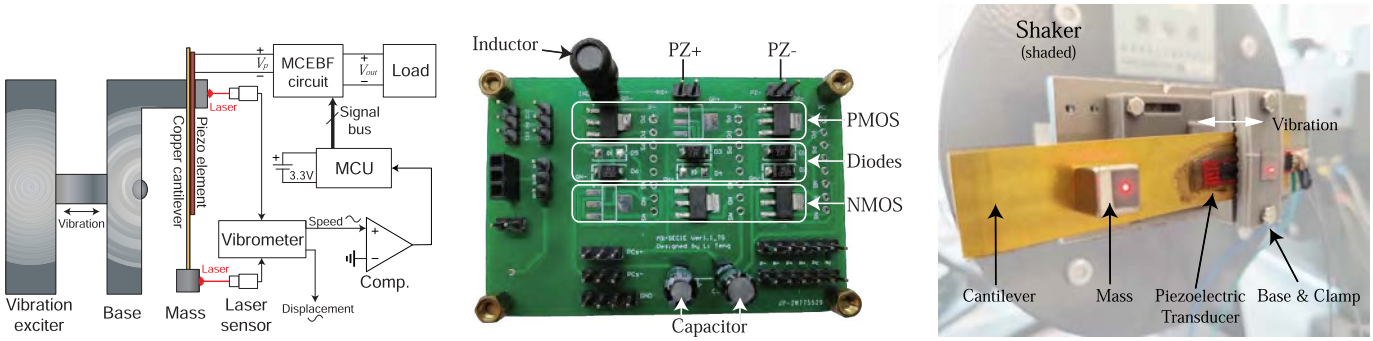
The diagram of the experimental setup is shown in Fig. 9(a). The printed circuit board (PCB) of MCEBF is shown in Fig. 9(b). STM32F103RCT6 microcontroller development board is used for signal processing and control. The signals from I/O pins are coupled to the MOSFETs by the RC bias-tee circuit. The peak detection is realized by using a vibrometer (Polytec OFV-552). It tracks the beam deflection amplitude for triggering the synchronized switch actions at the instants of extreme deflection. The piezoelectric cantilever is installed on a shaker, as shown in Fig. 9(c). The displacement amplitude is locked at 520 μm to create a case that the global electromechanical coupling is weak, or $k^2 \approx 0$ [43]. Detailed parameters of the experimental setup are listed in Table II. The load capacitors C_{ln} and C_{lp} have two values: the 10 μF ones are used as the storage capacitors in common conditions; while the 1 μF ones are utilized to manifest the output voltage fluctuation during the FW phases for better observation.

TABLE II
PARAMETERS OF THE CIRCUIT IN EXPERIMENTS

Parameter	Value/Type	Parameter (×number)	Value/Type
Piezo patch (PZT)	50×7.2×0.84 mm^3	L	47 mH
Cantilever (copper)	100×20×0.65 mm^3	$R_{ESR,\mathrm{L}}$	149 Ω
C_p	32 nF	C_{ln}, C_{lp}	10 μF, 1 μF
r	360 Ω	C_b	2.2 nF
γ	−0.62	R_b	10 MΩ
f	38.91 Hz	NMOS×2	ZVN4424GTA
Displacement (p-p)	520 μm	PMOS×2	ZVP4424GTA
V_{oc}	6.4 V	Diode×4	1N4002-SMD

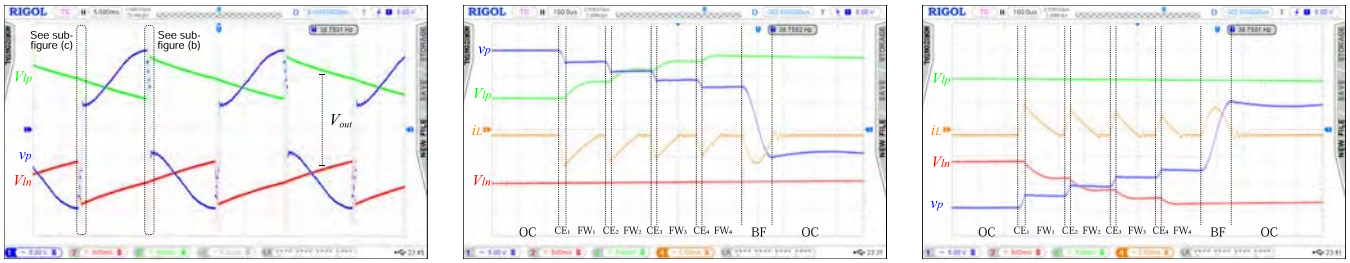
A. Operating Waveform

The operating waveforms of 4CEBF, for example, are shown in Fig. 10. In 4CEBF, there are four CE and four FW phases, and one BF phase in each synchronized instant. Fig. 10(a) shows the voltage overview in 4CEBF, including v_p the voltage across the piezoelectric transducer, V_{out} the voltages across two output capacitors, and i_L the inductor current. During a synchronized instant, the piezoelectric voltage drops or rises in a stair shape. The v_p downstairs instant is shown in Fig. 9(b). The simulated waveforms under the same condition were shown in Fig. 4. In 4CEBF, the energy is extracted gradually from the piezoelectric element by the inductor in four steps. After four steps of CE, the residual charge is flipped



(a) (b) (c)

Fig. 9. Experimental setup. (a) Setup diagram. (b) PCB prototype of MCEBF. (c) Piezoelectric structure.



(a) (b) (c)

Fig. 10. MCEBF experimental waveform. (a) Overview. (b) Enlarged view of a v_p downstairs instant. (c) Enlarged view of a v_p upstairs instant.

to prebias v_p, such that to prepare for the reversely charging in the next half-cycle. In Fig. 10(b) and (c), each FW phase has a long time duration. The long FW time ensures the complete depletion of the inductor current, in particular, when the load voltage is low.

B. Optimal Timing

The optimized control was derived in Section IV. The optimized CE phase timing $T_{\mathrm{CE,opt}}$ was given in (27). In this section, an experiment is performed to validate the theoretical optimal T_{CE} value. The circuit is configured to carry out MCEBF with M varying from one to four. We sweep the CE phase timing T_{CE} around the theoretical value derived in (27), while keeping other variables including the piezoelectric transducer and load resistance the same. The steady-state output voltage V_{out} is recorded to reflect the harvested power under different T_{CE} timing configurations.

As Fig. 11 shows, when the number of switching phases varies from one to four, the maximum power points in the experiment are close to the prediction of (27). Based on the sweep data, the peak of the output voltage is close to the theoretically derived T_{CE}. The theoretically derived optimal T_{CE} in Section IV is validated.

C. Performance Comparison

SECE and MCE can also be implemented by changing the control of this circuit prototype. Comparisons with SEH and parallel synchronized switch harvesting on inductor (P-SSHI) are also taken. For SEH, an FBR consisting of 1N4002-SMD diodes is used to rectify the piezoelectric voltage. For P-SSHI,

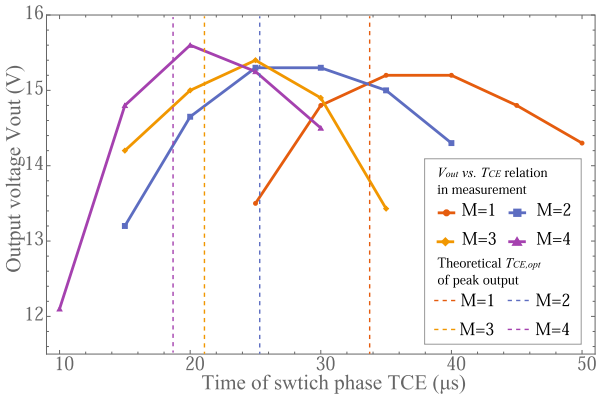


Fig. 11. Measured output voltage with different phase number M and switching duration T_{CE} ($R_L = 2$ MΩ).

the BF action is performed by the MCEBF circuit with no CE phase. The rectifier of P-SSHI is the same as the SEH setup. Other parameters of these interface circuits are provided in Table II. By sweeping the load resistance connected across the positive and negative output nodes, the harvested power of SEH, SECE (1CE), P-SSHI, and 4CEBF as a function of the output voltage is shown in Fig. 12. MCEBF can harvest 487% more power than SEH and 95% more power than SECE. Compared with P-SSHI (BF only), MCEBF can harvest 49% more power. Other comparison data, including some results from different experimental platforms, are listed in Table III.

Fig. 12 also shows the harvested power of SECE, MCE, and MCEBF with different M values. It can be observed that multistep switching actions can provide additional energy benefits in both MCE and MCEBF. The output power approaches

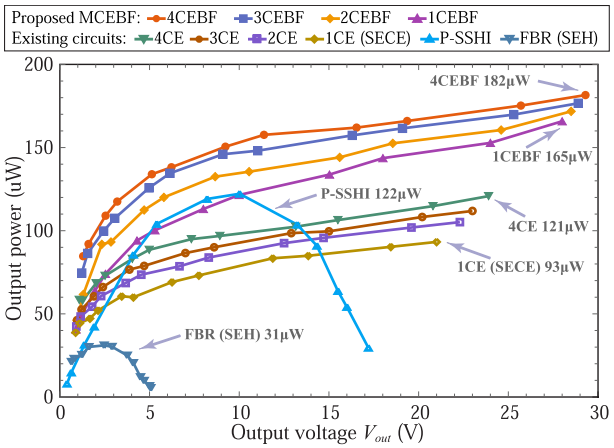


Fig. 12. Output power of MCEBF and MCE under different M values along with SEH.

TABLE III
HARVESTED POWER INCREMENT, COMPARED WITH SEH

Technology	Increment	Technology	Increment
SECE [11]	200%[a]	SSHI [8]	294%[a]
MS-SECE [28]	290%[a]	SMBF [30]	287%[b]
SSHC [32]	258% ∼ 721%[b]	DSSH [34]	up to 400%[b]
SICE [36]	up to 500%[b]	**MCEBF**	**487%**[a]

[a] Based on the measured result using the same setup of Fig. 9.
[b] Based on the results from literature.

are stable when the output voltage is above 10 V. Compared with SEH and P-SSHI, the solutions involving CEs, that is, SECE, MCE, and MCEBF, are more reluctant to load variation. Higher output voltage shortens the FW interval; thus, it reduces the circuit dissipation toward higher harvested power. Based on the measured results, MCEBF can significantly improve the harvesting capability compared with SECE and MCE. The merit of load independence or reluctance in SECE is inherited in MCEBF. Therefore, the optimal output power can be maintained under a wide range of load resistance.

VII. CONCLUSION

As summarized in [30], the improvement of PEH capability can be made in four steps: synchronizing the piezoelectric voltage and current polarities; utilizing passive BF actions to enlarge the voltage magnitude; adding an active BF action to further enlarge the voltage magnitude further; making a trade-off between increasing power extraction and decreasing power dissipation. MCEBF interface circuit is an enhanced version of SECE and MCE solutions for weakly coupled piezoelectric transducers. MCEBF integrally fulfills the philosophy of "increasing income and reducing expenditure." It extracts the electric charge in the piezoelectric element in multiple steps and flips the voltage with a BF action. The effectiveness of MCEBF was theoretically studied through energy analysis. The optimal control method was derived in theoretical form and validated in experiments. In the experiment, MCEBF can harvest 487% more power than SEH, 95% more power than SECE, and 49% more power than P-SSHI. Compared with SECE, MCEBF improves the harvesting capability without introducing additional sensors or control loops, which proves its high feasibility. These results confirm the effectiveness of the proposed MCEBF.

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