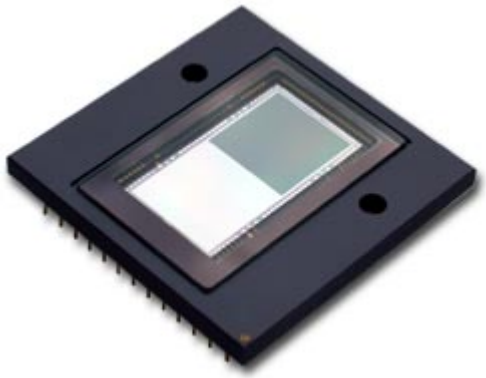
DATA SHEET



FTT1010M

1M Frame Transfer CCD Image Sensor

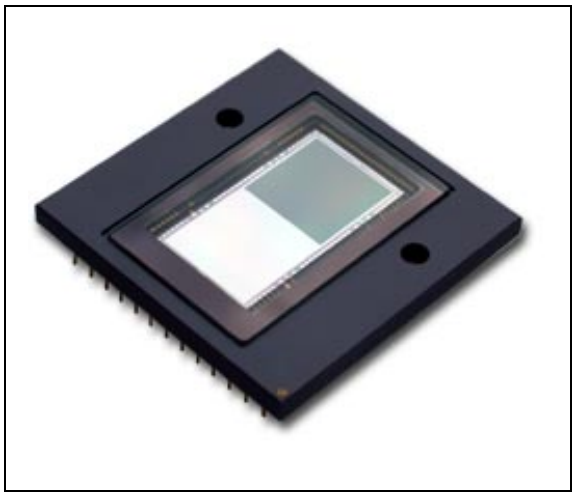
Product specification

2007, April 17

DALSA
Professional Imaging

1M Frame Transfer CCD Image Sensor FTT1010M

- **1-inch optical format**
- **1M active pixels (1024H x 1024V)**
- **Progressive scan**
- **Excellent antiblooming**
- **Variable electronic shuttering**
- **Square pixel structure**
- **H and V binning**
- **100% fill factor**
- **High dynamic range (>72dB)**
- **High sensitivity**
- **Low dark current and fixed pattern noise**
- **Low readout noise**
- **Data rate up to 2 x 40 MHz**
- **Mirrored and split readout**
- **RoHS compliant**



Description

The FTT1010M is a monochrome progressive-scan frame-transfer image sensor offering 1K x 1K pixels at 30 frames per second through a single output buffer. The combination of high speed and a high linear dynamic range (>12 true bits at room temperature without cooling) makes this device the perfect solution for high-end real time medical X-ray, scientific and industrial applications. A second output can either be used for mirrored images, or can be read out simultaneously with other output to double the frame rate. The device structure is shown in figure 1.

Device structure

Optical size:	12.288 mm (H) x 12.288 mm (V)
Chip size:	14.572 mm (H) x 26.508 mm (V)
Pixel size:	12 μm x 12 μm
Active pixels:	1024 (H) x 1024 (V)
Total no. of pixels:	1072 (H) x 1030 (V)
Optical black pixels:	Left: 20 Right:20
Timing pixels:	Left: 4 Right:4
Dummy register pixels:	Left: 7 Right: 7
Optical black lines:	Bottom: 6 Top: 6

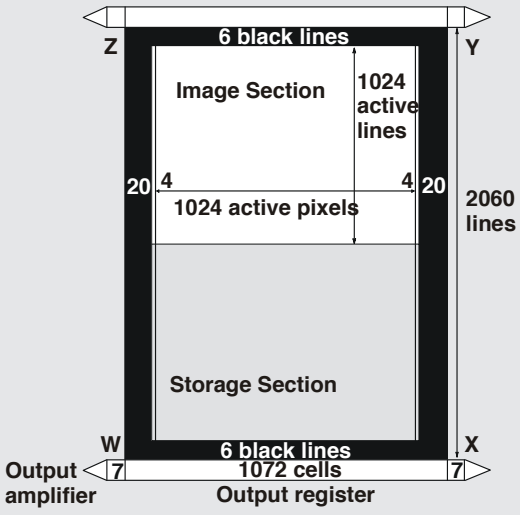


Figure 1 – Device Structure

Architecture of the FTT1010M

The FTT1010M consists of a shielded storage section and an open image section. Both sections are electronically the same and have the same cell structure with the same properties. The only difference between two sections is the optical light shield.

The optical centres of all pixels in the image section form a square grid. The charge is generated and integrated in this section. Output registers are located below the storage section. The output amplifiers Y and Z are not used in Frame Transfer mode and should be connected as not-used amplifiers.

After the integration time, the charge collected in the image section is shifted to the storage section. The charge is read out line by line through the lower output register.

The left and the right half of each output register can be controlled independently. This enables either single or multiple readout.

During vertical transport, the C3 gates separate the pixels in the register. The letters W, X, Y, and Z are used to define the four quadrants of the sensor. The central C3 gates of both registers are part of the W and Z quadrants of the sensor.

Both upper and lower registers can be used for vertical binning. Both registers also have a summing gate at each end that can be used for horizontal binning. Figure 2 shows the detailed internal structure.

IMAGE SECTION	
Image diagonal (active video only)	17.38 mm
Aspect ratio	1:1
Active image width x height	12.288 x 12.288 mm^2
Pixel width x height	12 x 12 μm^2
Fill factor	100%
Image clock pins	A1, A2, A3, A4
Capacity of each clock phase	2.5nF per pin
Number of active lines	1024
Number of black reference lines	6
Total number of lines	1030
Number of active pixels per line	1024
Number of overscan (timing) pixels per line	8 (2x4)
Number of black reference pixels per line	40 (2x20)
Total number of pixels per line	1072

STORAGE SECTION	
Storage width x height	12.864 x 12.360 mm^2
Cell width x height	12 x 12 μm^2
Storage clock phases	B1, B2, B3, B4
Capacity of each clock phase	2.5nF per pin
Number of cells per line	1072
Number of lines	1030

OUTPUT REGISTERS	
Output buffers (three-stage source follower)	4 (one on each corner)
Number of registers	2 (one above, one below)
Number of dummy cells per register	14 (2x7)
Number of register cells per register	1072
Output register horizontal transport clock pins	C1, C2, C3
Capacity of each C-clock phase	60pF per pin
Overlap capacity between neighbouring C-clocks	20pF
Output register Summing Gates	4 pins (SG)
Capacity of each SG	15pF
Reset Gate clock phases	4 pins (RG)
Capacity of each RG	15pF

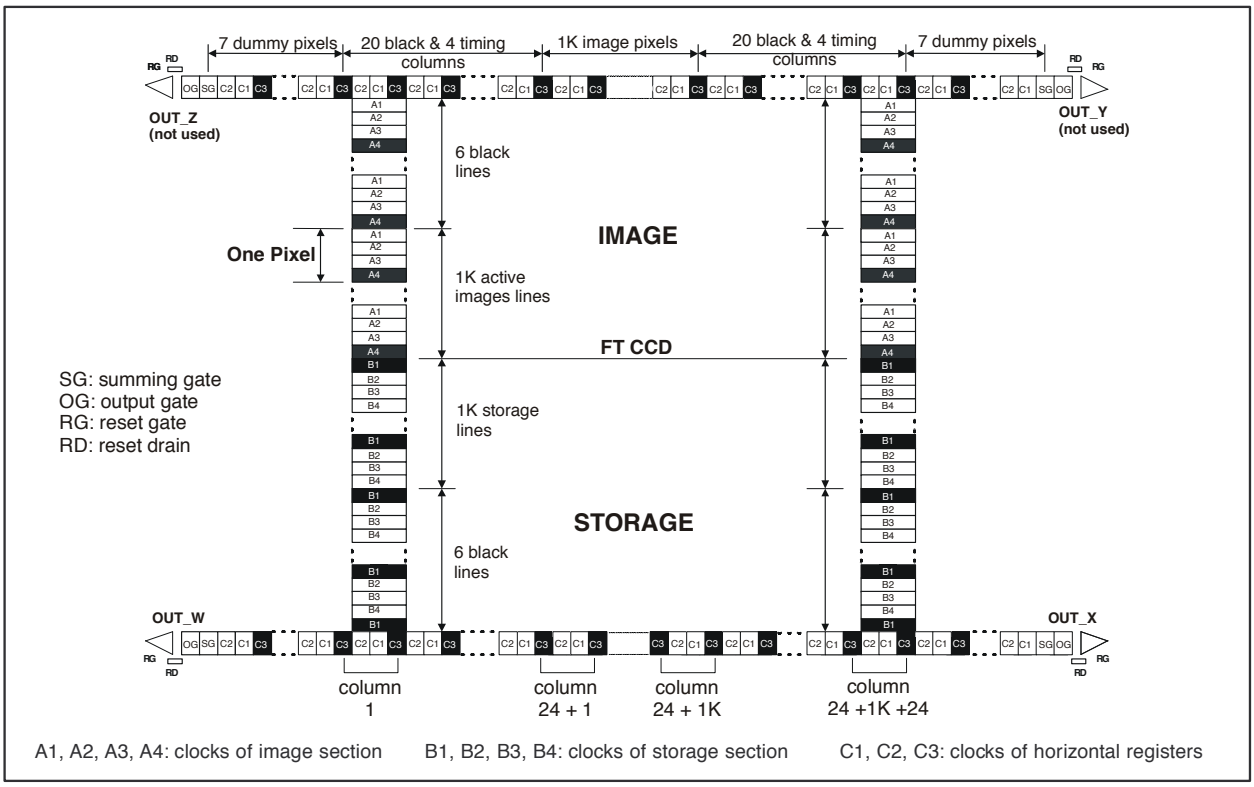


Figure 2 - Detailed internal structure

Specifications

ABSOLUTE MAXIMUM RATINGS[1]	MIN	MAX	UNIT
GENERAL:			
storage temperature	-55	+80	°C
ambient temperature during operation	-40	+60	°C
voltage between any two gates	-20	+20	V
DC current through any clock (absolute value)	-0.2	+0.2	μA
OUT current (no short circuit protection)	0	10	mA
VOLTAGES IN RELATION TO VPS:			
VPS, SFD, RD	-0.5	+30	V
VCS, SFS	-8	+5	V
All other pins	-5	+25	V
VOLTAGES IN RELATION TO VNS:			
SFD, RD	-15	+0.5	V
VCS, SFS, VPS	-30	+0.5	V
All other pins	-30	+0.5	V

DC CONDITIONS[2,3]		MIN [V]	TYPICAL [V]	MAX [V]	MAX [mA]
VNS[4]	N substrate	20	24	28	15
VPS	P substrate	1	3	7	15
SFD	Source Follower Drain	16	20	24	4.5
SFS	Source Follower Source	-	0	-	1
VCS	Current Source	-5	0	3	_
OG	Output Gate	4	6	8	_
RD	Reset Drain	13	15.5	18	_

AC CLOCK LEVEL CONDITIONS[2]	MIN	TYPICAL	MAX	UNIT
IMAGE CLOCKS:				
A-clock amplitude during integration and hold	8	10		V
A-clock amplitude during vertical transport (duty cycle=5/8) [5]	10	14		V
A-clock low level		0		V
Charge Reset (CR) level on A-clock[6]	-5	-5		V
STORAGE CLOCKS:				
B-clock amplitude during hold	8	10		V
B-clock amplitude during vertical transport (duty cycle=5/8)	10	14		V
OUTPUT REGISTER CLOCKS:				
C-clock amplitude (duty cycle during hor. transport=3/6)	4.75	5	5.25	V
C-clock low level	2	3.5		V
Summing Gate (SG) amplitude		10	10	V
Summing Gate (SG) low level		3.5		V
OTHER CLOCKS:				
Reset Gate (RG) amplitude	5	10	10	V
Reset Gate (RG) low level		3		V
Charge Reset (CR) pulse on Nsub[6]	0	10	10	V

[1] During Charge Reset it is allowed to exceed maximum rating levels (see note 5)
[2] All voltages in relation to SFS
[3] Power-up sequence: VNS, SFD, RD, VPS, others
[4] To set the VNS voltage for optimal Vertical Antiblooming (VAB), it should be adjustable between minimum and maximum values
[5] Three-level clock is preferred for maximum charge; the swing during vertical transport should be 4V higher than the voltage during integration
A two level clock (typically 10V) can be used if a lower maximum charge handling capacity is allowed
[6] Charge Reset can be achieved in two ways:
- The typical CR level is applied to all image clocks simultaneously (preferred).
- The typical A-clock low level is applied to all image clocks; for proper CR, an additional Charge Reset pulse on VNS is required. This will also affect the charge handling capacity in the storage areas.

Timing diagrams (for default operation)

AC CHARACTERISTICS	MIN	TYPICAL	MAX	UNIT
Horizontal frequency (1/Tp)[1]	0	18	40	MHz
Vertical frequency	0	450	1000	kHz
Charge Reset (CR) time	2	20		μs
Rise and fall times: image clocks (A)	10	20		ns
storage clocks (B)	10	20		ns
register clocks (C)[2]	3	5	1/6 Tp	ns
summing gate (SG)	3	5	1/6 Tp	ns
reset gate (RG)	3	5	1/6 Tp	ns

[1] TP=1 clock period
[2] Duty cycle=50% and phase shift of the C clocks is 120 degrees

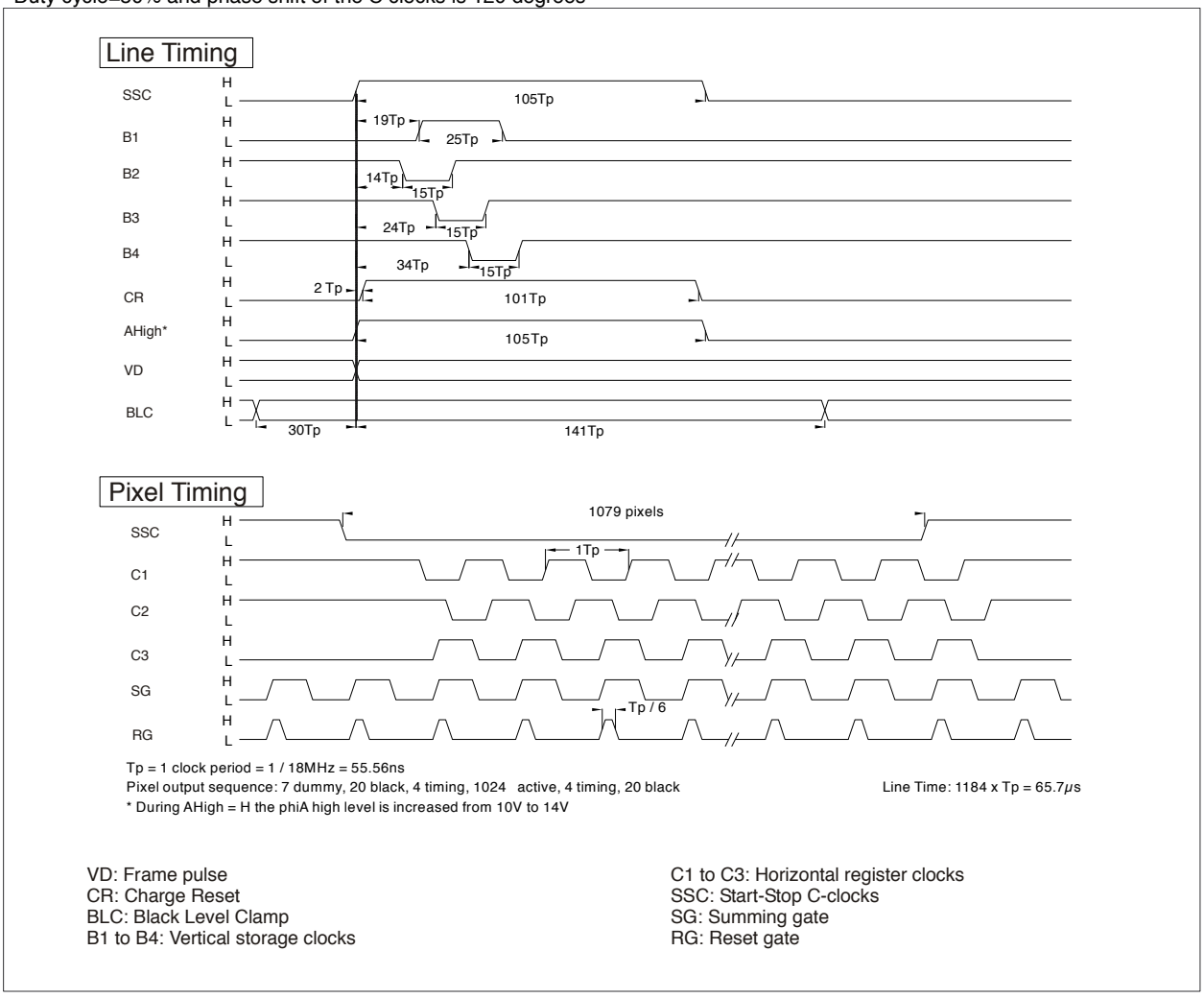
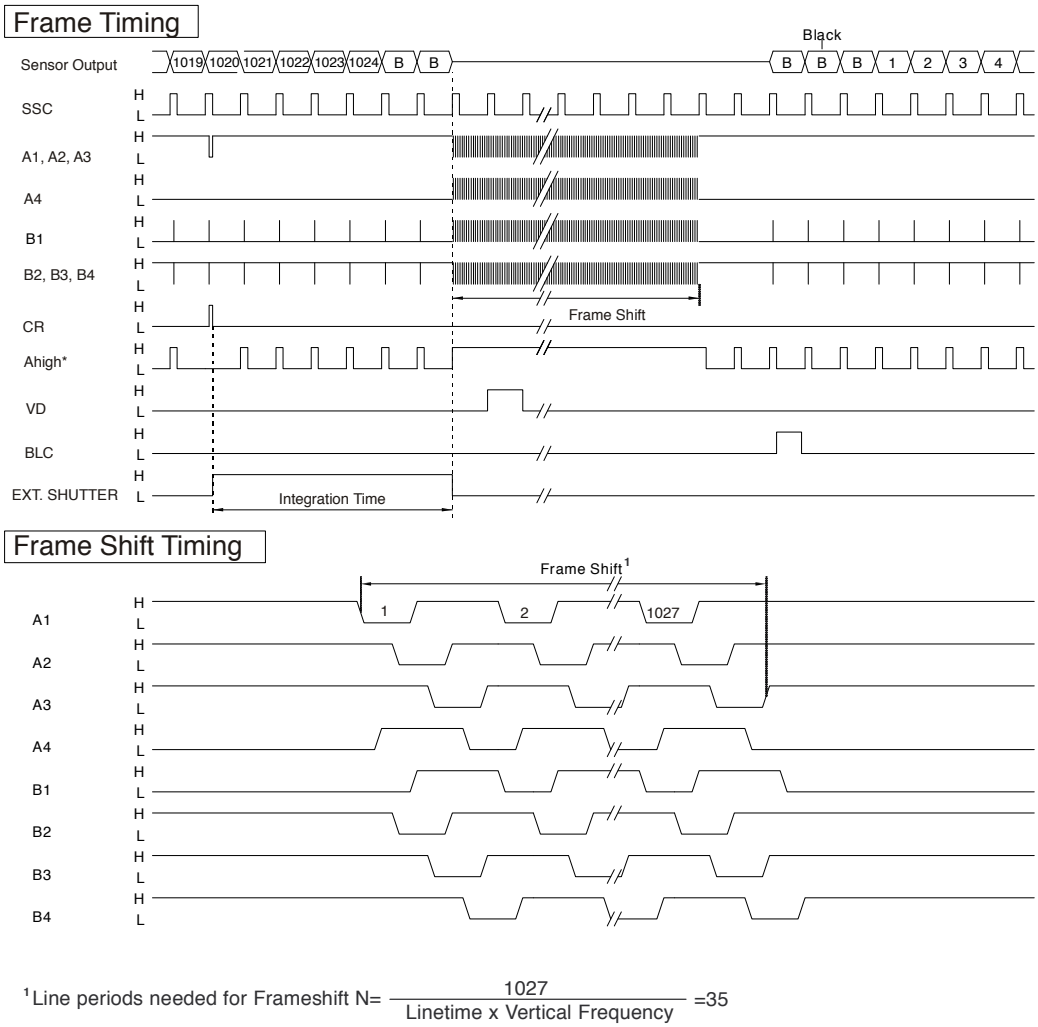


Figure 3 - Line and pixel timing diagrams



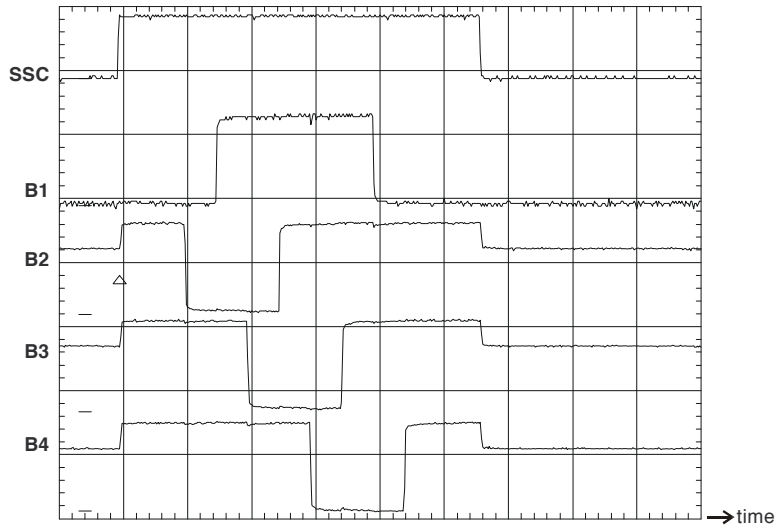
[1] Line periods needed for Frameshift N= $\frac{1027}{\text{Linetime x Vertical Frequency}}$ =35

VD: Frame pulse
CR: Charge Reset
BLC: Black Level CLamp
A1 to A4: Vetical Image clocks

B1 to B4: Vertical storage clocks
C1 to C3: Horizontal register clocks
SSC: Start-Stop C-clocks
SG: Summing gate
RG: Reset gate

Figure 4 - Frame timing diagrams

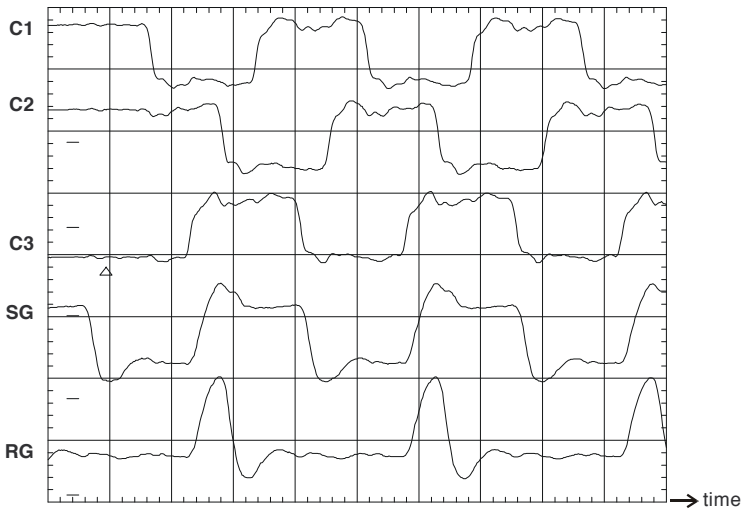
Line timing



Y/Div. : 10V (B1, B2, B3, B4); 5V (SSC)

Figure 5 - Vertical readout

Pixel timing



Y/Div. : 5V (C1, C2, C3); 10V (SG, RG)

Figure 6 - Start horizontal readout

Performance

The test conditions for the performance characteristics are as follows:

- All values are measured using typical operating conditions.
- VNS is adjusted as low as possible while maintaining proper Vertical Antiblooming
- Sensor temperature=60°C (333K)
- Horizontal transport frequency=18MHz
- Vertical transport frequency=450kHz
- Integration time=10ms
- The light source is a lamp of 3200K in conjunction with neutral density filters and a 1.7mm thick BG40 infrared cut-off filter. For Linear Operation measurements, a temperature conversion filter (Melles Griot type no. 03FCG261, -120 mired, thickness: 2.5mm) is applied.

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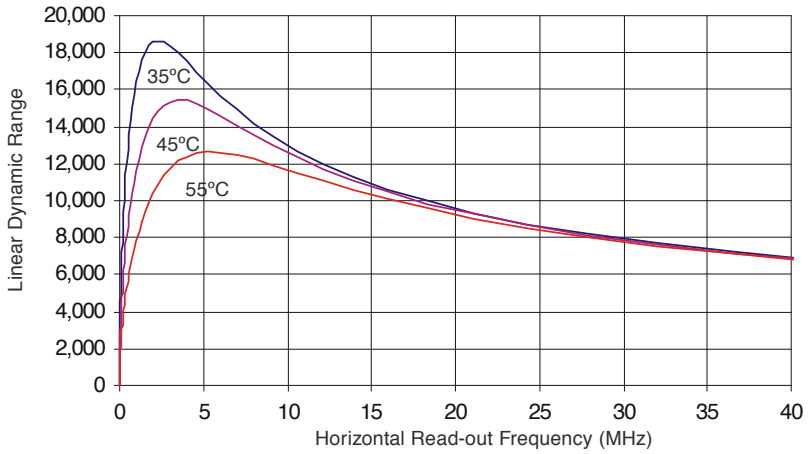
LINEAR OPERATION	MIN	TYPICAL	MAX	UNIT
Charge Transfer Efficiency[1] vertical		0.999995		
Charge Transfer Efficiency[1] horizontal		0.999999		
Image lag			0	%
Smear[2]		-39	0	dB
Resolution (MTF) @ 42lp/mm	65			%
Light sensitivity	180	250		kel/lux•s
Low Pass Shading[3]			2.5	%
Random Non-Uniformity (RNU)[4]		0.3	5	%

[1]Charge Transfer Efficiency values are tested by evaluation and expressed as the value per gate transfer.
[2]Smear is defined as the ratio of 10% of the vertical transport time to the integration time. It indicates how visible a spot of 10% of the image height would become.
[3]Low Pass Shading is defined as the ratio of the one-σ value of the pixel output distribution expressed as a percentage of the mean value output (low-pass image).
[4]RNU is defined as the ratio of the one-σ value of the highpass image to the mean signal value at nominal light.



Linear dynamic range is defined as the ratio of Q_{lin} to read-out noise (the latter reduced by Correlated Double Sampling).

Figure 7 - Typical Linear dynamic range vs. horizontal read-out frequency and sensor temperature

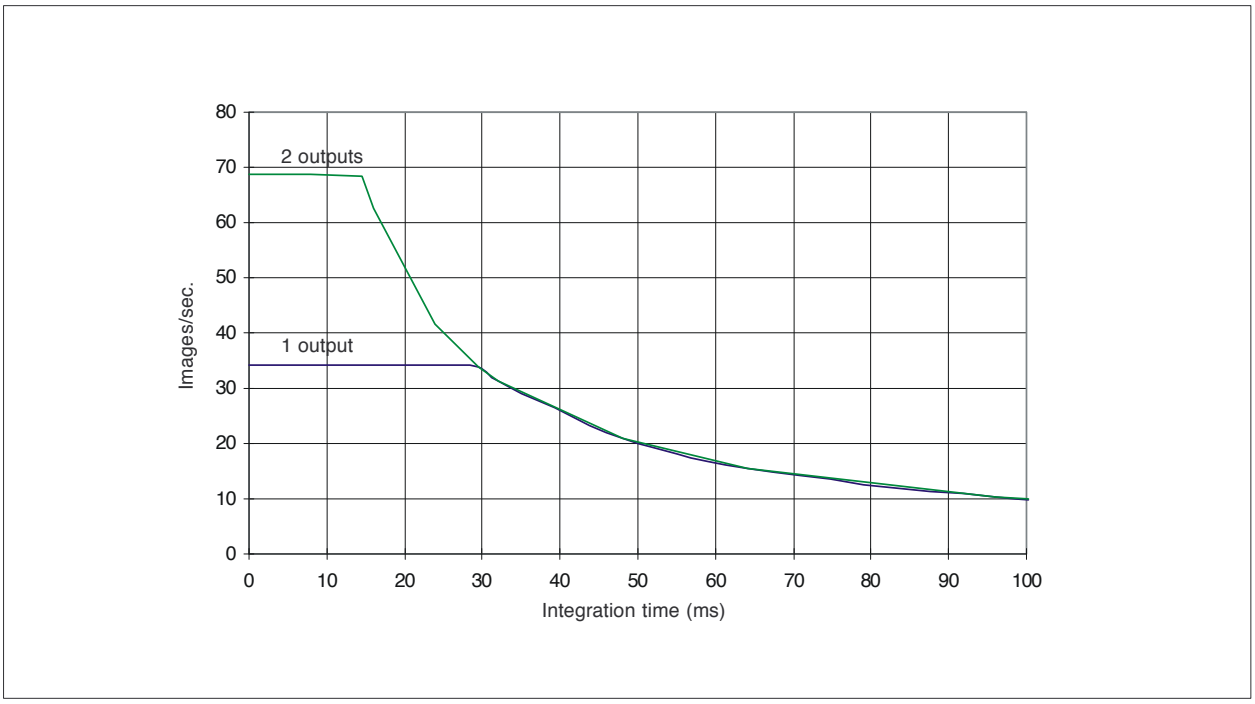


Figure 8 - Maximum number of images/second versus integration time

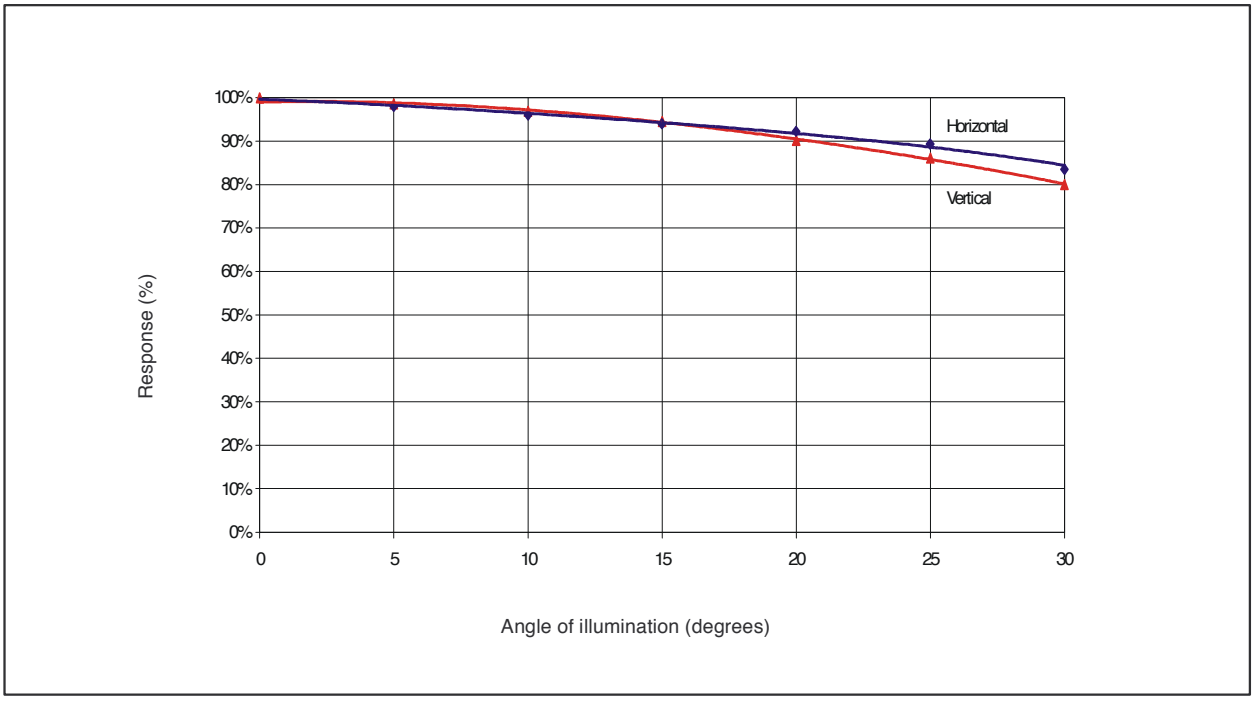


Figure 9 - Angular response versus angle of illumination

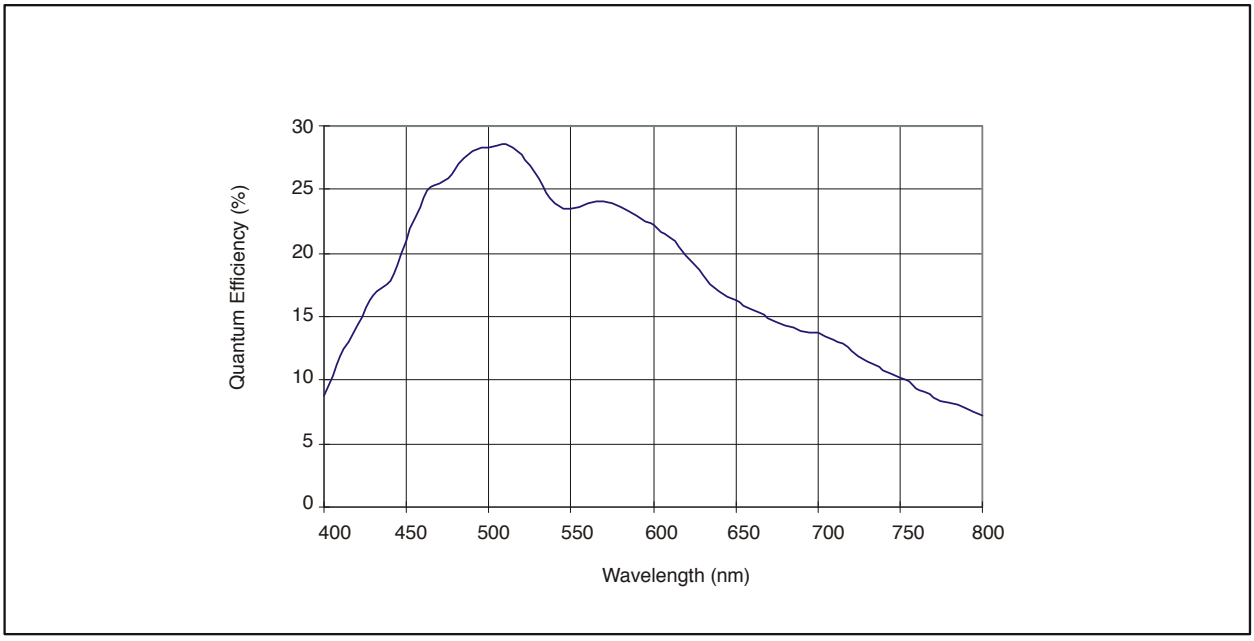


Figure 10 - Quantum efficiency versus wavelength

LINEAR/SATURATION	MIN	TYPICAL	MAX	UNIT
Full-well capacity saturation level (Qmax)[1]	250	500	600	kel
Full-well capacity linear operation (Qlin)[2]	200	350		kel
Charge handling capacity[3]		600		kel
Overexposure[4] handling	100	200		x Qmax level

[1]Qmax is determined from the low-pass filtered image.
[2]The linear full-well capacity Qlin is calculated from linearity test (see dynamic range). The evaluation test guarantees 97% linearity.
[3]Charge handling capacity is the largest charge packet that can be transported through the register and read-out through the output buffer.
[4]Overexposure over entire area while maintaining good Vertical Antiblooming (VAB). It is tested by measuring the dark line.

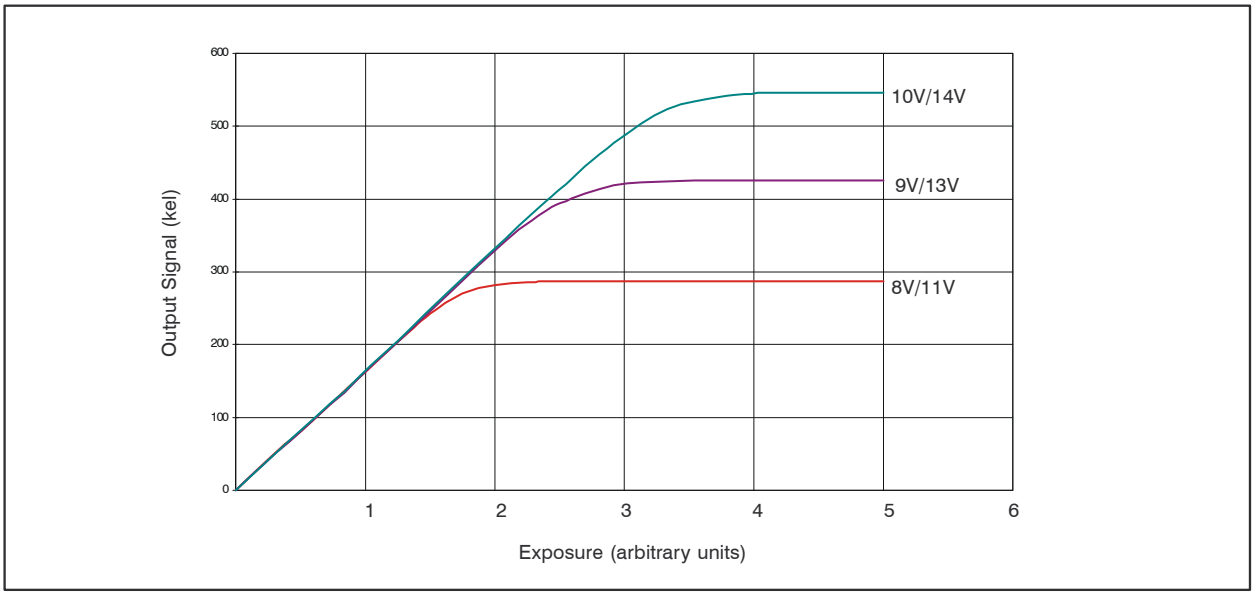


Figure 11 – Charge handling versus integration/transport voltage

OUTPUT BUFFERS	MIN	TYPICAL	MAX	UNIT
Conversion factor	6	8	12	μV/el
Mutual conversion factor matching (ΔACF)[1]		0	2	μV/el
Supply current		4		mA
Bandwidth		110		MHz
Output impedance buffer (R_{load}=3.3Ω, C_{load}=2pF)		400		Ω

[1]Matching of the four outputs is specified as ΔACF with respect to reference measured at the operating point (Q_{lin}/2)

DARK CONDITION	MIN	TYPICAL	MAX	UNIT
Dark current level @ 20°C		10	30	pA/cm^2
Dark current level @ 60°C		0.3	0.6	nA/cm^2
Fixed Pattern Noise[1] (FPN) @ 60ºC		15	25	el
RMS readout noise @ 9MHz bandwidth after CDS		25	30	el

[1]FPN is one-σ value of the high-pass image.

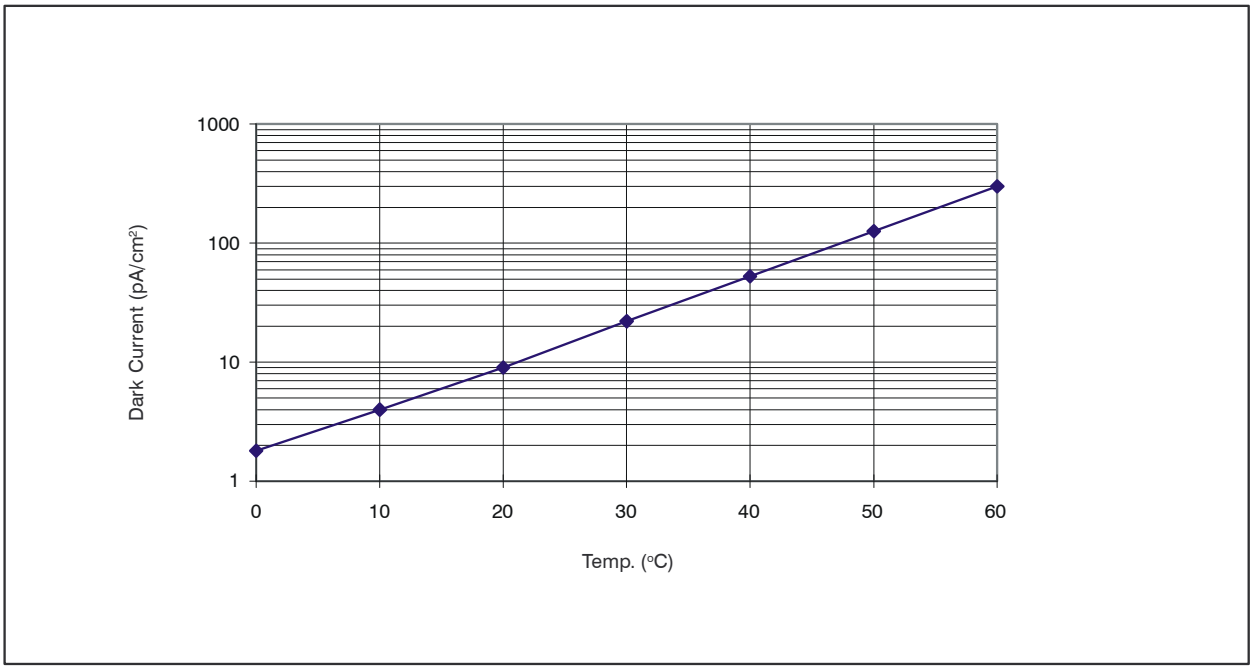


Figure 12 – Dark current versus temperature

Application information

Current handling
One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from overexposure), free electrons are drained to VNS. No current should flow into any VPS connection of the sensor. During high overexposure a total current of 10 to 15mA through all VPS connections together may be expected. The PNP emitter follower in the circuit diagram (figure 12) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During high overexposure, a total current of 10 to 15mA through all VNS connections together may be expected. The clamp circuit, consisting of the diode and electrolytic capacitor, enables the addition of a Charge Reset (CR) pulse on top of an otherwise stable VNS voltage. To protect the CCD, the current resulting from this pulse should be limited. This can be accomplished by designing a pulse generator with a rather high output impedance.

Decoupling of DC voltages
All DC voltages (not VNS, which has additional CR pulses as described above) should be decoupled with a 100nF decoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons that build up the charge packets that will reach the floating diffusions only add up to a small current, which will float through VRD. Therefore, a large series resistor in the VRD connection may be used.

Outputs
To limit the on-chip power dissipation, the output buffers are designed with open source outputs. Outputs to be used should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 400Ω) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is avoided by avoiding a too-small quiescent current in the emitter follower; about 10mA should do the job. The collector of the emitter follower should be decoupled properly to suppress the Miller effect from the base-collector capacitance.

A CCD output load resistor of 3.3Ω typically results in a bandwidth of 110MHz. The bandwidth can be enlarged to about 130MHz by using a resistor of 2.2kΩ instead, which, however, also enlarges the on-chip power dissipation.

Device protection
The output buffers of the FTT1010M are likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera. The RD voltage should always be lower than the SFD voltage.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 10mA. Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-type substrate, we are dealing with some parasitic npn transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram of figure 12.

Unused sections
To reduce power consumption, the following steps can be taken. Connect unused output register pins (C1...C3, SG, OG) and unused SFS pins to zero Volts.

More information
Detailed application information is provided in the application note AN01 entitled “**Camera Electronics for the mK x nK CCD Image Sensor Family**”.

Device Handling

An image sensor is a MOS device which can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in the CCD image sensor process is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remain undamaged. When handling the sensor, use fingercots.

When cleaning the glass we recommend using ethanol (or possibly water). Use of other liquids is strongly discouraged:

- if the cleaning liquid evaporates too quickly, rubbing is likely to cause ESD damage.
- the cover glass and its coating can be damaged by other liquids.

Rub the window carefully and slowly.

Dry rubbing of the window may cause electro-static charges or scratches which can destroy the device.

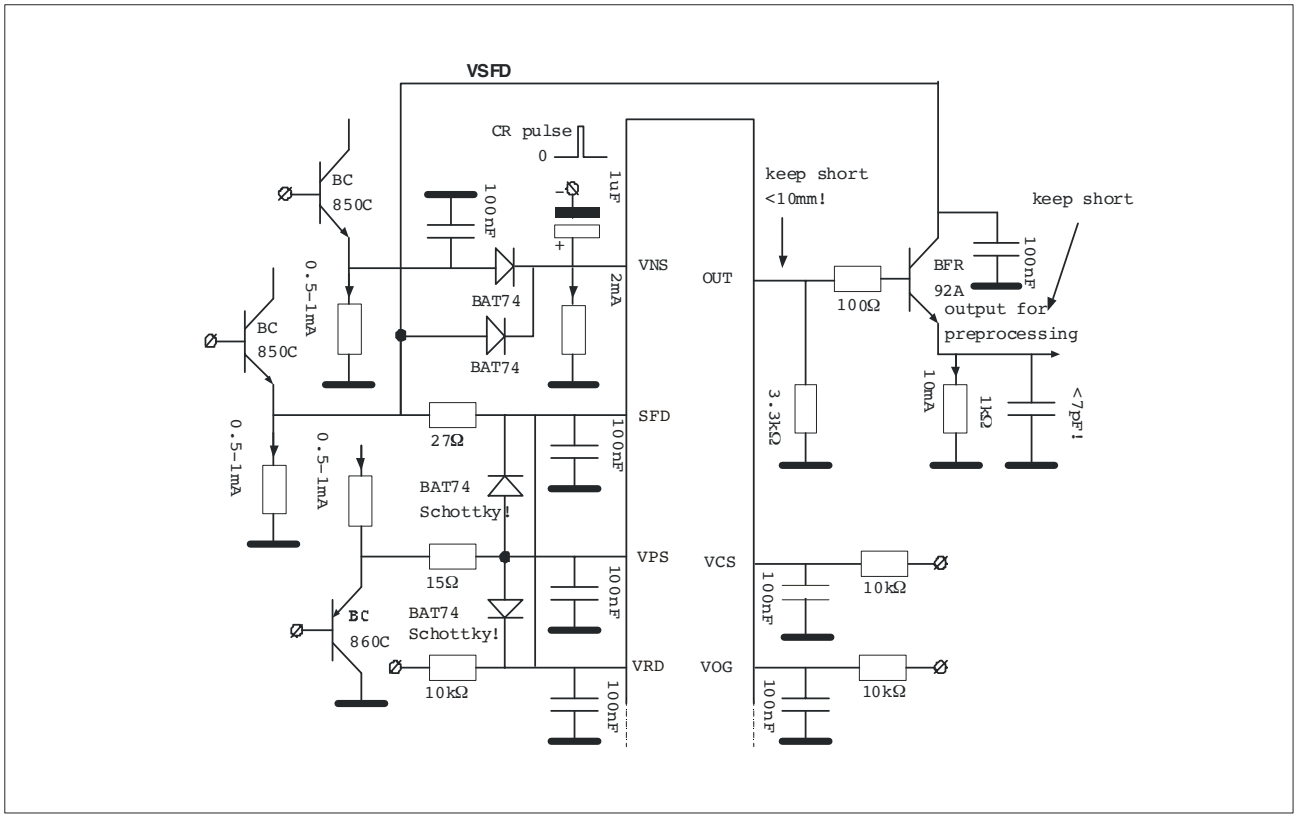


Figure 13– Application diagram

Pin configuration

The FTT1010M is mounted in a Pin Grid Array (PGA) package with 80 pins in a 15x13 grid of 40.00 x 40.00 mm^2. The position of pin A1 is marked with a gold dot on top of the package. The image clock phases of quadrant W are internally connected to X, and the clock phases of Y are connected to Z.

SYMBOL	LINEAR/SATURATION	PIN # W	PIN # X	PIN # Y	PIN # Z
VNS	N substrate	A12	A3	J2	F11
VNS	N substrate	D11	B2	F3	H12
VNS	N substrate	E11	D3	-	J11
VNS	N substrate	E12	E2	-	-
VNS	N substrate	-	E3	-	-
VPS	P substrate	C11	C3	G3	G11
SFD	Source Follower Drain	A13	A1	J1	J13
SFS	Source Follower Source	A10	B5	J4	H9
VCS	Current Source	A11	A4	J3	J10
OG	Output Gate	B13	B1	H1	H13
RD	Reset Drain	B12	B3	H2	H11
A1	Image Clock (Phase 1)	-	-	F1	F13
A2	Image Clock (Phase 2)	-	-	G2	G12
A3	Image Clock (Phase 3)	-	-	F2	F12
A4	Image Clock (Phase 4)	-	-	G1	G13
B1	Storage Clock (Phase 1)	D13	D1	-	-
B2	Storage Clock (Phase 2)	C12	C2	-	-
B3	Storage Clock (Phase 3)	D12	D2	-	-
B4	Storage Clock (Phase 4)	C13	C1	-	-
C1	Register Clock (Phase 1)	B9	A6	H5	J8
C2	Register Clock (Phase 2)	B8	A7	H6	J7
C3	Register Clock (Phase 3)	A8	B6	J6	H8
SG	Summing Gate	B10	A2	H4	J12
RG	Reset Gate	A9	A5	J5	J9
OUT	Output	B11	B4	H3	H10
NC	Not Connected	B7		H7	

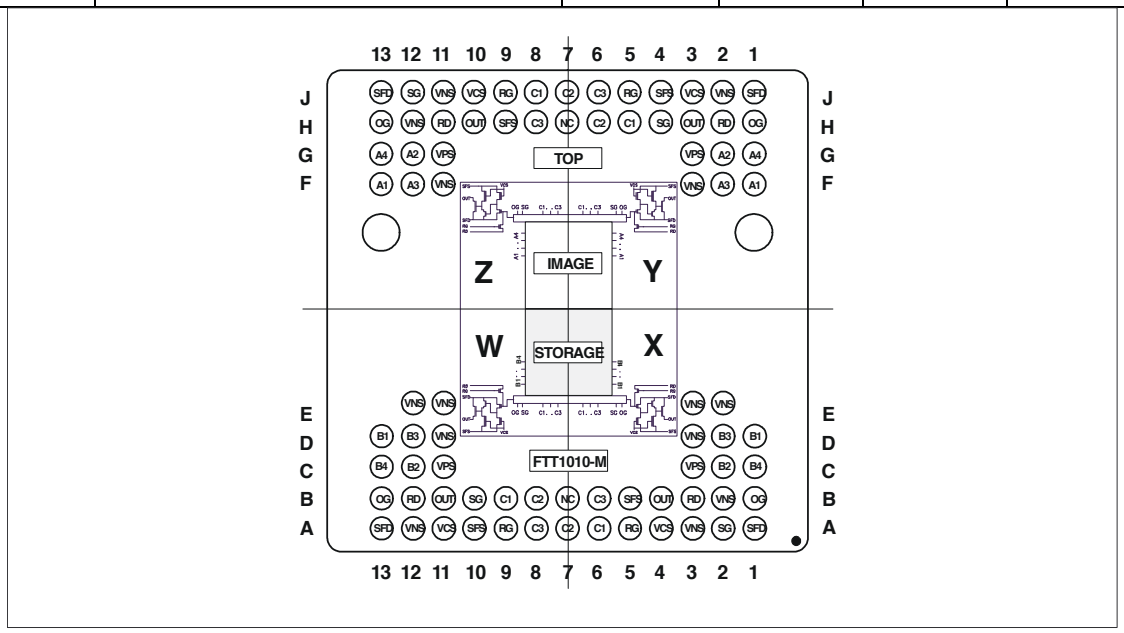


Figure 14 - Pin configuration (top view)

Package information

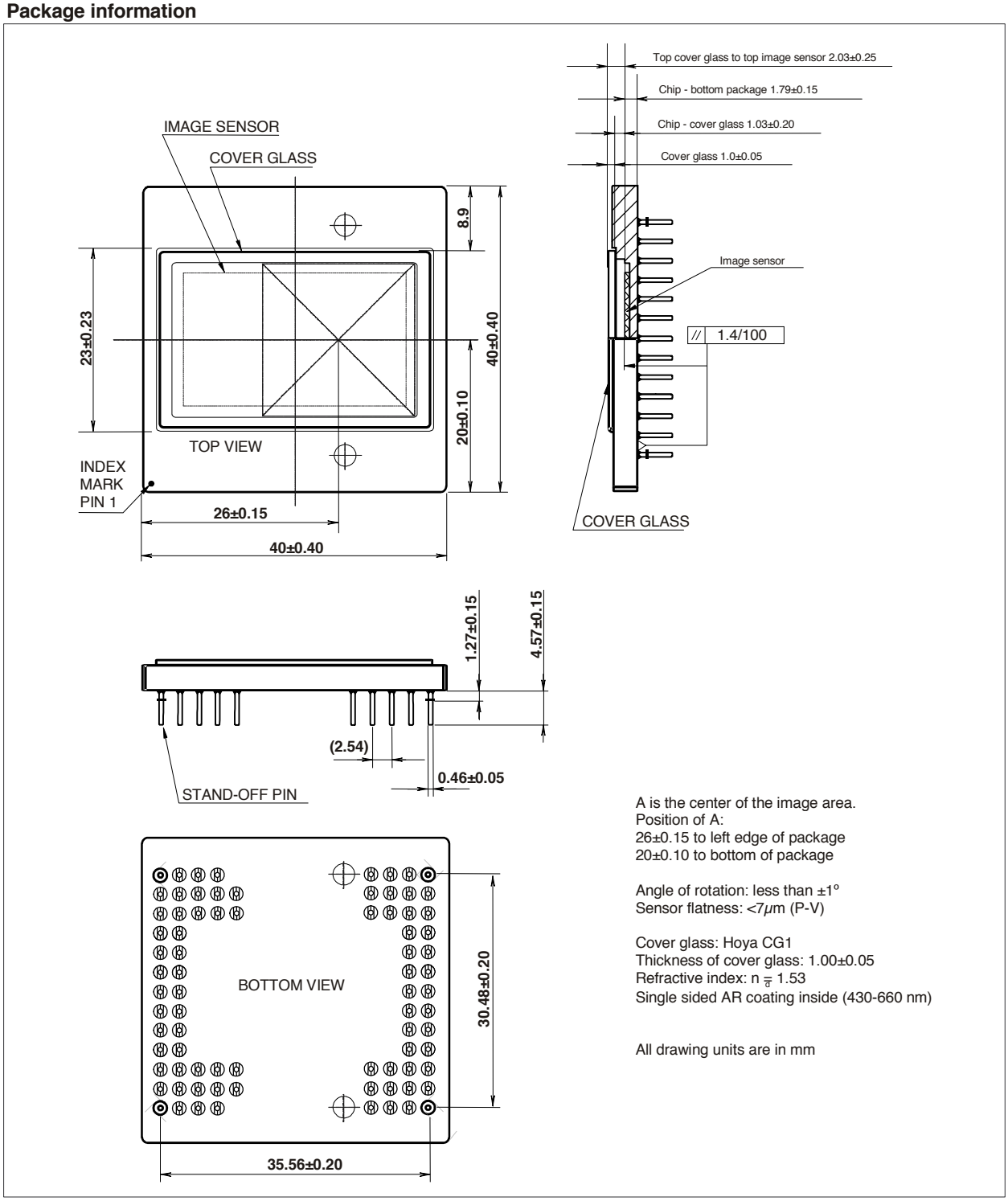


Figure 15– Mechanical drawing of the PGA package of the FTT1010M

Order codes

The sensor can be ordered using the following code:

FTT1010M sensors		
Description	**Quality Grade**	**Order Code**
FTT1010M/TG	Test grade	9922 157 35231
FTT1010M/EG	Economy grade	9922 157 35251
FTT1010M/IG	Industrial grade	9922 157 35221
FTT1010M/HG	High grade	9922 157 35211

Defect Specifications

The CCD image sensor can be ordered in a specific quality grade. The grading is defined with the maximum amount of pixel defects, column defects, row defects and cluster defects, in both illuminated and non-illuminated conditions. For detailed grading information, please contact your local DALSA representative.

For More Information

For more detailed information on this and other products, contact your local rep or visit our Web site at http://www.dalsa.com/sensors/products/products.asp.

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