Finite State Machines modeling using Verilog HDL

Mohammed A. Elsha3rawy

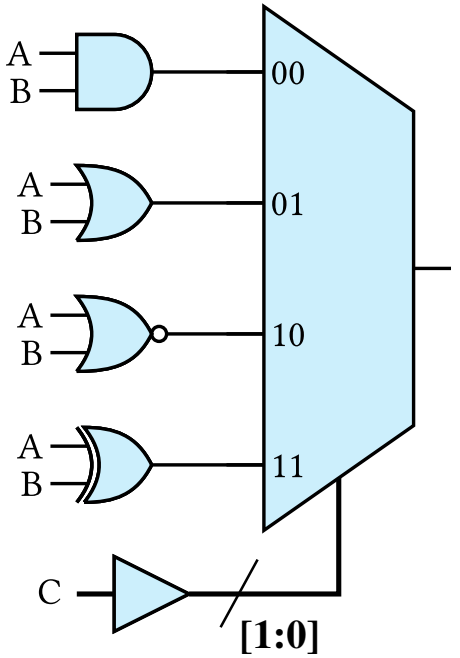
Contents

Combinational Circuits

-- **Consists of (logic gates, Mux, DeMux, encoder, decoder, …)**

-- **Output depends only on the input**

-- **Don't have any memory cells or latches**



" Don't ever forget The third info. "

Finite State Machines

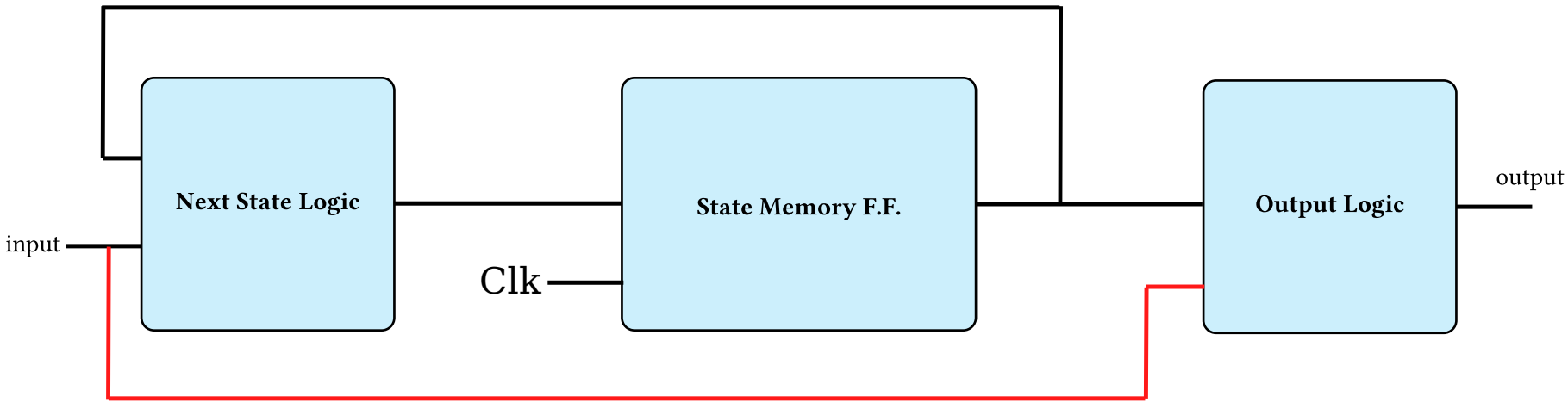
-- **Don't depend on input (at least not only)**

-- **Consist of combinational parts as well as memory cells (Flip_Flop)**

-- **Most famous applications :**

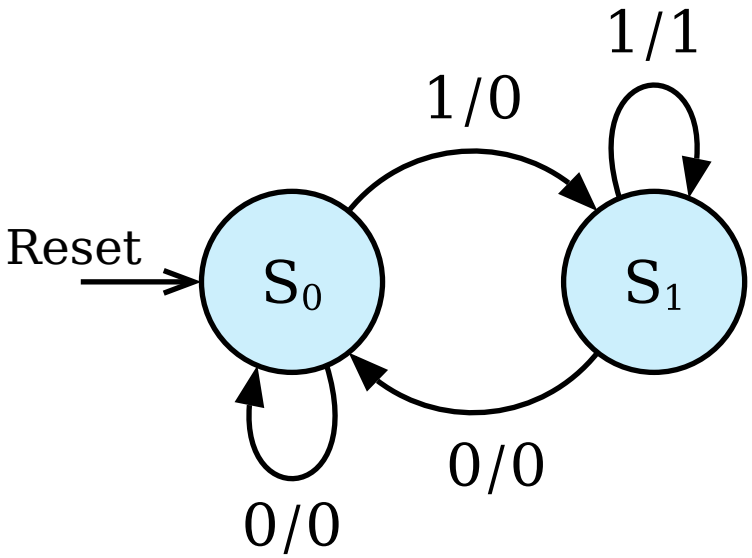
1. **Sequence Detectors "comm. protocol"**
2. **Control units**

Finite State Machines "Internals"

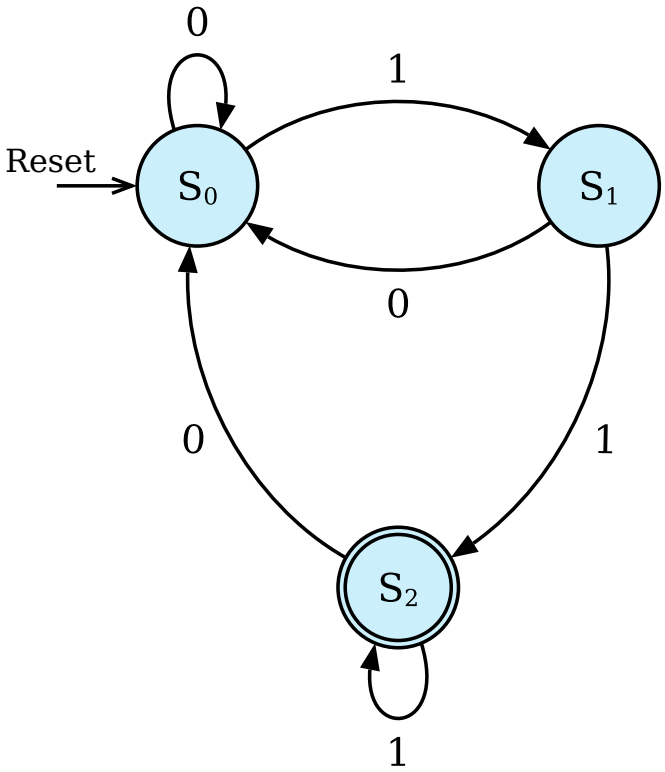


internal structure of FSM

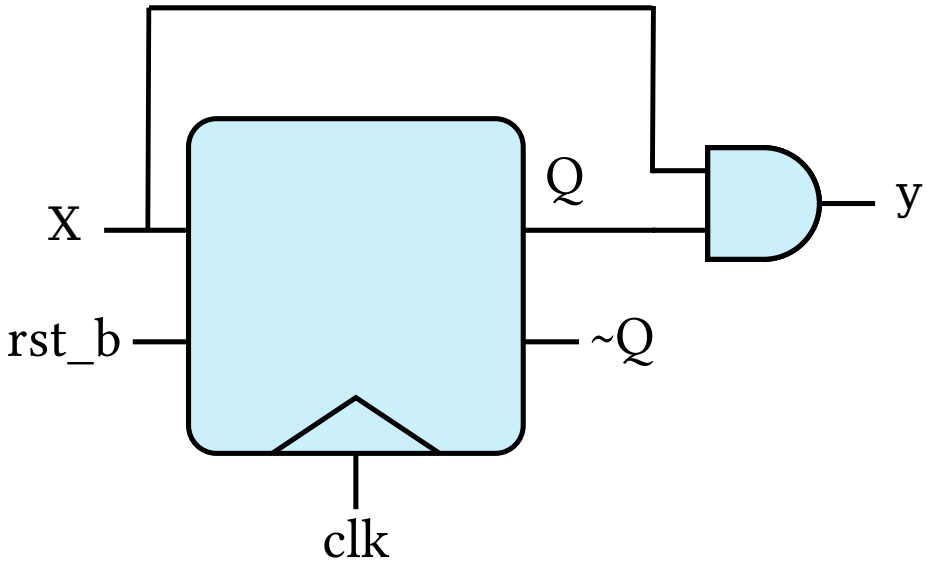
"11" Sequence detector - Mealy



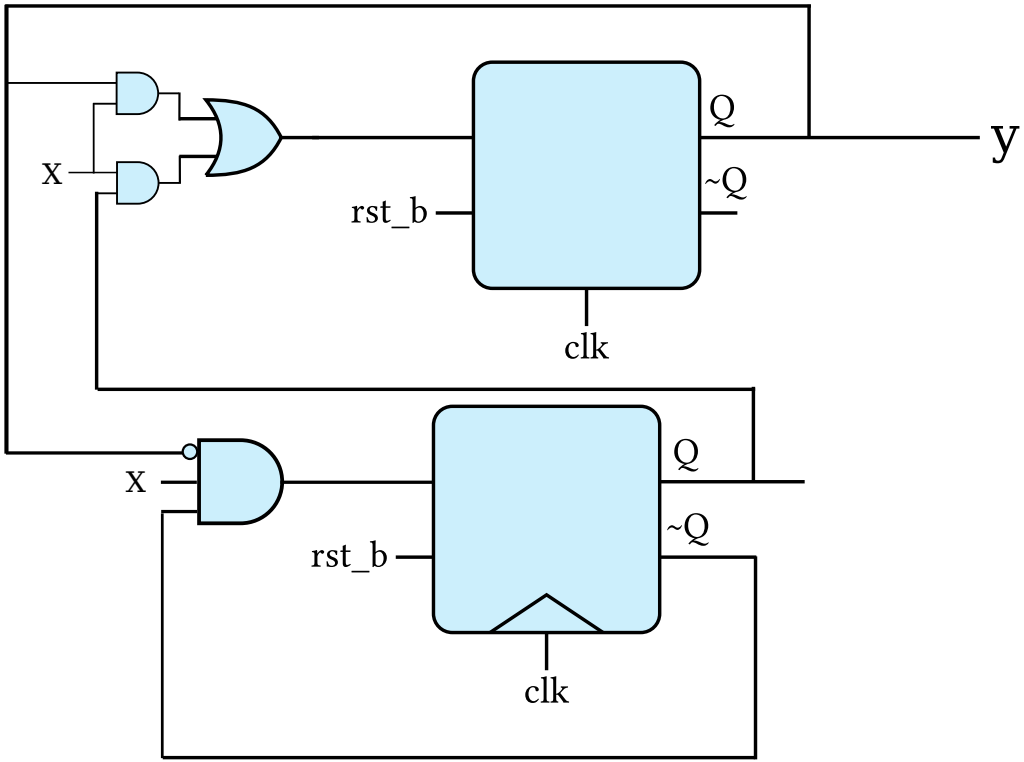
"11" Sequence detector - Moore



"11" Sequence detector - Mealy



"11" Sequence detector - Moore

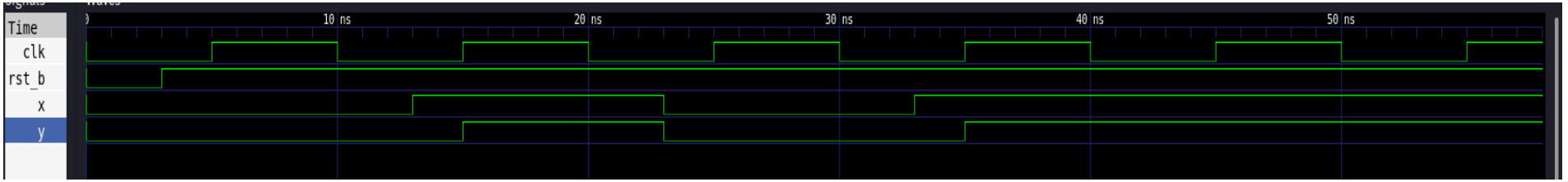


verilog

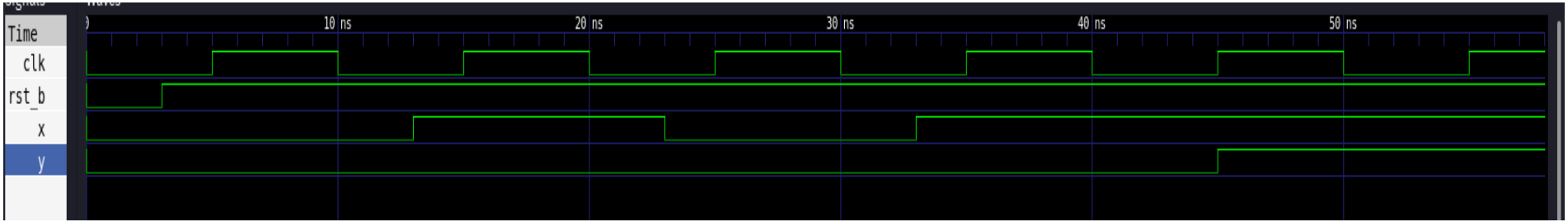
```verilog
module moore_seq(
    input x,
    input clk,
    input rst_b,
    output y
);

    localparam S0= 2'b00;
    localparam S1= 2'b01;
    localparam S2= 2'b10;

    reg [1:0] NextState, PresentState;

    always @(posedge clk or negedge rst_b) begin
        if(!rst_b) PresentState <= S0;
        else PresentState <= NextState;
    end

    always @(x,PresentState) begin
        case(PresentState)
        S0: NextState = (x)? S1:S0;
        S1: NextState = (x)? S2:S0;
        S2: NextState = (x)? S2:S0;
        endcase
    end

    assign y=(PresentState==S2);

endmodule
```

verilog

```verilog
module mealy_seq(
    input x,
    input clk,
    input rst_b,
    output y
);

    localparam S0= 1'b0;
    localparam S1= 1'b1;

    reg NextState, PresentState;

    always @(posedge clk or negedge rst_b) begin
        if(!rst_b) PresentState <= S0;
        else PresentState <= NextState;
    end

    always @(x,PresentState) begin
        case(PresentState)
        S0: NextState = (x)? S1:S0;
        S1: NextState = (x)? S1:S0;
        endcase
    end

    assign y = (PresentState == S1) & (x==1);

endmodule
```

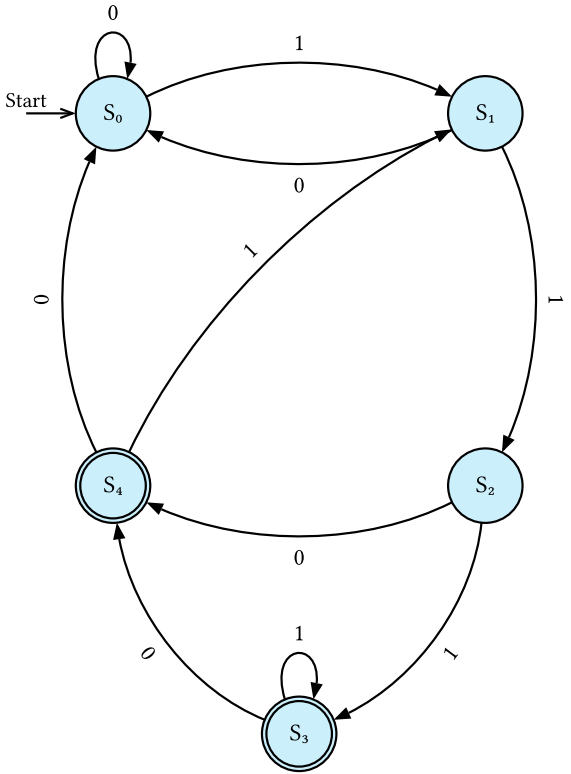


Mealy Output Waveform

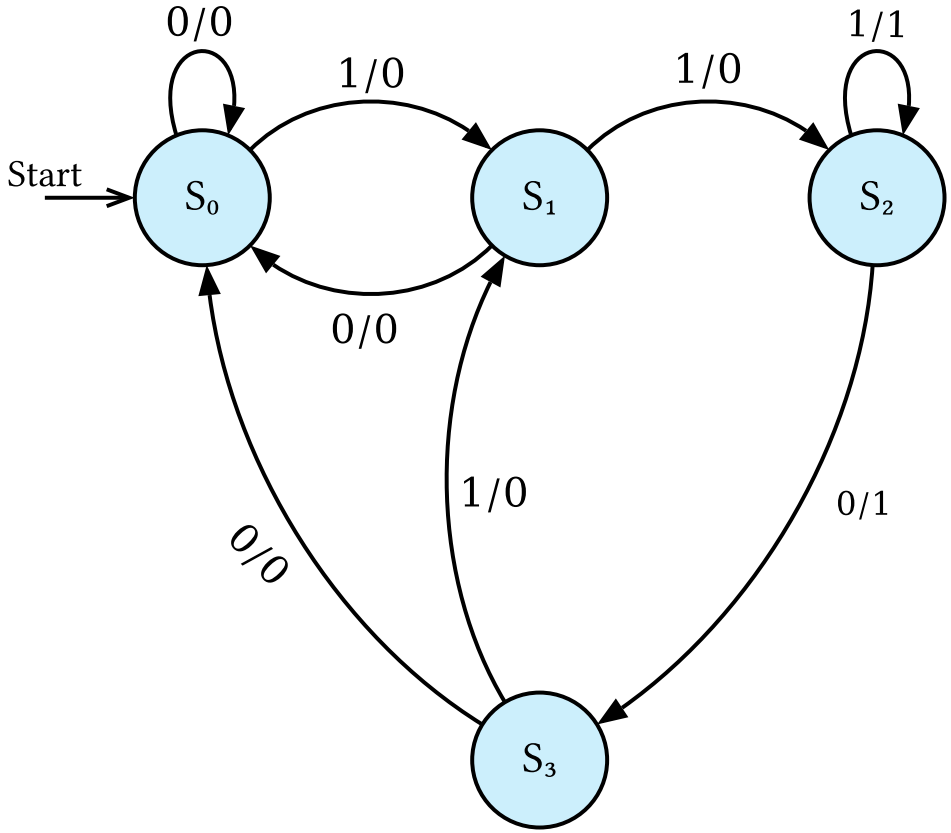


Moore Output Waveform

Complex FSM "110/111" detector - Moore



Complex FSM "110/111" detector -Mealy



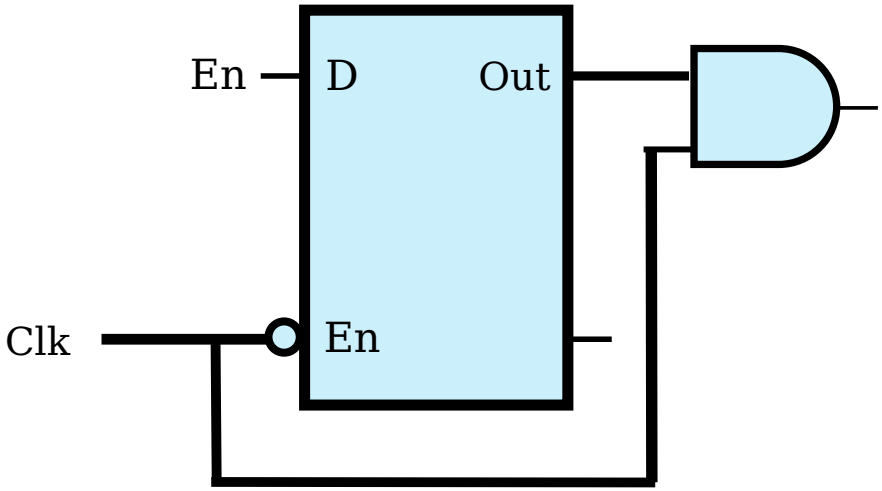
State Encodings

-- Binary Encoding

-- One-Hot Encoding

-- Gray Encoding

Clock Gating using Latches



Clock Gating using Latches

verilog

```verilog
module clk_gate(
    input clk,
    input en,
    output clk_gated
);

    reg out;

    always @(*) begin
        if(!clk) out = en;
    end

    assign clk_gated = (out & clk);

endmodule
```