Rui (Rick) Xie

Ph.D. Candidate
Electrical, Computer, and Systems Engineering Department
Rensselaer Polytechnic Institute

xier2@rpi.edu
+1-518-918-5886
rickxie.cn

Research Statement

M research focuses on **optimizing memory architectures**, primarily DRAM and SSDs, to enhance hardware performance and software efficiency. I explore solutions in data processing and AI, aiming to contribute to more efficient and sustainable computing systems.

Education

- **Rensselaer Polytechnic Institute** — Troy, US
  Ph.D. Candidate, Computer & Systems Engineering, Advisor: Tong Zhang — *Aug. 2022 – Present*
- **Southern University of Science and Technology** — Shenzhen, CN
  B.Eng with Honors, Microelectronics Science and Engineering — *Aug. 2018 – Jun. 2022*

Publications

Under review

2024 **Rui Xie**, Linsen Ma, Alex Zhong, Feng Chen, Tong Zhang, "ZipCache: A Hybrid-DRAM/SSD Cache with Built-in Transparent Compression"

Conference

2023 Linsen Ma, **Rui Xie**, Tong Zhang, "ZipKV: In-Memory Key-Value Store with Built-In Data Compression", International Symposium on Memory Management (ISMM)

2022 Ziyi Guan, Wenyong Zhou, Yuan Ren, **Rui Xie**, Hao Yu, Ngai Wong, "A Hardware-Aware Neural Architecture Search Pareto Front Exploration for In-Memory Computing," in Proc. IEEE Int. Conf. Solid-State and Integrated Circuit Technology (ICSICT)

2021 **Rui Xie**, Mingyang Song, Junzhuo Zhou, Jie Mei, Quan Chen, A Fast Method for Steady-State Memristor Crossbar Array Circuit Simulation, IEEE International Conference on Integrated Circuits Technologies and Applications

Skills

Programming Languages: C++, Python, Java, Verilog HDL

Selected Projects

- **Graceful implementation of AI via importance-proportional dynamic model quantization**:
  - *Supporter: IBM*
  - Engineered solutions for in-memory AI model storage and dynamic data format/precision conversion, achieving proportional energy consumption and reduced transfer latency.
- **B+ tree based hybrid memory/flash caching with in-memory compression**:
  - Proposed a B+ tree based DRAM/SSD cache architecture with integrated data compression.
  - Demonstrated up to 72.4% higher throughput and 42.4% lower latency, with notable reduction in SSD write amplification.
- **Enhanced key-value store with in-memory compression**:
  - Addressed challenges in read/write amplification and developed a solution to reduce compression-induced speed performance degradation, enhancing system efficiency.
  - Demonstrated improvements in query latency and throughput, achieving up to 68% reduction and up to 3.8× increase respectively.
- **Steady-State Memristor Crossbar Array Circuit Simulation, Apr. 2021 - Jul. 2021**:
  - Exploited the structural regularity of MCAs to develop efficient preconditioner and rethink the inverse process.

Honors and Awards

2022 Excellent Graduate in Southern University of Science and Technology

2021 First Class of the Merit Student Scholarship

Peer Review Experience

ISCAS (2022, 2023)