Rui (Rick) Xie

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(Updated Jan. 2023)

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Education

- **Ph.D. Student, Computer System Engineering** — Troy, NY, United States
  Rensselaer Polytechnic Institute, Advisor: Tong Zhang — *Aug. 2022 – Present*
- **B.Eng with Honors, Microelectronics Science and Engineering** — Shenzhen, China
  Southern University of Science and Technology, Advisor: Quan Chen — *Aug. 2018 – Jun. 2022*

Experience

- **Engineer Intern** — Shenzhen, China
  BTD Technologies — *Dec. 2021 – Jun. 2022*
  - **Interface development of BTDSim**: Improved the functions of the interface, Connected to *Virtuoso*
- **Research Intern** — Remote
  The University of Hong Kong (Host: Zhongrui Wang) — *Jun. 2021 – Aug. 2021*
  - **Feedback States Convergence Adjustment of Memristor**: Fine-tuned the memristor device to I-V curve
  - ***ARC One* Implementation**: Developed converge method of memristor device on *ArC ONE* and Keysights B1500A
- **Visiting Student, Oxford International Study Abroad Programme** — Oxford, United Kingdom
  University of Oxford — *Jul. 2019 – Aug. 2019*
  - **Big Data and Social Media**: R Programming and Data Analysis
  - **University, Tutorial System and Interdisciplinary**: Research on Mass Psychology and Higher Education

Research Interests

- **Computer System Design**
  Storage and Cache System
  - **B-tree Based Cache System with Data Compression in DRAM**:
    1. DRAM/SSD-based caching systems play an important role in modern IT infrastructure
    2. DRAM accounts for a significant (and increasing) portion of system TCO
    3. NAND flash memory has limited (and decreasing) P/E cycling endurance

Honors and Awards

- Excellent Graduate in Southern University of Science and Technology, Jun. 2022
- Graduation with Honor: College Graduate Excellence Award, Jun. 2022
- First Class of the Merit Student Scholarship, Sep. 2021
- Outstanding Cadre Award of Zhicheng College, May. 2021
- First Prize of College Student Innovation and Entrepreneurship Training Program, Mar. 2021
- Second Class of the Merit Student Scholarship, Sep. 2020
- Third Prize of China College IC Competition in Southern China, Jul. 2020
- Third Class of the Merit Student Scholarship, Sep. 2019

Service

- Alumni Mentor of Zhicheng College at SUSTech, 2022

Skills

- **Programming Languages**: C++, C, Python, Java, Verilog HDL, Scala
- **Software**: Virtuoso, Quartus, ModelSim, Icepack, Silvaco, LTSPICE, Comsol, SolidWorks, AutoCAD, MATLAB

Publications

1. Ziyi Guan, Wenyong Zhou, Yuan Ren, **Rui Xie**, Hao Yu, Ngai Wong, "A Hardware-Aware Neural Architecture Search Pareto Front Exploration for In-Memory Computing," in Proc. 2022 IEEE 16th Int. Conf. Solid-State and Integrated Circuit Technology (ICSICT), Oct 2022 (invited paper)
2. Yuan Ren, Wenyong Zhou, Ziyi Guan, **Rui Xie**, Quan Chen, Hao Yu, Ngai Wong, XMAS: An Efficient Customizable Flow for Crossbarred-Memristor Architecture Search, 59th Design Automation Conference Engineering Track
3. **Rui Xie**, Mingyang Song, Junzhuo Zhou, Jie Mei, Quan Chen, A Fast Method for Steady-State Memristor Crossbar Array Circuit Simulation, 2021 IEEE International Conference on Integrated Circuits Technologies and Applications
4. Quan Chen, Dayi Fan, **Rui Xie**, Mingyang Song, Construction and optimization of neural networks for memristor arrays based on circuit simulation. CN 202110673101.

Projects

- **RRAM (Resistive RAM) Non-Ideal Simulation, Jun. 2021 - Aug. 2021**:
  1. Designed the multiply-add method
  2. Developed the simulator by noise model and non-linearity
- **Neural architectural search for RRAM-based AI accelerator, Aug. 2021**:
  1. An organized network with One-Shot NAS by NNI (An open source AutoML toolkit by Microsoft)
  2. For EDAthon 2021 project, an competition held by CEDA Hong Kong with graduate students
  3. Ranked **7/24** in the EDAthon 2021 with graduate participants
- **Steady-State Memristor Crossbar Array (MCA) Circuit Simulation, Apr. 2021 - Jul. 2021**:
  1. Exploited the structural regularity of MCAs to develop preconditioner
  2. Designed the inverse process by Kronecker product and block matrix formula
  3. Experimented the numerical verification
- **A design of** 4×4 **Bits array multiplier based on virtuoso, Nov. 2020 - Dec. 2020**:
  1. A 4×4 array multiplier of $180nm$ technique on Virtuoso of Cadence with special carry method
  2. $10\times$ less area consumption than common design
  3. Designed with layered structure and organized locating and wiring
- **TPU development based on RISC-V and Chisel based on Scala, Sep. 2020 - Dec. 2020**:
  1. A Google TPU structure based on systolic array using Chisel
  2. Redesigned look up table multiplier
  3. VGG-16 network test, $10\times$ less energy consumption than common structure
- **An Optimization Algorithm for Demosaicing Using DE-1 FPGA and Camera with LCD Screen Display, Oct. 2020 - Nov. 2020**:
  1. Crafted parallel demosaic algorithm, with median filtering and gamma correction
  2. Designed pipeline structure to store 4×4 pixel data for speed up
  3. Deployed on DE1 FPGA, 5CSEMA5F31C6
- **Surrogate Modeling of Electro-Thermal Simulation, Sep. 2020 - Nov. 2020**:
  1. Simulated the process of SiC sandwich devices with *Ansys Icepak*
  2. Designed the surrogate model
- **A LSTM-based Campus Bus Travel Time Prediction Software Development, Mar. 2020 - Jun. 2020**:
  1. LSTM based prediction method, displaying congestion level and arrival time
  2. Friendly UI and Deployed on WeChat Program, cooperated with SUSTech Campus Bus
  3. Won the first prize of 2021 School of Microelectronics Innovation Competition
- **SOBEL Operator Edge Detection on FPGA Based on ARM Architecture, Mar. 2020 - May. 2020**:
  1. Customized architecture by CMSDK of Arm Cortex-M3 DesignStart Eval IP
  2. Float-avoid operations by lookup tables, simplify the square and multiplication operations
  3. Pixel thresholds tests to ensure accuracy of real-time display