

# MC74HC4851A, MC74HC4852A

## Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

### Automotive Customized

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply voltage range.

The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

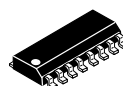
#### Features

- Injection Current Cross-Coupling Less than 1 mV/mA (See Figure 10)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- In Compliance With the Requirements of JEDEC Standard No. 7 A
- Chip Complexity: 154 FETs or 36 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

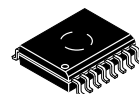


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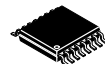
[www.onsemi.com](http://www.onsemi.com)



SOIC-16  
D SUFFIX  
CASE 751B



SOIC-16 WIDE  
DW SUFFIX  
CASE 751G

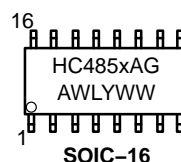


TSSOP-16  
DT SUFFIX  
CASE 948F

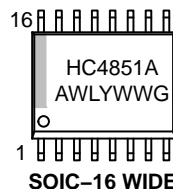


QFN16  
MN SUFFIX  
CASE 485AW

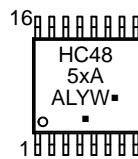
#### MARKING DIAGRAMS



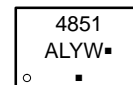
SOIC-16



SOIC-16 WIDE



TSSOP-16



QFN16\*

\*V4851 marking used for  
NLV74HC4851AMN1TWG

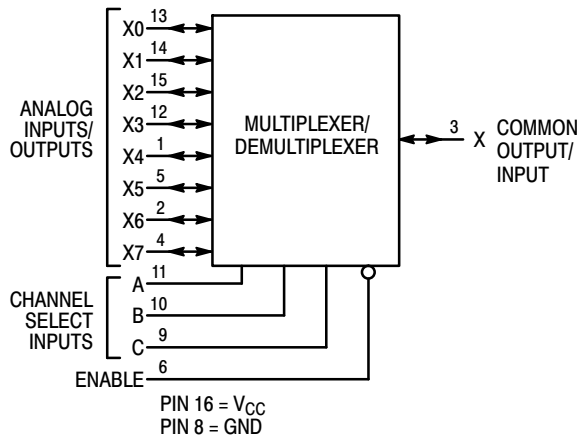
x = 1 or 2  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

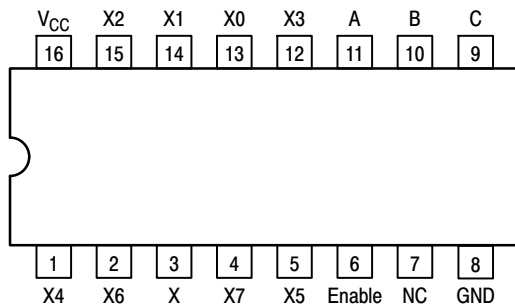
## MC74HC4851A, MC74HC4852A



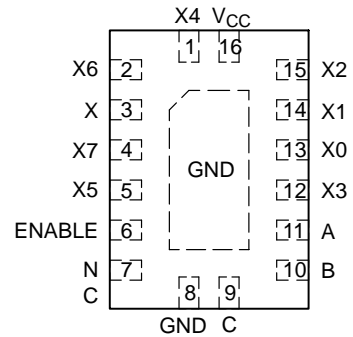
**Figure 1. MC74HC4851A Logic Diagram  
Single-Pole, 8-Position Plus Common Off**

**FUNCTION TABLE – MC74HC4851A**

Control Inputs				ON Channels
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE



**Figure 2. MC74HC4851A 16-Lead Pinout (Top View)**

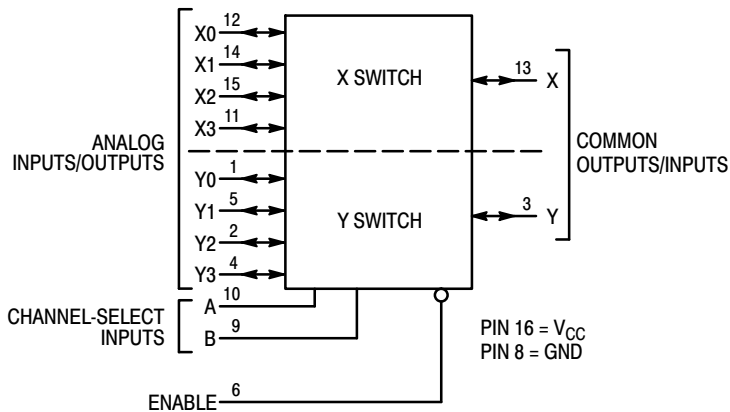


**Figure 3. MC74HC4851A QFN Pinout**

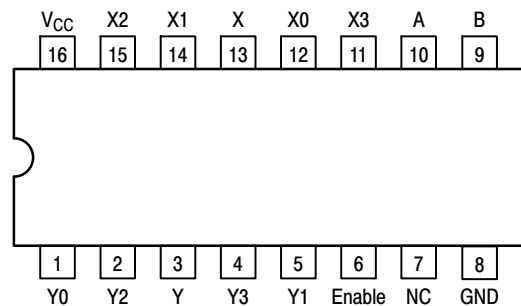
**FUNCTION TABLE – MC74HC4852A**

Control Inputs				
Enable	Select			
	B	A	ON Channels	
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care



**Figure 4. MC74HC4852A Logic Diagram  
Double-Pole, 4-Position Plus Common Off**



**Figure 5. MC74HC4852A 16-Lead Pinout (Top View)**

# MC74HC4851A, MC74HC4852A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Any Pin) (Referenced to GND)	−0.5 to $V_{CC} + 0.5$	V
I	DC Current, Into or Out of Any Pin	±25	mA
$P_D$	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature Range	−65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: −7 mW/°C from 65° to 125°C

TSSOP Package: −6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}$	DC Input Voltage (Any Pin) (Referenced to GND)	GND	$V_{CC}$	V
$V_{IO}^*$	Static or Dynamic Voltage Across Switch	0.0	1.2	V
$T_A$	Operating Temperature Range, All Package Types	−55	+125	°C
$t_r, t_f$	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

\*For voltage drops across switch greater than 1.2 V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = GND$ , Except Where Noted

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
$V_{IL}$	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
$I_{in}$	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	$V_{in} = V_{CC} \text{ or } GND$	6.0	±0.1	±1.0	±1.0	μA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)} = V_{CC} \text{ or } GND$ $V_{in(analog)} = GND$	6.0	2	20	40	μA

# MC74HC4851A, MC74HC4852A

## DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V <sub>CC</sub>	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
R <sub>on</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IS</sub> = V <sub>CC</sub> to GND (Note 1); I <sub>S</sub> ≤ 2.0 mA (Note 2)	2.0	1700	1750	1800	Ω
			3.0	1100	1200	1300	
			4.5	550	650	750	
			6.0	400	500	600	
ΔR <sub>on</sub>	Delta "ON" Resistance	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IS</sub> = V <sub>CC</sub> /2 (Note 1); I <sub>S</sub> ≤ 2.0 mA (Note 2)	2.0	300	400	500	Ω
			3.0	160	200	240	
			4.5	80	100	120	
			6.0	60	80	100	
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel Common Channel	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±0.1	±0.1	μA
				±0.1	±0.1	±0.1	
I <sub>on</sub>	Maximum On-Channel Leakage Channel-to-Channel	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±0.1	±0.1	μA

1. V<sub>IS</sub> is the input voltage of an analog I/O pin.

2. I<sub>S</sub> is the current flowing in or out of analog I/O pin.

## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub>	-55 to 25°C	≤85°C	≤125°C	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay, Analog Input to Analog Output	2.0	160	180	200	ns
		3.0	80	90	100	
		4.5	40	45	50	
		6.0	30	35	40	
t <sub>PHL</sub> , t <sub>PHZ,PZH</sub> , t <sub>PLH</sub> , t <sub>PLZ,PZL</sub>	Maximum Propagation Delay, Enable or Channel-Select to Analog Output	2.0	260	280	300	ns
		3.0	160	180	200	
		4.5	80	90	100	
		6.0	78	80	80	
C <sub>in</sub>	Maximum Input Capacitance (All Switches Off) (All Switches Off)	Digital Pins	10	10	10	pF
		Any Single Analog Pin	35	35	35	
		Common Analog Pin	40	40	40	
C <sub>PD</sub>	Power Dissipation Capacitance	Typical	5.0	20		pF

## INJECTION CURRENT COUPLING SPECIFICATIONS (V<sub>CC</sub> = 5V, T<sub>A</sub> = -55°C to +125°C)

Symbol	Parameter	Condition	Typ	Max	Unit
VΔ <sub>out</sub>	Maximum Shift of Output Voltage of Enabled Analog Channel	I <sub>in</sub> * ≤ 1 mA, R <sub>S</sub> ≤ 3.9 kΩ	0.1	1.0	mV
		I <sub>in</sub> * ≤ 10 mA, R <sub>S</sub> ≤ 3.9 kΩ	1.0	5.0	
		I <sub>in</sub> * ≤ 1 mA, R <sub>S</sub> ≤ 20 kΩ	0.5	2.0	
		I <sub>in</sub> * ≤ 10 mA, R <sub>S</sub> ≤ 20 kΩ	5.0	20	

\* I<sub>in</sub> = Total current injected into all disabled channels.

# MC74HC4851A, MC74HC4852A

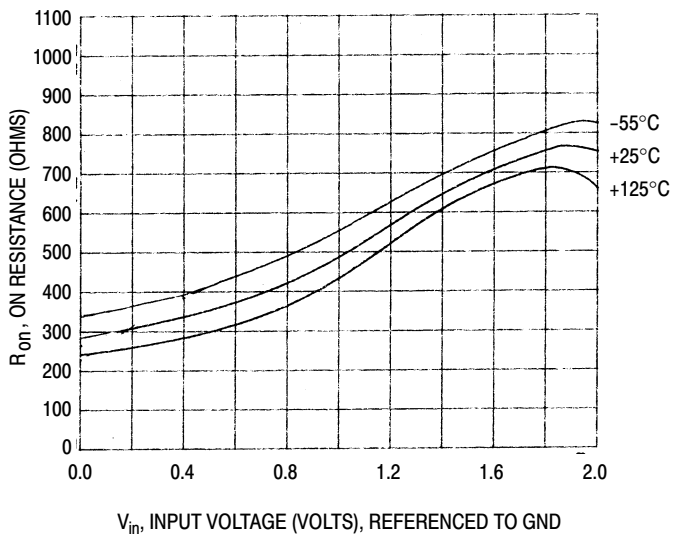


Figure 6. Typical On Resistance  $V_{CC} = 2V$

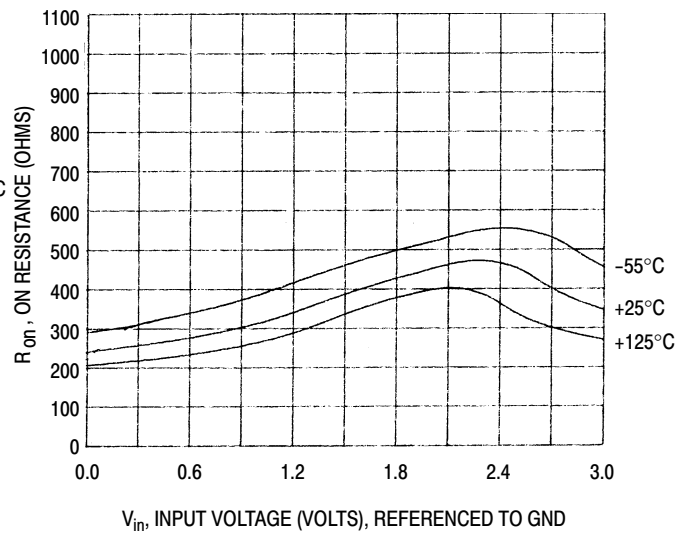


Figure 7. Typical On Resistance  $V_{CC} = 3V$

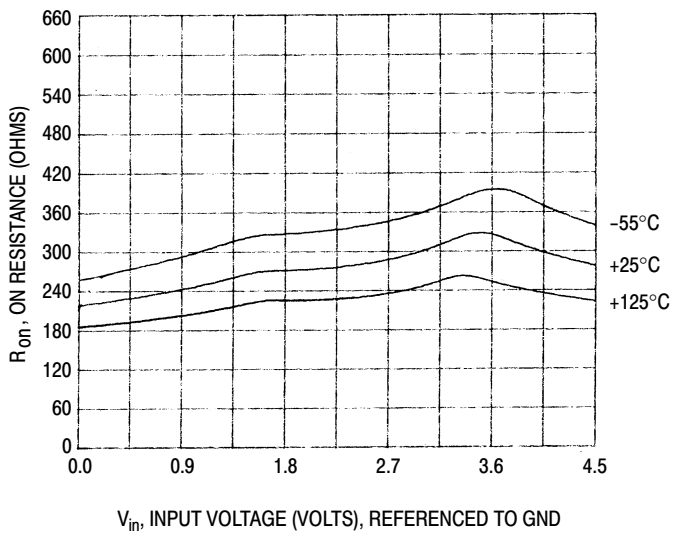


Figure 8. Typical On Resistance  $V_{CC} = 4.5V$

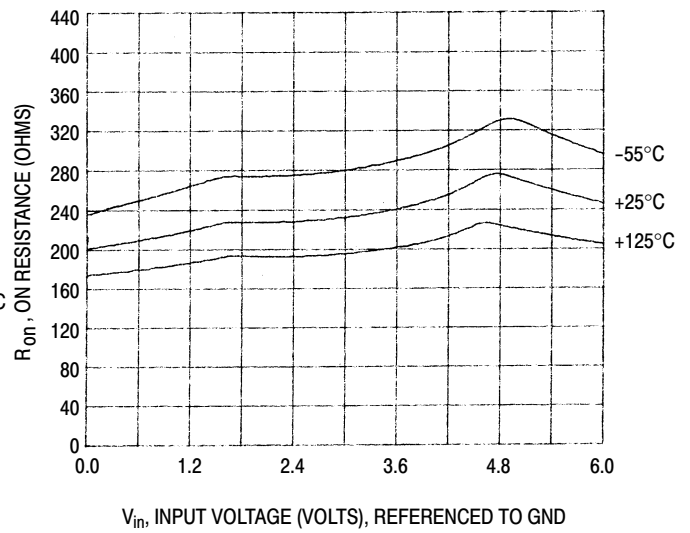
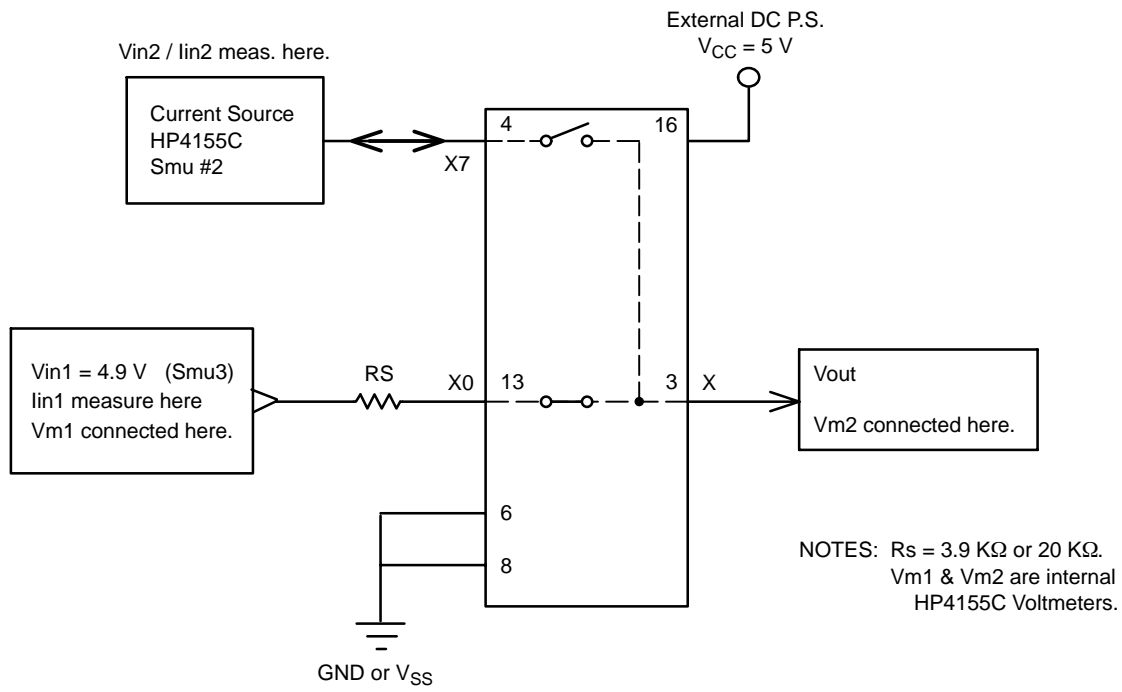


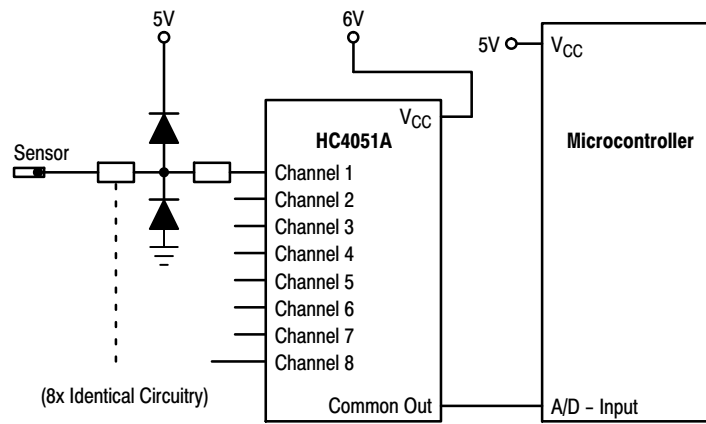
Figure 9. Typical On Resistance  $V_{CC} = 6V$

# MC74HC4851A, MC74HC4852A



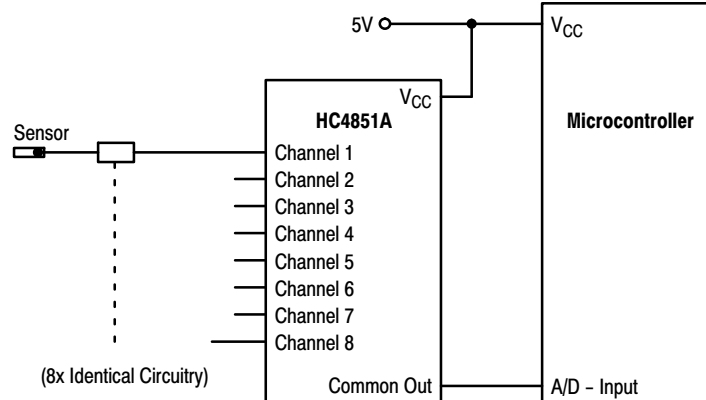
**Figure 10. Injection Current Coupling Specification**

## MC74HC4851A, MC74HC4852A



**Figure 11. Actual Technology**

Requires 32 passive components and one extra 6V regulator to suppress injection current into a standard HC4051 multiplexer



**Figure 12. MC74HC4851A Solution**

Solution by applying the HC4851A multiplexer

# MC74HC4851A, MC74HC4852A

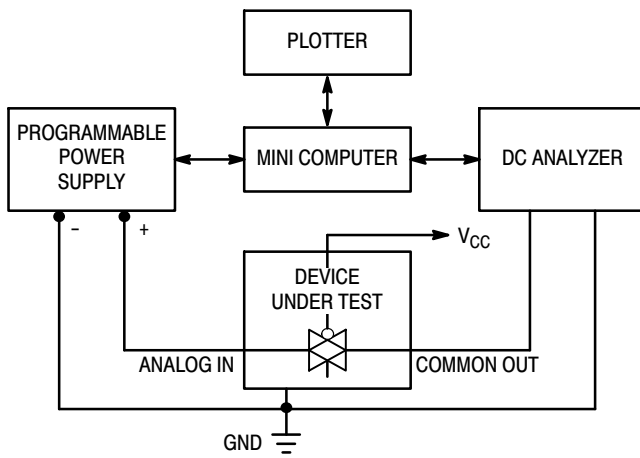


Figure 13. On Resistance Test Set-Up

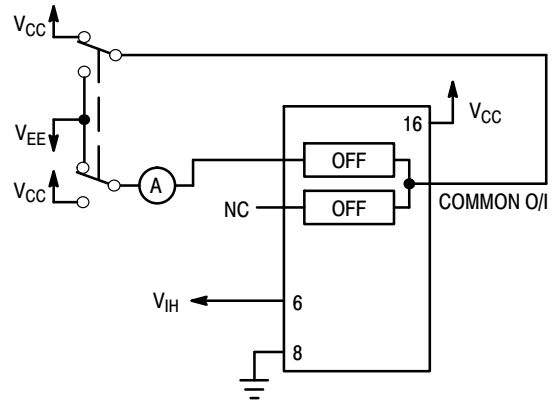


Figure 14. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

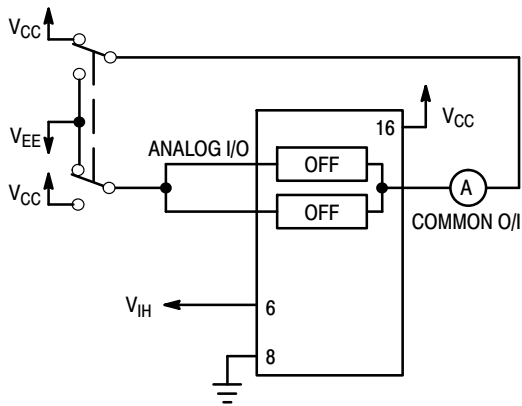


Figure 15. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

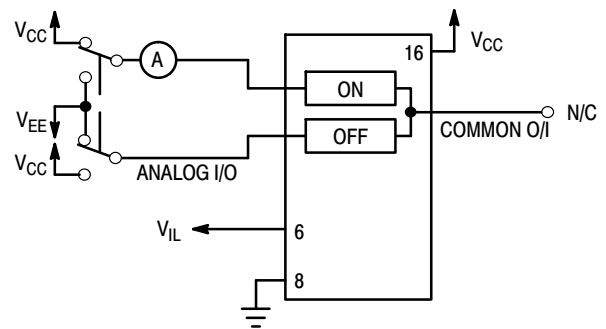


Figure 16. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

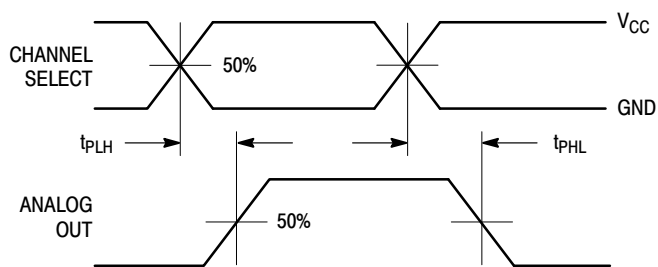
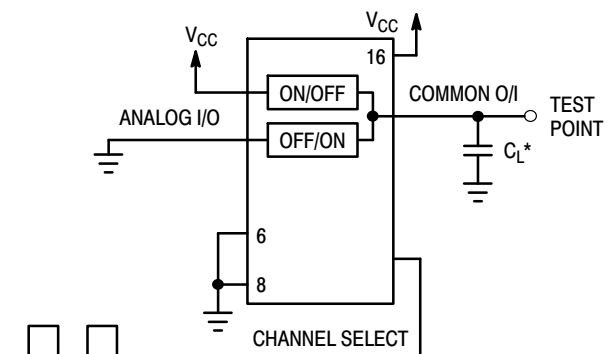


Figure 17. Propagation Delays, Channel Select to Analog Out

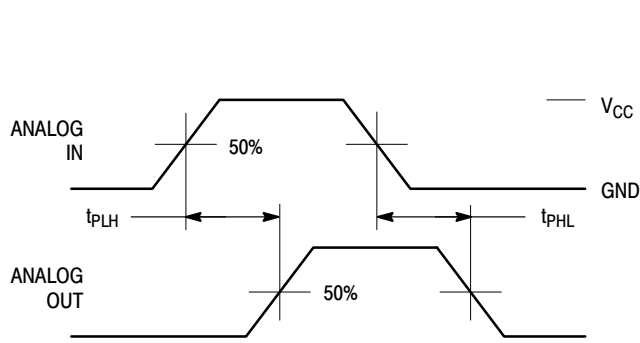


\*Includes all probe and jig capacitance

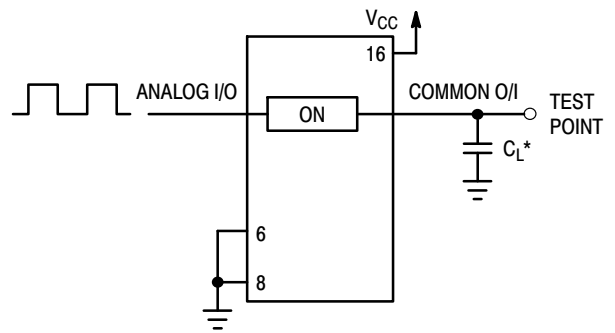
Figure 18. Propagation Delay, Test Set-Up Channel Select to Analog Out



# MC74HC4851A, MC74HC4852A

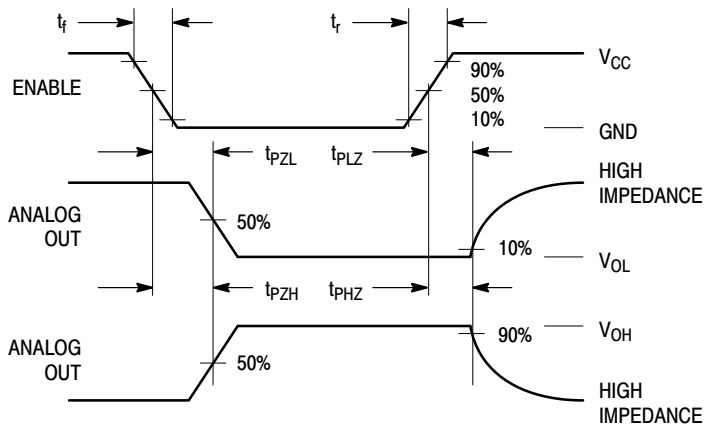


**Figure 19. Propagation Delays, Analog In to Analog Out**

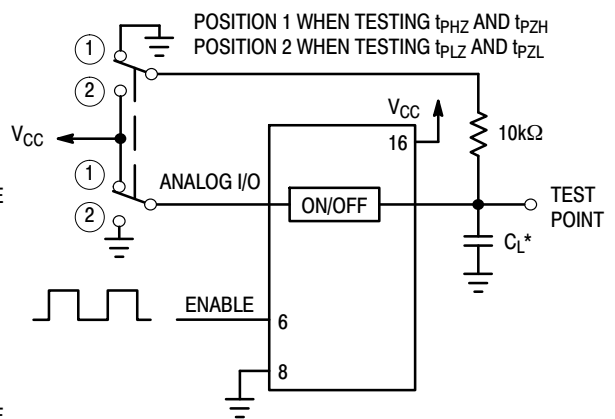


\*Includes all probe and jig capacitance

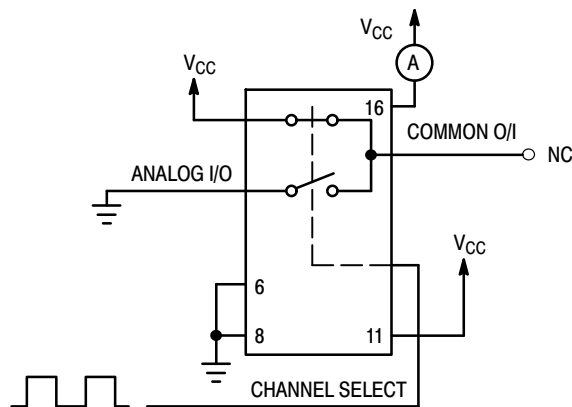
**Figure 20. Propagation Delay, Test Set-Up Analog In to Analog Out**



**Figure 21. Propagation Delays, Enable to Analog Out**

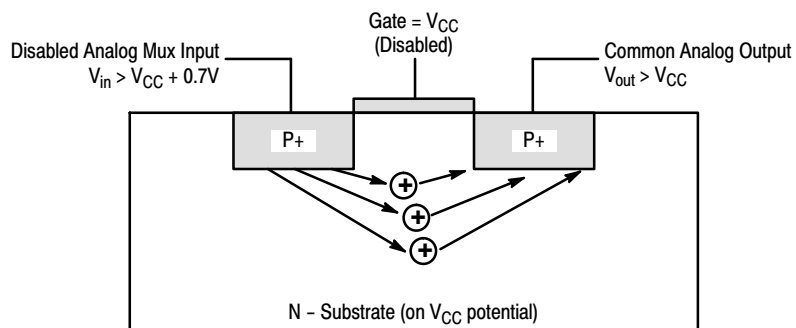


**Figure 22. Propagation Delay, Test Set-Up Enable to Analog Out**

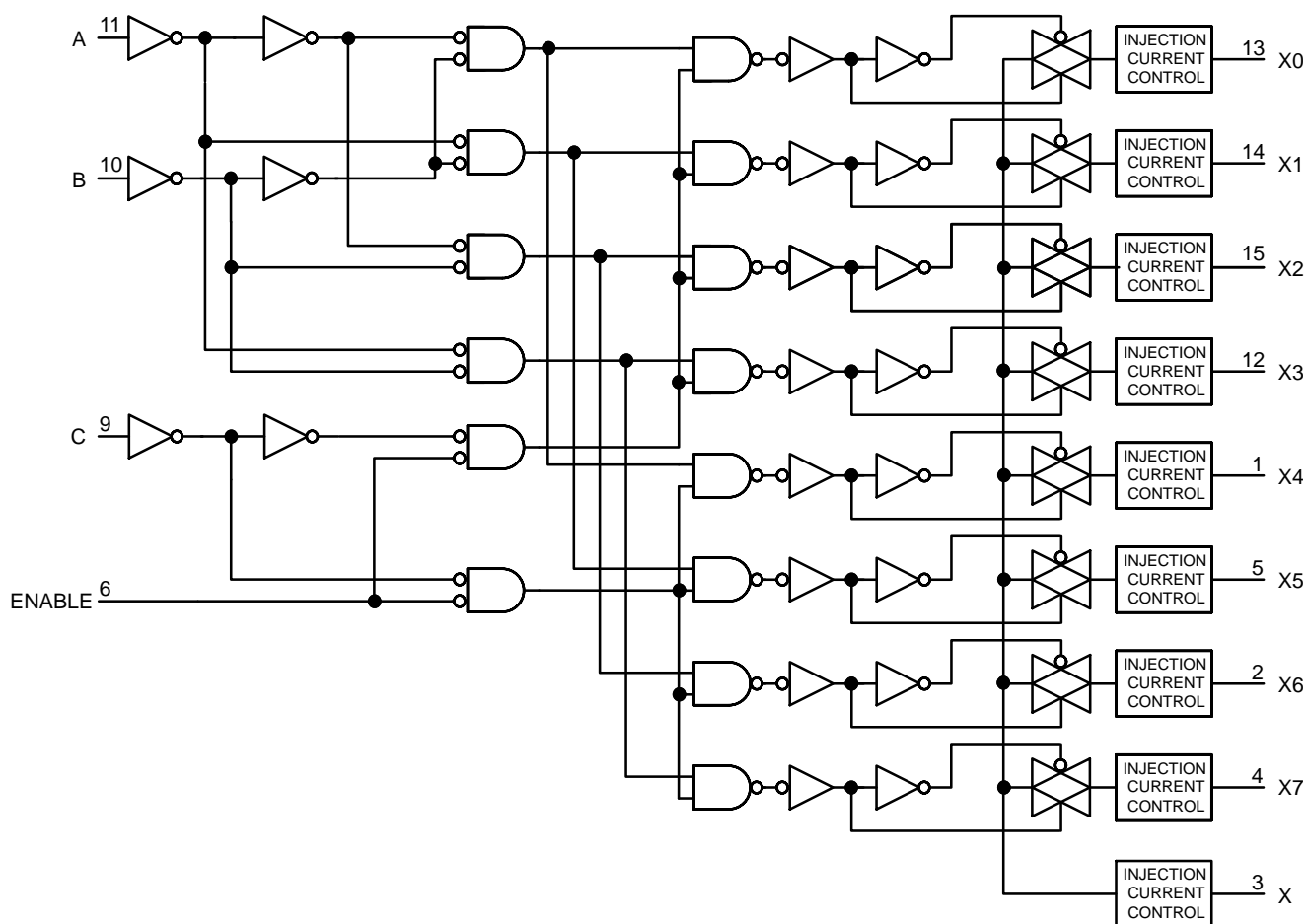


**Figure 23. Power Dissipation Capacitance, Test Set-Up**

## MC74HC4851A, MC74HC4852A



**Figure 24. Diagram of Bipolar Coupling Mechanism**  
Appears if  $V_{in}$  exceeds  $V_{CC}$ , driving injection current into the substrate



**Figure 25. Function Diagram, HC4851A**

# MC74HC4851A, MC74HC4852A

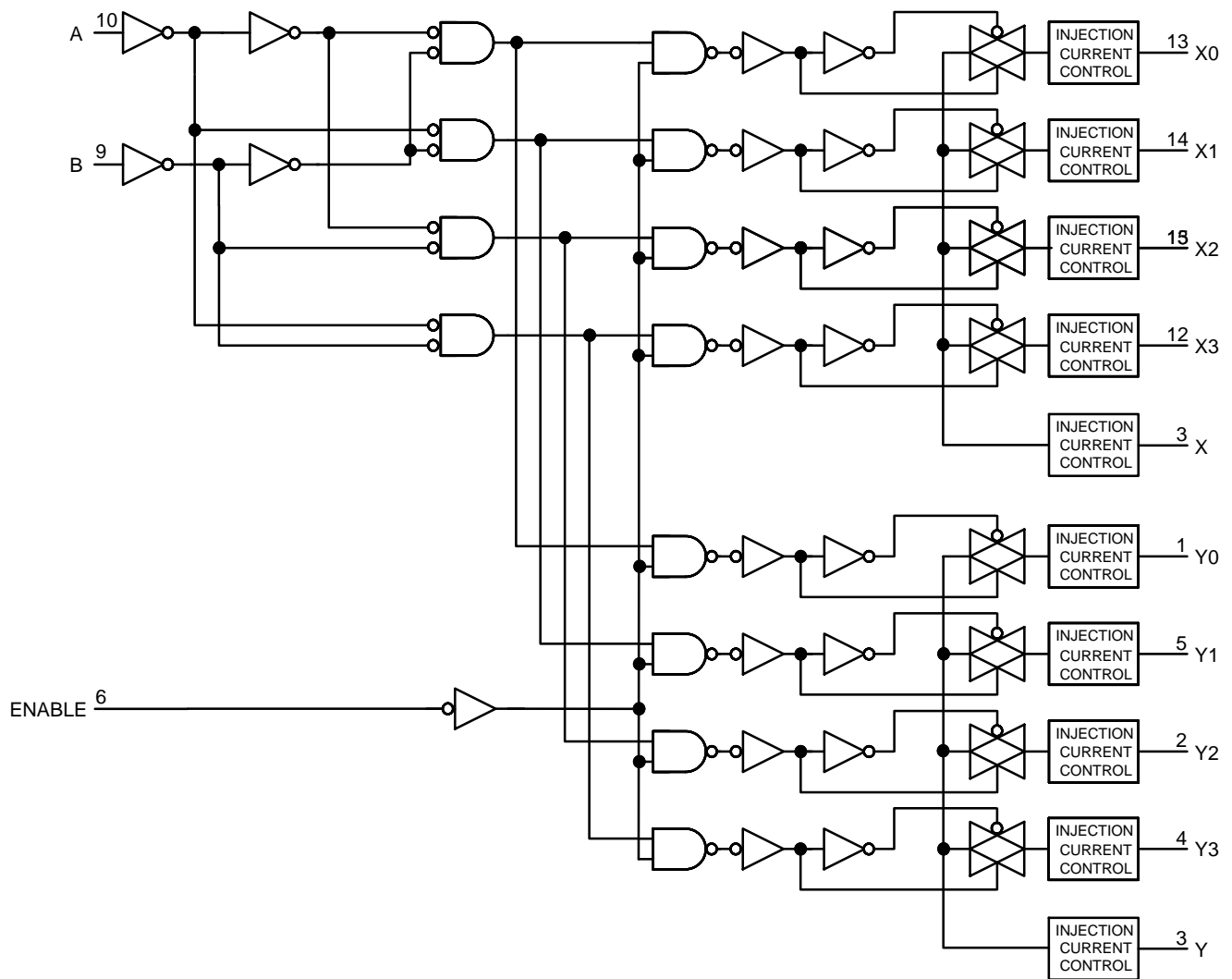


Figure 26. Function Diagram, HC4852A

# MC74HC4851A, MC74HC4852A

## ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4851ADG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74HC4851ADR2G		2500 Units / Tape & Reel
NLVHC4851ADR2G*		2500 Units / Tape & Reel
MC74HC4851ADTR2G	TSSOP–16 (Pb–Free)	2500 Units / Tape & Reel
NLVHC4851ADTR2G*		
MC74HC4851ADWR2G	SOIC–16 WIDE (Pb–Free)	1000 Units / Tape & Reel
NLVHC4851ADWR2G*		
NLV74HC4851AMNTWG*#	QFN16 (Pb–Free)	3000 Units / Tape & Reel
NLV74HC4851AMN1TWG*#		3000 Units / Tape & Reel

MC74HC4852ADG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74HC4852ADR2G		2500 Units / Tape & Reel
NLV74HC4852ADR2G*		2500 Units / Tape & Reel
MC74HC4852ADTR2G	TSSOP–16 (Pb–Free)	2500 Units / Tape & Reel
NLVHC4852ADTR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

#MN suffix is with pull–back lead, MN1 is without pull–back lead. Refer to 'Detail A' of case outline on page 16.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

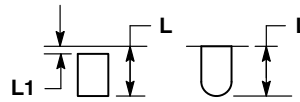
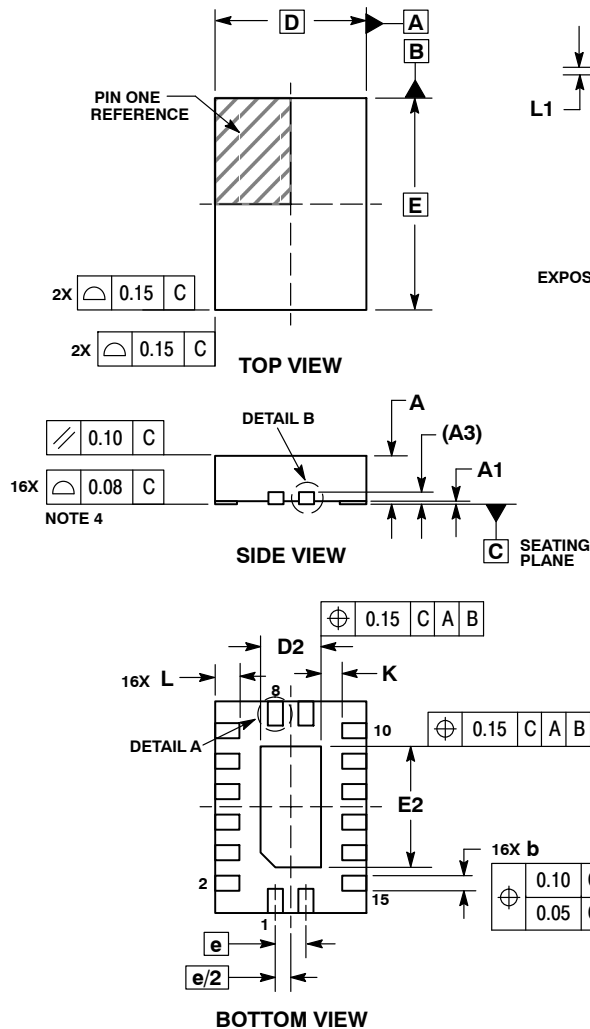
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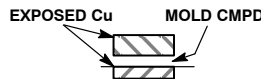
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**QFN16, 2.5x3.5, 0.5P**  
CASE 485AW-01  
ISSUE O

DATE 11 DEC 2008



**DETAIL A**  
ALTERNATE TERMINAL  
CONSTRUCTIONS



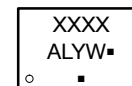
**DETAIL B**  
ALTERNATE  
CONSTRUCTIONS

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

### GENERIC MARKING DIAGRAM\*

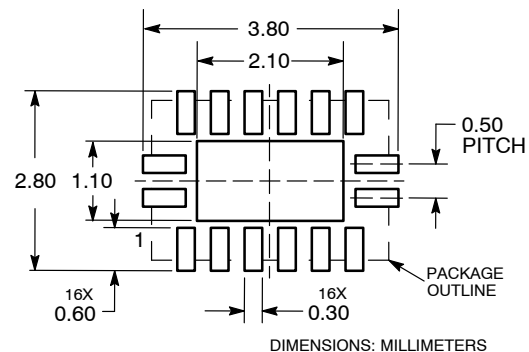


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>QFN16, 2.5X3.5, 0.5P</b>	<b>PAGE 1 OF 1</b>

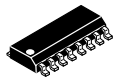
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

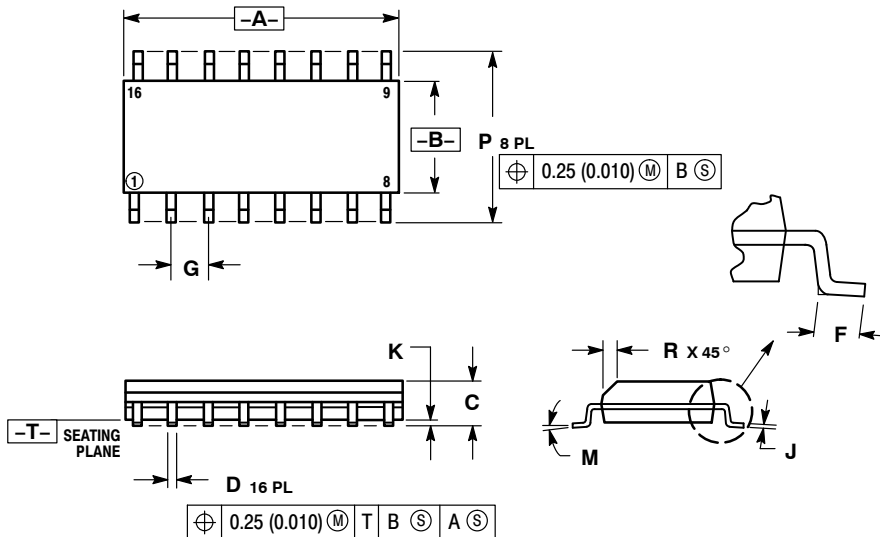
ON



SCALE 1:1

### SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



#### NOTES:

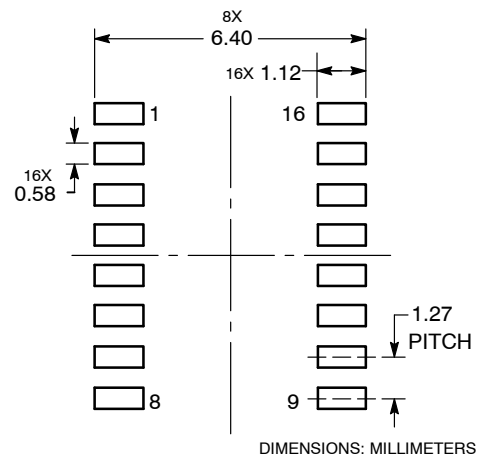
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	0.40	1.25	0.016	0.049
F	1.27 BSC		0.050 BSC	
G	0.19	0.25	0.008	0.009
H	0.10	0.25	0.004	0.009
I	0°	7°	0°	7°
J	5.80	6.20	0.229	0.244
K	0.25	0.50	0.010	0.019

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1. COLLECTOR	PIN 1. CATHODE	PIN 1. COLLECTOR, DYE #1	PIN 1. COLLECTOR, DYE #1
2. BASE	2. ANODE	2. BASE, #1	2. COLLECTOR, #1
3. EMITTER	3. NO CONNECTION	3. EMITTER, #1	3. COLLECTOR, #2
4. NO CONNECTION	4. CATHODE	4. COLLECTOR, #1	4. COLLECTOR, #2
5. EMITTER	5. CATHODE	5. COLLECTOR, #2	5. COLLECTOR, #3
6. BASE	6. NO CONNECTION	6. BASE, #2	6. COLLECTOR, #3
7. COLLECTOR	7. ANODE	7. EMITTER, #2	7. COLLECTOR, #4
8. COLLECTOR	8. CATHODE	8. COLLECTOR, #2	8. COLLECTOR, #4
9. BASE	9. CATHODE	9. COLLECTOR, #3	9. BASE, #4
10. EMITTER	10. ANODE	10. BASE, #3	10. EMITTER, #4
11. NO CONNECTION	11. NO CONNECTION	11. EMITTER, #3	11. BASE, #3
12. EMITTER	12. CATHODE	12. COLLECTOR, #3	12. EMITTER, #3
13. BASE	13. CATHODE	13. COLLECTOR, #4	13. BASE, #2
14. COLLECTOR	14. NO CONNECTION	14. BASE, #4	14. EMITTER, #2
15. EMITTER	15. ANODE	15. EMITTER, #4	15. BASE, #1
16. COLLECTOR	16. CATHODE	16. COLLECTOR, #4	16. EMITTER, #1

STYLE 5:	STYLE 6:	STYLE 7:
PIN 1. DRAIN, DYE #1	PIN 1. CATHODE	PIN 1. SOURCE N-CH
2. DRAIN, #1	2. CATHODE	2. COMMON DRAIN (OUTPUT)
3. DRAIN, #2	3. CATHODE	3. COMMON DRAIN (OUTPUT)
4. DRAIN, #2	4. CATHODE	4. GATE P-CH
5. DRAIN, #3	5. CATHODE	5. COMMON DRAIN (OUTPUT)
6. DRAIN, #3	6. CATHODE	6. COMMON DRAIN (OUTPUT)
7. DRAIN, #4	7. CATHODE	7. COMMON DRAIN (OUTPUT)
8. DRAIN, #4	8. CATHODE	8. SOURCE P-CH
9. GATE, #4	9. ANODE	9. SOURCE P-CH
10. SOURCE, #4	10. ANODE	10. COMMON DRAIN (OUTPUT)
11. GATE, #3	11. ANODE	11. COMMON DRAIN (OUTPUT)
12. SOURCE, #3	12. ANODE	12. COMMON DRAIN (OUTPUT)
13. GATE, #2	13. ANODE	13. GATE N-CH
14. SOURCE, #2	14. ANODE	14. COMMON DRAIN (OUTPUT)
15. GATE, #1	15. ANODE	15. COMMON DRAIN (OUTPUT)
16. SOURCE, #1	16. ANODE	16. SOURCE N-CH

#### SOLDERING FOOTPRINT

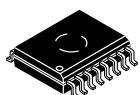


DIMENSIONS: MILLIMETERS

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DESCRIPTION:	SOIC-16	PAGE 1 OF 1

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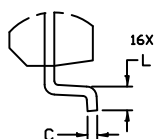
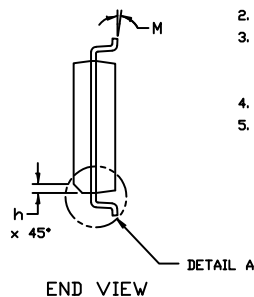
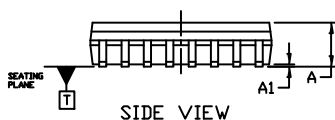
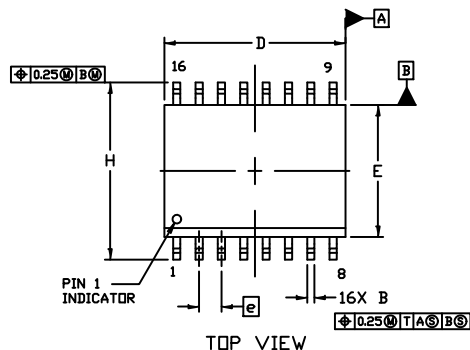
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1  
SCALE 1:1

## SOIC-16 WB CASE 751G ISSUE E

DATE 08 OCT 2021



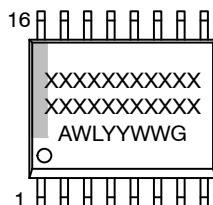
DETAIL A  
2X SCALE

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.  
ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

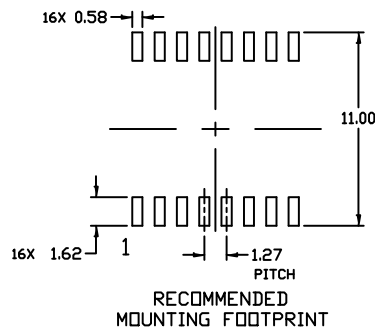
DIM	MILLIMETERS	
	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27	BSC
H	10.05	10.55
h	0.53	REF
L	0.50	0.90
M	0°	7°

### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

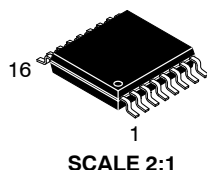


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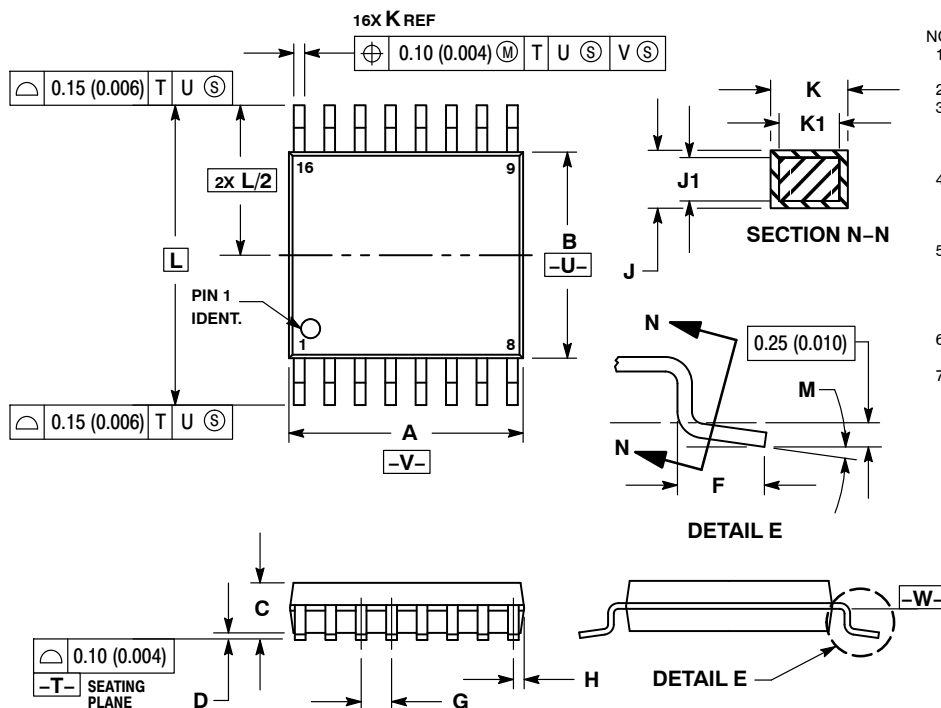
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



**TSSOP-16**  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006

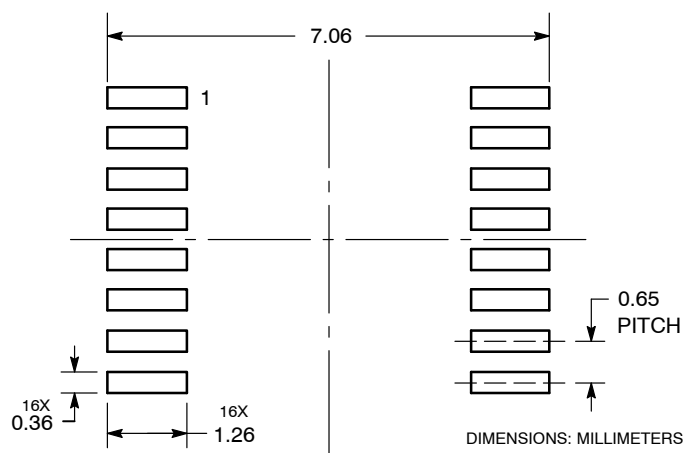


## NOTES:

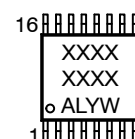
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

## SOLDERING FOOTPRINT



## GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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