JM1

JAMMA_CONN

#	Inner (left)	Inner (right)	Letter
1	GND	GND	A
2	VSSA	GND	B
3	VDDA	+5V	C
4	+5V	VCC	D
5	−5V	−5V	E
6	+12V	+12V	F
8	COIN_CNT_1	COIN_CNT_2	J
9	NC	NC	K
10	SPEAKER_(+)	SPEAKER_(−)	L
11	NC	NC	M
12	RED	GREEN	N
13	BLUE	SYNC	P
14	VIDEO_GND	SERVICE	R
15	NC	NC	S
16	COIN_1	COIN_2	T
17	1P_START	2P_START	U
18	1P_UP	2P_UP	V
19	1P_DOWN	2P_DOWN	W
20	1P_LEFT	2P_LEFT	X
21	1P_RIGHT	2P_RIGHT	Y
22	1P_BTN_1	2P_BTN_1	Z
23	1P_BTN_2	2P_BTN_2	a
24	1P_BTN_3	2P_BTN_3	b
25	1P_BTN_4	2P_BTN_4	c
26	1P_SELECT	2P_SELECT	d
27	GND	GND	e
28	GND	GND	f

Outer left labels: VSS, VCC, −5V, +12V, COIN_CNT_1, N.C0, SPEAKER(+), N.C1, RED, BLUE, VSS, NC, COIN_1, 1P_START, 1P_UP, 1P_DOWN, 1P_LEFT, 1P_RIGHT, 1P_BTN_1, 1P_BTN_2, 1P_BTN_3, VSS

Outer right labels: VSS, VCC, −5V, +12V, COIN_CNT_2, N.C3, SPEAKER(−), NC, GREEN, SYNC, SERVICE, N.C4, COIN_2, 2P_START, 2P_UP, 2P_DOWN, 2P_LEFT, 2P_RIGHT, 2P_BTN_1, 2P_BTN_2, 2P_BTN_3, VSS

ZD1 BZD27

PWR_FLAG

VSS

CABINET I/O

RC Filters
J5 J2 J1 R_P
R_Pack08

	VCC	VSS	
1	1P_START	1P_START	16
2	1P_BTN_1	1P_BTN_1	15
3	SERVICE	SERVICE	14
4	N.C4	TILT	13
5	2P_START	2P_START	12
6	2P_BTN_1	2P_BTN_1	11
7	VCC	VSS	10

1	1P_BTN_2	1P_BTN_2	16
2	1P_BTN_3	1P_BTN_3	15
3	1P_DOWN	1P_DOWN	14
4	1P_UP	1P_UP	13
5	1P_RIGHT	1P_RIGHT	12
7	1P_LEFT	1P_LEFT	11

8	VCC	VSS	9
1	2P_BTN_3	2P_BTN_3	16
2	2P_BTN_2	2P_BTN_2	15
3	2P_DOWN	2P_DOWN	14
4	2P_UP	2P_UP	13
5	1P_RIGHT	2P_RIGHT	12
6	1P_LEFT	2P_LEFT	11
7	VCC	VSS	10

H3
SETA-X1-004
P[23..10]

2	1P_START	P10	28
3	1P_BNT_3	P11	29
4	1P_BNT_2	P12	30
5	1P_BNT_1	P13	31
6	1P_DOWN	P14	32
7	1P_UP	P15	33
8	1P_RIGHT	P16	34
9	1P_LEFT	P17	35
10	2P_START	P20	37
11	2P_BNT_3	P21	40
12	2P_BNT_2	P22	41
13	2P_BNT_1	X10	42
14	2P_DOWN	X11	44
15	2P_UP	X12	45
16	2P_RIGHT	X13	46
17	2P_LEFT	X14	47
22	INC3	X15	48
23	INC2	X16	49
	N.C	X17	51
25	SERVICE		

CI/O2, CI/O1, TILT, SERVICE
VSS

---

main
Archivo: main.kicad_sch

Inputs: WDRES, VBLK, H[4..0], SND_RD, SND_MREQ, SND_WR
Outputs/signals: GFX_WR, SND_WAIT, OBJCODELO, MAIN_D[7..0], MAIN_A[15..0], VA[11..0], MAIN_VD[15..8], H4_BUF, MAIN_RD, H0_BUF, GFX_CE, RAM_WE, H2_BUF, SND_RST, WATCHDOG, RAM_CS1, GFXA_CS, GFXB_CS, GFXC_CS, GFXD_CS, H1_BUF, SBNKSWR, SBNKMWR, H3_BUF, SND_SELECT, BGTRNSP

mcu
Archivo: mcu.kicad_sch

RESET, SND_CS, COIN_LOCK, CI/O1, CI/O2, H1_BUF, N.C0, N.C3, MCU_RST, SND_A[15..0], P[23..10]
SND_D[7..0], SND_RD, P26_DRQ, SND_WR, CNN1A, CNN1B, COIN_1, COIN_2, COIN_CNT_1, COIN_CNT_2

gfx
Archivo: gfx.kicad_sch

GFX_CE, OBJCODELO, GFX_WR, GFXA_CS, GFXB_CS, GFXC_CS, GFXD_CS, MAIN_RD, H4_BUF, MAIN_A[15..0], MAIN_D[7..0], VA[11..0], H3_BUF
VSYNC, DATAEN, GFX_CLK, VBLK, H[4..0], VD[15..0], GDA[7..0], GDB[7..0], GDC[7..0], GDD[7..0], HBLK, WDRES, HC[8..0]

colmix
Archivo: colmix.kicad_sch

VSYNC, GFX_CLK, BGTRNSP, VD[15..0], GDA[7..0], GDB[7..0], GDC[7..0], GDD[7..0], H1_BUF, HBLK, DATAEN, HC[8..0]
SYNC, RED, GREEN, BLUE

watchdog
Archivo: watchdog.kicad_sch

WATCHDOG, +12V, P26_DRQ, CNN1B, CNN1A
RESET, COIN_LOCK

sound
Archivo: sound.kicad_sch

SND_A[15..0], SND_D[7..0], SND_SELECT, SND_WR, SND_RD, H0_BUF, SND_RST, SND_WAIT, MAIN_RD, N.C1, SPEAKER(−), SPEAKER(+), MAIN_A[13..0], H2_BUF, RAM_WE, RAM_CS1, SBNKSWR, SBNKMWR
MAIN_VD[15..8], SND_MREQ, SND_CS, MCU_RST

capacitors
Archivo: capacitors.kicad_sch

VCC

PWR_FLAG

| C1 | C22 | C23 | C24 | C25 | C26 | C27 | C28 | C29 | C30 | C31 | C32 | C33 | C34 | C35 | C36 | C37 |
| 1000μF | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 | 104 |

H12C

V+ 8

V− 4

NJM4558

VSS

PWR_FLAG

| H5E | B7C | B4C | B3C | B2E | G13G | C6E | B6E | B1G |
| 74LS02 | 74LS74 | 74LS74 | 74LS74 | 74LS08 | 74LS04 | 74LS32 | 74LS08 | 74LS04 |

JT

MAIN_A[15..0]

VCC

BANK_CFG[2..0]

MAIN_VD[15..8]

VCC

D6 PAL16L8
MAIN_A15 1 I1 VCC 20
MAIN_A14 2 I2 IO1 19 GFXA_CS
MREQ 3 I3 IO2 18 GFXB_CS
RFSH 4 I4 IO3 17 GFXC_CS
BANK_CFG2 5 I5 IO4 16 GFXD_CS
BANK_CFG0 6 I6 IO5 15 ROMB_A14
VA11 7 I7 IO6 14 RM_OEB
OBJCODELO 8 I8 IO7 13 RM_OEA
OBJCODEHI 9 I9 IO8 12
H3_BUF 11 I10 GND 10
VSS

C9
MAIN_A0 10 A0 VCC 28 D0 11 MAIN_VD8
MAIN_A1 9 A1 D1 12 MAIN_VD9
MAIN_A2 8 A2 D2 13 MAIN_VD10
MAIN_A3 7 A3 D3 15 MAIN_VD11
MAIN_A4 6 A4 D4 16 MAIN_VD12
MAIN_A5 5 A5 D5 17 MAIN_VD13
MAIN_A6 4 A6 D6 18 MAIN_VD14
MAIN_A7 3 A7 D7 19 MAIN_VD15
MAIN_A8 25 A8
MAIN_A9 24 A9
MAIN_A10 21 A10
MAIN_A11 23 A11
MAIN_A12 2 A12
MAIN_A13 26 A13
A14
BANK_CFG0 27 A15
BANK_CFG1 1
VSS 20 CE
RM_OEA 22 OE   GND 14
VSS   27C512

74LS174
MAIN_VD8 3 D0 Q0 2 BANK_CFG0
MAIN_VD9 4 D1 Q1 5 BANK_CFG1
MAIN_VD10 6 D2 Q2 7 BANK_CFG2
MAIN_VD13 11 D3 Q3 10
MAIN_VD12 13 D4 Q4 12
MAIN_VD11 14 D5 Q5 15
9 Cp
WDRES 1 Mr
hex flip flop
B5
SND_RST'

WDOGCLR
WDRES

74LS08 B2A
SND_RST

B1C 74LS04
WATCHDOG

VCC

E8 Z80CPU
11 VCC
WDRES 26 RESET A0 30 MAIN_A0
6 CLK A1 31 MAIN_A1
A2 32 MAIN_A2
A3 33 MAIN_A3
VCC A4 34 MAIN_A4
B4A A5 35 MAIN_A5
17 NMI A6 36 MAIN_A6
16 INT A7 37 MAIN_A7
D Q A8 38 MAIN_A8
74LS74 A9 39 MAIN_A9
VBLKD A10 40 MAIN_A10
Q A11 1 MAIN_A11
RFSH 27 M1 A12 2 MAIN_A12
28 RFSH A13 3 MAIN_A13
MAIN_WAIT 24 WAIT A14 4 MAIN_A14
18 HALT A15 5 MAIN_A15

MAIN_RD 21 RD D0 14 MAIN_D0
MAIN_WR 22 WR D1 15 MAIN_D1
19 MREQ D2 12 MAIN_D2
20 IORQ D3 8 MAIN_D3
D4 7 MAIN_D4
25 BUSRQ D5 9 MAIN_D5
23 BUSACK D6 10 MAIN_D6
D7 13 MAIN_D7
GND 29
VSS

MAIN_D[7..0]

VCC

C11
MAIN_A0 10 A0 VCC 28 D0 11 MAIN_VD8
MAIN_A1 9 A1 D1 12 MAIN_VD9
MAIN_A2 8 A2 D2 13 MAIN_VD10
MAIN_A3 7 A3 D3 15 MAIN_VD11
MAIN_A4 6 A4 D4 16 MAIN_VD12
MAIN_A5 5 A5 D5 17 MAIN_VD13
MAIN_A6 4 A6 D6 18 MAIN_VD14
MAIN_A7 3 A7 D7 19 MAIN_VD15
MAIN_A8 25 A8
MAIN_A9 24 A9
MAIN_A10 21 A10
MAIN_A11 23 A11
MAIN_A12 2 A12
MAIN_A13 26 A13
ROMB_A14 27 A14
ROMB_A15 1 A15
VSS 20 CE
RM_OEB 22 OE   GND 14
VSS   27C512

BANK_CFG1 9 B2C
MAIN_A15 10 74LS08 8

VCC
R330Ω R19

VCC

VCC

R330Ω R2

B13
H2 2 A0 B0 18 H2_BUF
3 A1 B1 17
H0 4 A2 B2 16
5 A3 B3 15 H0_BUF
6 A4 B4 14
H1 7 A5 B5 13 H1_BUF
H3 8 A6 B6 12 H3_BUF
H4 9 A7 B7 11 H4_BUF
buffers
VCC 1 A->B
VSS 19 CE 74LS245

H[4..0]

B1A 74LS04

RR15
R150Ω
LOW PASS FILTER

CC4
C101
VSS

D8 PAL16L8
MAIN_A15 1 I1 VCC 20
MAIN_A14 2 I2 IO1 19
MAIN_A13 3 I3 IO2 18
MAIN_A12 4 I4 IO3 17 OBJCODEHI
MAIN_A11 5 I5 IO4 16 WDOGCLR
MAIN_A10 6 I6 IO5 15 BGTRNSP
MAIN_A9 7 I7 IO6 14
8 I8 IO7 13 OBJCODELO
MREQ I8 GFX_WR
RFSH 9 I9 IO8 12
MAIN_WR 11 I10 GND 10
VSS

74LS08 B6B
GFX_CE

VCC

R31 R1
R1KΩ R1KΩ

C3 PAL16L8
MAIN_WR 1 I1 VCC 20
2 I2 IO1 19 SND_SELECT
SND_MREQ 3 I3 IO2 18 RAM_WE
SND_WR 4 I4 IO3 17 RAM_CS1
5 I5 IO4 16 SBNKMWR
6 I6 IO5 15 SBNKSWR
7 I7 IO6 14 MAIN_WAIT
SND_CLK' 9 I8 IO7 13 SND_WAIT
SND_CLK' 11 I9 IO8 12
I10 GND 10
VSS

H2_BUF 4 B2B
H3_BUF 5 74LS08 6

B4B
12 D Q 9
74LS74
Q 8
VCC

JT

B15

BGTRNSP 2 | BGTRNSP
GFX_CLK 3 | CLK
DATAEN 4 | DATAEN
VD7 5 | PAL4/TRSP
VD6 6 | PAL3
VD5 7 | PAL2
VD4 8 | PAL1
VD3 9 | PAL0
VD2 10 | D2

VD[7..0]

COL0 20 | COL0
COL1 21 | COL1
COL2 22 | COL2
COL3 23 | COL3
COL4 24 | COL4
COL5 25 | COL5
COL6 26 | COL6
COL7 27 | COL7
COL8 28 | COL8
UK 29

HC8 11 | HC8
HC7 12 | HC7
HC6 13 | HC6
HC5 14 | HC5
HC4 15 | HC4
HC3 16 | HC3
HC2 17 | HC2
HC1 18 | HC1
HC0 19 | HC0

HC[8..0]

GDA0 56 | GDA0
GDA1 57 | GDA1
GDA2 58 | GDA2
GDA3 59 | GDA3
GDA4 60 | GDA4
GDA5 61 | GDA5
GDA6 62 | GDA6
GDA7 63 | GDA7
GDB0 48 | GDB0
GDB1 49 | GDB1
GDB2 50 | GDB2
GDB3 51 | GDB3
GDB4 52 | GDB4
GDB5 53 | GDB5
GDB6 54 | GDB6
GDB7 55 | GDB7
GDC0 40 | GDC0
GDC1 41 | GDC1
GDC2 42 | GDC2
GDC3 43 | GDC3
GDC4 44 | GDC4
GDC5 45 | GDC5
GDC6 46 | GDC6
GDC7 47 | GDC7
GDD0 30 | GDD0
GDD1 31 | GDD1
GDD2 34 | GDD2
GDD3 35 | GDD3
GDD4 36 | GDD4
GDD5 37 | GDD5
GDD6 38 | GDD6
GDD7 39 | GDD7

GDA[7..0]
GDB[7..0]
GDC[7..0]
GDD[0..7]

YM3909
SETA_X1-002

VSS

COL[8..0]

F17
MB7124E
ROM 1kB

COL0 1 | A0
COL1 2 | A1
COL2 3 | A2
COL3 4 | A3
COL4 5 | A4
COL5 16 | A5
COL6 17 | A6
COL7 18 | A7
COL8 19 | A8
15 | CE

VCC 20
D0 6
D1 7
D2 8
D3 9
D4 11
D5 12
D6 13
D7 14
VSS 10

F15
MB7124E
ROM 1kB

COL0 1 | A0
COL1 2 | A1
COL2 3 | A2
COL3 4 | A3
COL4 5 | A4
COL5 16 | A5
COL6 17 | A6
COL7 18 | A7
COL8 19 | A8
15 | CE

VCC 20
D0 6
D1 7
D2 8
D3 9
D4 11
D5 12
D6 13
D7 14
VSS 10

H1_BUF

RC Filters
R_P G17
G15 R_P

HH16
SETAX1-003

D0 1 | RDC 36
D1 11 | R0 37
D2 12 | R1 38
D3 13 | R2 39
D4 14 | R3 40
D5 15 | R4 41
D6 16 | GDC 30
D7 17 | G0 31
D8 5 | G1 32
D9 7 | G2 33
D10 9 | G3 34
D11 6 | G4 35
D12 4 | BDC 29
D13 3 | B0 28
D14 2 | B1 27
D15 18 | B2 26
D16 | B3 25
UK | B4 24
VSYNC 20 | SYNC 23
HBLK 19 | HBLK 22
RDC 1 | VCC 2
VSS 21

VSYNC
HBLK

1kΩ
6,04kΩ
3,01kΩ
1,5kΩ
0,7kΩ
0,3kΩ
VSS

H15
R0-012
LSB
MSB

RED

H16
R0-012

GREEN

H17
R0-012

BLUE

VSS
VSS

SYNC

VCC
VSS

GA[15..0]

VD[15..0]

E11

MAIN_D1	2	A0	B0	18	VD9
MAIN_D0	3	A1	B1	17	VD8
MAIN_D7	4	A2	B2	16	VD15
MAIN_D6	5	A3	B3	15	VD14
MAIN_D5	6	A4	B4	14	VD13
MAIN_D4	7	A5	B5	13	VD12
MAIN_D3	8	A6	B6	12	VD11
MAIN_D2	9	A7	B7	11	VD10

MAIN_D[7..0]

buffers

MAIN_RD1 A−>B
19 CE
74LS245

OBJCODELOD 2
GFX_WR 1
74LS00 B6A 3

12 C6D 11
13 74LS37

A16

VD10	3	D0	Q0	2	GA7
VD11	4	D1	Q1	5	GA8
VD12	7	D2	Q2	6	GA9
VD13	8	D3	Q3	9	GA10
VD14	13	D4	Q4	12	GA11
VD8	14	D5	Q5	15	GA5
VD9	17	D6	Q6	16	GA6
VD15	18	D7	Q7	19	GA12

flip flops

H4_BUF 11 Cp
VCC 1 Mr
74LS273

E12

MAIN_D1	2	A0	B0	18	VD1
MAIN_D0	3	A1	B1	17	VD0
MAIN_D7	4	A2	B2	16	VD7
MAIN_D6	5	A3	B3	15	VD6
MAIN_D5	6	A4	B4	14	VD5
MAIN_D4	7	A5	B5	13	VD4
MAIN_D3	8	A6	B6	12	VD3
MAIN_D2	9	A7	B7	11	VD2

buffers

MAIN_RD 1 A−>B
19 CE
74LS245

H3_BUF

2 C6A 3
74LS32

GFX_CE 1

A15

VD1	3	D0	Q0	2	GA14
VD0	4	D1	Q1	5	GA13
VD5	6	D2	Q2	7	ROM_CE
VD4	11	D3	Q3	10	
VD3	13	D4	Q4	12	GA15
VD2	14	D5	Q5	15	ROM_OE

74LS174

H4_BUF 9 Cp
VCC 1 Mr
hex flip flop

VCC
R4 3.3kΩ
R3 22Ω

A17
1 Standby
GND VDD Out 3
12.000MHz
2 VSS

VCC

C17
VCC VCC

MAIN_RD 63 CLK CLKO 62 GFX_CLK
2 RD VBLK 58
GFX_WR 3 WR HBLK2 57
VD7 60 FLIPX VSYNC 56 VSYNC
VD6 59 FLIPY HBLK 55 HBLK
VD0 4 XC0 DATAEN 61 DATAEN

13 B1F 12 VBLK
74LS04

VD15	7	D7	HC8	54	HC8
VD14	8	D6	HC7	53	HC7
VD13	9	D5	HC6	52	HC6
VD12	10	D4	HC5	51	HC5
VD11	11	D3	HC4	50	HC4
VD10	12	D2	HC3	49	HC3
VD9	13	D1	HC2	48	HC2
VD8	14	D0	HC1	47	HC1
			HC0	46	HC0

HC[8..0]

YM3906

VA0	15	A0	H8	43	H4
VA1	16	A1	H4	42	H3
VA2	17	A2	H2	41	H2
VA3	18	A3	H0	40	H0
VA4	19	A4	HPH90	39	H1
VA5	20	A5	H		
VA6	21	A6			
VA7	22	A7			
VA8	23	A8			
VA9	24	A9			
VA10	25	A10			
VA11	28	A11			

VA[11..0]

H[4..0]

CHA0	35	GA0
CHA1	36	GA1
CHA2	37	GA2
CHA4	38	GA4

SPBANK1 26 SPBANK1
MAIN_A11 27 SPBANK2

MAIN_A[15..0]

H8B 34 HRB
WDRES 29 WDRES
30 RW

MAIN_RD 9 B1D 8
74LS04

5 74LS32 6 GFX_WR
4 C6B

5 UK
6 UK
31 UK
45 UK
44 UK

VSS VSS
64 62
VSS

SETA_X1-001

gfx_ram
H3_BUF H3_BUF SPBANK1 SPBANK1
MAIN_A[15..0] MAIN_A[15..0] VA[11..0] VA[11..0]
GFXA_CS GFXA_CS VD[15..0] VD[15..0]
GFXB_CS GFXB_CS
GFXC_CS GFXC_CS
GFXD_CS GFXD_CS
GFX_WR GFX_WR
Archivo: gfx_ram.kicad_sch

gfx_rom
ROM_CE ROM_CE GDA[7..0] GDA[7..0]
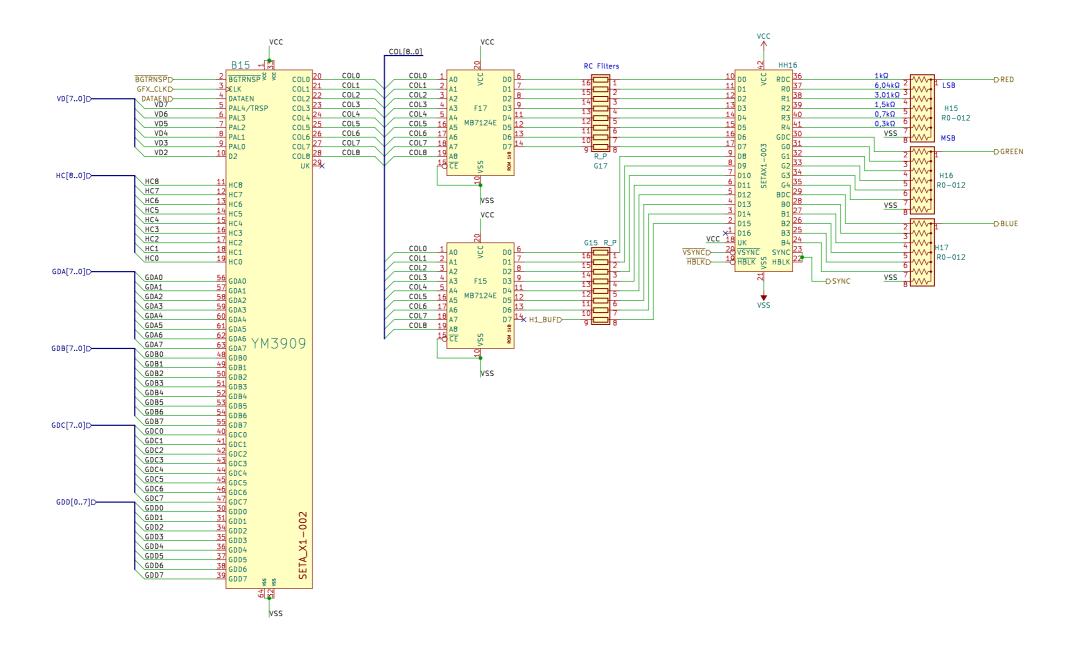ROM_OE ROM_OE GDB[7..0] GDB[7..0]
GA[15..0] GA[15..0] GDC[7..0] GDC[7..0]
HRB HRB GDD[7..0] GDD[7..0]
Archivo: gfx_rom.kicad_sch

JT

SND_A[15..0]

SND_A0

P[23..10]

VCC

G3

26 VDD
40 VCC

9 A0   D0 12   SND_D0
27 P10   D1 13   SND_D1
28 P11   D2 14   SND_D2
29 P12   D3 15   SND_D3
30 P13   D4 16   SND_D4
31 P14   D5 17   SND_D5
32 P15   D6 18   SND_D6
33 P16   D7 19   SND_D7
34 P17
21 P20   P24_OBF 35
22 P21   P26_DRQ 37
23 P22   P27_DACK 38
24 P23   RD 8
25 PROG   WR 10
36 P25_IBF   SYNC 11

INTEL8742

1 TEST0
39 TEST1
2 XTAL1
3 XTAL2
4 RESET
5 SS
6 CS
7 EA

8-BIT SLAVE MICROCONTROLLER

VSS 20

TEST0
TEST1
H1_BUF
H1_BUF
MCU_RST
VCC
SND_CS
VSS

VSS

SND_D[7..0]

P26_DRQ

SND_RD
SND_WR

11
13 H5D
12 74LS02
OBF

5
4 H5B
6 74LS02

RESET

9
10 H5C
8 74LS02

JJ10

28 COIN_2   COINOUT2 26   TEST1
27 COIN_1   COINOUT1 25   TEST0
14 UK   COIN_CNT_1 16   COIN_CNT_1
3 UK   COIN_CNT_2 4   COIN_CNT_2
23 COIN1   LOCK-OUT1 19   IN.C0
12 OBF   LOCK-OUT2 18   IN.C3
20 DACK   CNN1 2   CNN1A
8 IBF   CNN2 10   CNN1B
13 UK   UK.N.C 7
             UK.NC 12
             UK.NC 23

11 VSS
6 VSS
5 VSS   VCC 5
1 VSS   VCC 9   VCC
24 VSS   VCC 21

PC050CM

COIN_2
COIN_1
CI/O2
CI/O1
COIN_LOCK

VSS

VCC

R20
R330Ω

H1_BUF

11 G15E 10   H1_BUF
74LS04

GA[15..0]

NOT MOUNTED

VCC

A13 28 VCC — 27C512
GA0 10 A0 D0 11 GDA0
GA1 9 A1 D1 12 GDA1
GA2 8 A2 D2 13 GDA2
HR8 7 A3 D3 15 GDA3
GA4 6 A4 D4 16 GDA4
GA5 5 A5 D5 17 GDA5
GA6 4 A6 D6 18 GDA6
GA7 3 A7 D7 19 GDA7
GA8 25 A8
GA9 24 A9
GA10 21 A10
GA11 23 A11
GA12 2 A12
GA13 26 A13
GA14 27 A14
GA15 1 A15
ROM_CE 20 CE
ROM_OE 22 OE
VSS 14 GND

A12 28 VCC — 27C512
GA0 10 A0 D0 11 GDA0
GA1 9 A1 D1 12 GDA1
GA2 8 A2 D2 13 GDA2
HR8 7 A3 D3 15 GDA3
GA4 6 A4 D4 16 GDA4
GA5 5 A5 D5 17 GDA5
GA6 4 A6 D6 18 GDA6
GA7 3 A7 D7 19 GDA7
GA8 25 A8
GA9 24 A9
GA10 21 A10
GA11 23 A11
GA12 2 A12
GA13 26 A13
GA14 27 A14
GA15 1 A15
ROM_CE 20 CE
ROM_OE 22 OE
VSS 14 GND

GDA[7..0]

A10 28 VCC — 27C512
GA0 10 A0 D0 11 GDB0
GA1 9 A1 D1 12 GDB1
GA2 8 A2 D2 13 GDB2
HR8 7 A3 D3 15 GDB3
GA4 6 A4 D4 16 GDB4
GA5 5 A5 D5 17 GDB5
GA6 4 A6 D6 18 GDB6
GA7 3 A7 D7 19 GDB7
GA8 25 A8
GA9 24 A9
GA10 21 A10
GA11 23 A11
GA12 2 A12
GA13 26 A13
GA14 27 A14
GA15 1 A15
ROM_CE 20 CE
ROM_OE 22 OE
VSS 14 GND

A8 28 VCC — 27C512
GA0 10 A0 D0 11 GDB0
GA1 9 A1 D1 12 GDB1
GA2 8 A2 D2 13 GDB2
HR8 7 A3 D3 15 GDB3
GA4 6 A4 D4 16 GDB4
GA5 5 A5 D5 17 GDB5
GA6 4 A6 D6 18 GDB6
GA7 3 A7 D7 19 GDB7
GA8 25 A8
GA9 24 A9
GA10 21 A10
GA11 23 A11
GA12 2 A12
GA13 26 A13
GA14 27 A14
GA15 1 A15
ROM_CE 20 CE
ROM_OE 22 OE
VSS 14 GND

GDB[7..0]

ROM_CE 11 B1E 10 ROM_CE'
74LS04

A7 28 VCC — 27C512
GA0 10 A0 D0 11 GDC0
GA1 9 A1 D1 12 GDC1
GA2 8 A2 D2 13 GDC2
HR8 7 A3 D3 15 GDC3
GA4 6 A4 D4 16 GDC4
GA5 5 A5 D5 17 GDC5
GA6 4 A6 D6 18 GDC6
GA7 3 A7 D7 19 GDC7
GA8 25 A8
GA9 24 A9
GA10 21 A10
GA11 23 A11
GA12 2 A12
GA13 26 A13
GA14 27 A14
GA15 1 A15
ROM_CE 20 CE
ROM_OE 22 OE
VSS 14 GND

A5 28 VCC — 27C512
GA0 10 A0 D0 11 GDC0
GA1 9 A1 D1 12 GDC1
GA2 8 A2 D2 13 GDC2
HR8 7 A3 D3 15 GDC3
GA4 6 A4 D4 16 GDC4
GA5 5 A5 D5 17 GDC5
GA6 4 A6 D6 18 GDC6
GA7 3 A7 D7 19 GDC7
GA8 25 A8
GA9 24 A9
GA10 21 A10
GA11 23 A11
GA12 2 A12
GA13 26 A13
GA14 27 A14
GA15 1 A15
ROM_CE 20 CE
ROM_OE 22 OE
VSS 14 GND

GDC[7..0]

A4 28 VCC — 27C512
GA0 10 A0 D0 11 GDD0
GA1 9 A1 D1 12 GDD1
GA2 8 A2 D2 13 GDD2
HR8 7 A3 D3 15 GDD3
GA4 6 A4 D4 16 GDD4
GA5 5 A5 D5 17 GDD5
GA6 4 A6 D6 18 GDD6
GA7 3 A7 D7 19 GDD7
GA8 25 A8
GA9 24 A9
GA10 21 A10
GA11 23 A11
GA12 2 A12
GA13 26 A13
GA14 27 A14
GA15 1 A15
ROM_CE 20 CE
ROM_OE 22 OE
VSS 14 GND

A2 28 VCC — 27C512
GA0 10 A0 D0 11 GDD0
GA1 9 A1 D1 12 GDD1
GA2 8 A2 D2 13 GDD2
HR8 7 A3 D3 15 GDD3
GA4 6 A4 D4 16 GDD4
GA5 5 A5 D5 17 GDD5
GA6 4 A6 D6 18 GDD6
GA7 3 A7 D7 19 GDD7
GA8 25 A8
GA9 24 A9
GA10 21 A10
GA11 23 A11
GA12 2 A12
GA13 26 A13
GA14 27 A14
GA15 1 A15
ROM_CE 20 CE
ROM_OE 22 OE
VSS 14 GND

GDD[7..0]

JT