Xilinx Spartan™-3 400 Evaluation Kit

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1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the Spartan-3 400 Evaluation Kit from Avnet Design Services. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the example projects.

1.1 Description

The Spartan-3 Evaluation Kit provides a platform for engineers designing with the Xilinx Spartan-3 FPGA. The board provides the necessary hardware to not only evaluate the advanced features of the Spartan-3 but also to implement complete user applications. Example projects are provided to help the user understand the design tool flow of the Xilinx Embedded Development Kit (EDK) software environment.

1.2 Features:

- FPGA
  - Xilinx Spartan-3
    - XC3S400-FG456
    - XC3S1500-FG456
- Board I/O Connectors
  - Two140-pin general purpose I/O expansion connectors (AvBus)
  - 50 – Pin 0.1" Header (4 LVDS pairs)
  - 32 bit PCI edge connector (3.3V/5V universal)
- Memory
  - Cypress Async SRAM -1MB
  - Atmel Serial EEPROM – 256kb (1Mbit on 3S1500)
- Communication
  - 10/100 base T Ethernet
  - Two PS2 compatible ports
  - RS-232 serial port
- Video
  - RGB Video DAC (DB15)
- Analog I/O
  - DAC (per Xilinx AP-Note XAPP154)
  - A/D (per Xilinx AP-Note XAPP155)
- Power
  - 10+ Watt AC/DC +5.0V power supply
  - Texas Instruments 3.3V 6A Module
  - National Linear regulators
- Configuration
  - Xilinx XCF02S PROM (XCF04S+XCF01S)
  - On Board Parallel III Cable circuitry and support for Parallel IV cable
  - Fly-wire support for any Xilinx or compatible cable

1.3 Demo Applications:

The Spartan-3 Evaluation Kit from Avnet Design Services comes with both source code and example projects designed in Xilinx Platform Studio (XPS). XPS is a software tool in the Xilinx Embedded Development Kit (EDK) that provides the user with a single tool flow for creating both hardware and software for processor-based systems. The source code and example projects that will be discussed in detail later in this document are listed below.

- Source Code
  - Mouse Interface (PS2)
  - Video DAC Interface (VHDL)
  - Analog Comparator (Verilog)
  - LED Segment Display (VHDL)
- XPS Example Projects
  - Hello World
  - External Memory Project
  - Multi-Peripheral Project
  - Video/Mouse Game

Figure 1 - Spartan-3 Evaluation Board Picture

1.4 Ordering Information:

The following table lists the evaluation kit part numbers and available software options.
Internet link at http://www.ads.avnet.com

Part Number	Hardware
ADS-XLX-SP3-EVL400	Xilinx Spartan-3 Evaluation Kit populated with an XC3S400 device
ADS-XLX-SP3-EVL1500	Xilinx Spartan-3 Evaluation Kit populated with an XC3S1500 device
ADS-SP3-MB-EVL400	Xilinx Spartan-3 Evaluation Kit populated with an XC3S400 device and bundled with MicroBlaze Core License
ADS-SP3-MB-EVL1500	Xilinx Spartan-3 Evaluation Kit populated with an XC3S1500 device and bundled with MicroBlaze Core License
ADS-FOUNDATION-BUNDLE	ISE Foundation (only available with purchase of the ADS-XLX-SP3-EVL1500)
ADS-BASEX-BUNDLE	ISE BaseX (only available with purchase of the ADS-XLX-SP3-EVL400)

Table 1 - Ordering Information

2.0 User Information

This section provides the user with information on how to get started using the Spartan-3 Evaluation board. It discusses how to power the board, configure the FPGA devices and set-up the jumpers.

2.1 Power

The Spartan-3 Evaluation Kit includes a 5V AC/DC Adapter that plugs into the board at "J9".

2.2 Configuration

The Spartan-3 Evaluation board supports only Boundary-scan configuration of the FPGA and programming of the configuration PROMs. Using the iMPACT tool from Xilinx or equivalent the user can use the included parallel cable, Parallel III / IV cable or Multi-Pro Cable to download configuration data.

2.2.1 Boundary scan

Programming the Spartan-3 FPGA via Boundary-scan requires a JTAG download cable attached to one of three interfaces that are all wired in parallel on the board. The included parallel cable can be attached to the DB25 mating connector "P1" or an alternate cable can be attached to either the 14pin 2mm spaced header "JP3" with a ribbon cable or to the SIP Header "JP5" with flying leads as appropriate to your cable. For more information about JTAG download cables see the Xilinx web page http://www.xilinx.com. Click on the "Products" tab and then click on the "Configuration" link. Scroll down to "Desktop Programmers and Download Cables" and select the download cable of interest.

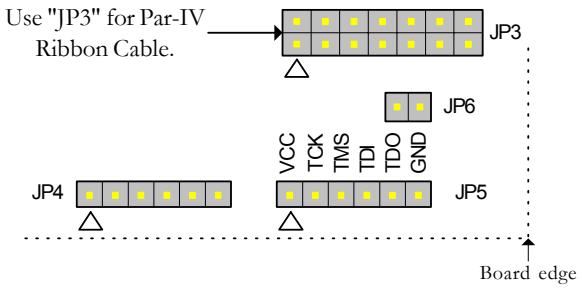


Figure 2 - Configuration / Debug Connectors

If the Parallel Cable IV is used, the ribbon cable connector mates with the JP3 connector. This connector is keyed to ensure the connections are made correctly.

The Spartan-3 Evaluation board provides the user with the ability to add/remove devices from the JTAG chain. By the default settings, the chain of the ADS-XLX-SP3-EVL400 board includes the XCF02S configuration and the Spartan-3 FPGA. On the ADS-XLX-SP3-EVL1500 board a second configuration FLASH is included to allow sufficient memory for the configuration data. The header labeled "JP4" allows the user to select additional devices for inclusion in the chain. This will be discussed in greater detail in the hardware section of this manual. Most users will only use the JTAG chain in standalone mode with a jumper installed across pins 2-3 on JP4. It is recommended to start with standalone mode.

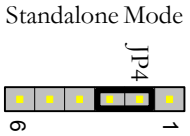


Figure 3 - JTAG Chain Standalone Mode

The configuration modes of the FPGA must be selected before applying power to the board. Jumper settings will allow the Spartan 3 device to be set to any possible mode but only 2 Master Serial and Boundary Scan are supported on this board. The Spartan-3 FPGA is set to Master Serial mode when no jumpers are installed on JP1. To set the FPGA to boundary-scan mode, install shunts on JP1 at locations 1-2 & 5-6 as shown in Figure 4. For a complete list of available modes, please see the Configuration Modes section of Chapter 3 in the Spartan-3 Platform FPGA Handbook.

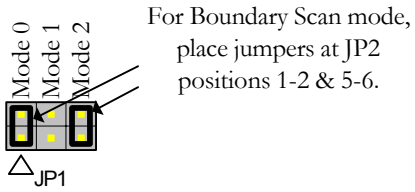


Figure 4 – Boundary Scan Mode Selection via JP1

After the download cable, chain and modes have been set; apply power to the board and open/run the iMPACT software to configure the boundary-scan devices. It is recommended to use the version of iMPACT in the Xilinx ISE 6.1i or later tools. Earlier versions of the tools may work but they will not be supported.

2.2.2 Configuration from XCF0xS PROMs

The PROMs provide easy-to-use non-volatile storage for the configuration file. These devices are in system programmable via the boundary scan chain and will configure the FPGA in Master Serial mode. After programming the proms with configuration data, remove power and set JP1 appropriately as indicated in Figure 5. When power is re-applied, the FPGA will clock the serial data from the PROMs.

Master Serial Mode:
No Jumpers on JP1

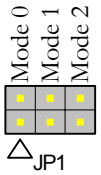
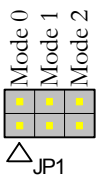


Figure 5 - Master Serial mode via JP1

2.3 Jumper Settings

This section provides a description of the jumper settings for the Evaluation board. The jumpers are listed in order by JP number. The board is ready to use out of the box with the default jumper settings.

JP1 – Configuration mode selection. Use to select the configuration mode for the FPGA. By default, these pins are pulled low enabling Master Serial mode. Installing jumpers on JP1 will pull the corresponding mode pin high, as indicated in Figure 6. See the Configuration section of this document or Chapter 3 of the Spartan-3 Platform FPGA Handbook for further information.



JP1	1-2	3-4	5-6
Config Mode	M0	M1	M2
Master Serial	0	0	0
Slave Serial	1	1	1
Master SelectMAP	1	1	0
Slave SelectMAP	0	1	1
Boundary Scan	1	0	1

Figure 6 - JP1

JP2 – HSWAP_EN, Enables pull-ups on the Spartan-3 I/O pins during configuration. A pull-down resistor "R24" is used to enable the I/O pull-ups during configuration. Install a jumper to disable the configuration pull-ups. Default: Open; pull-ups enabled.

JP3 – Parallel IV connector. See the **Boundary scan** section of this document for more information.

JP4 – JTAG chain configuration. Selects the JTAG chain configuration. Install a jumper across pins 2-3 for standalone mode. Install jumpers across pins 1-2 and pins 4-5 to add the AvBus connector labeled "P5" on to the standalone chain. Install jumpers across pins 1-2, pins 3-4 and pins 5-6 to add the AvBus connector labeled "J8" on to the standalone chain. These settings are described in detail in the Hardware section of this manual (see section 3.12).
Default: Installed across pins 2-3; standalone chain mode.

JP5 –Flying Lead connector for JTAG interface.

JP6 – JTAG TRST, forces TRST low. Default Open

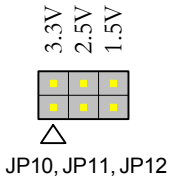
JP7 – 50-pin general purpose header I/O. See the I/O Connectors section of this document.

JP9 – Video clock disable. The 25.175MHz Oscillator "U14" provides the clock for the VGA interface on the board. The clock is enabled if the shunt is placed on pins 1-2 and disabled when the shunt is placed on pins 2-3. Default 1-2, enabled

Note: the oscillator may also have an internal pull-up resistor to enable it when no shunt is installed.

JP10 – Analog I/O interface

JP11 – Bank 5 VCCO selection. Selects I/O voltage for FPGA bank 5. Only one jumper should be placed at this connector. Valid placements are 1-2, 3-4, or 5-6 as indicated in Figure 7. By removing the shunt and attaching an external power supply to pins 2, 4 or 6 of JP11, alternate voltages can be supported. If an external supply is used be sure that it does not exceed the capabilities of the Spartan-3 device, as there is no protection on the board.



Jumper Position	1-2	3-4	5-6
I/O Voltage	3.3V	2.5V	1.2V

Figure 7 - I/O Voltage Selection

JP12 – Active Heat sink Power

JP13 – Serial EEPROM write protect, install shunt to protect programmed data. Default, Open, read/write enabled

Additional flexibility has been designed into the circuit in the form of resistor jumpers "JTx" and series resistors that can be moved or removed to alter the functionality of the board. The purpose of some of these components may be discussed in other sections of this manual others may not all be discussed at all. The position of these components should not be altered without careful revue of the schematics and associated component data sheets to prevent damage to the board.

3.0 Hardware

This section of the manual describes the hardware of the Spartan-3 Evaluation board. The hardware was designed with the Spartan-3 FPGA as the focal point. The block diagram is shown in Figure 8.

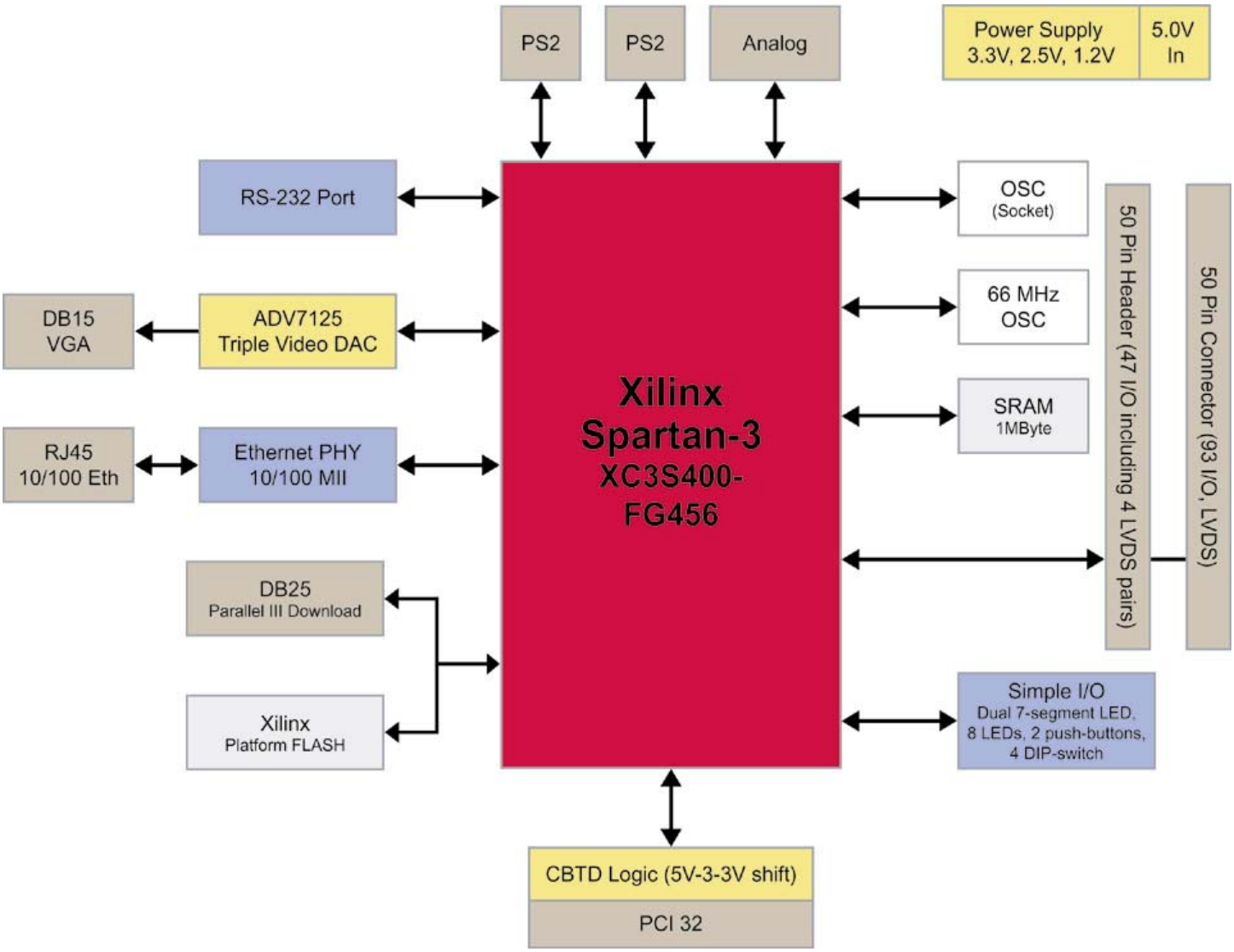


Figure 8 - Spartan-3 Evaluation Board Block Diagram

3.1 Spartan-3 FPGA

The Spartan-3 Evaluation board was designed to support the Spartan-3 FPGA in the 456-pin, BGA package (FG456). The FG456 package is a versatile package supporting three mid-range densities 3S400, 3S1000 and 3S1500. The Spartan-3 Evaluation board will be available with device options of the 400 and 1500. The schematic symbol used for the Spartan-3 device indicates the specific I/O pins available in each density (264 I/Os with 3S400 and 333 I/Os with the 3S1000 and 3S1500). This design of this board was limited to the 264 I/O pins available on all device densities. The extra I/O pins on the higher density parts are attached to vias to allow probing or external connection but they have no other connection on the board.

3.2 Memory

The Spartan-3 Evaluation board is populated with two asynchronous SRAM devices and one serial EEPROM device. Additional memory including Flash, SDRAM, and SRAM are available with the purchase of the Avnet Communications/Memory Module.

3.2.1 Asynchronous SRAM

Two Cypress SRAM devices, part number: CY7C1041CV33, make up a 32-bit data bus and provide 1M Byte of data storage.

Signal Name	FPGA pin#		Signal Name	FPGA pin#
ADDR0	E22		DATA0	U19
ADDR1	E21		DATA1	T21
ADDR2	D21		DATA2	U20
ADDR3	E20		DATA3	U21
ADDR4	D22		DATA4	V21
ADDR5	D20		DATA5	V22
ADDR6	C22		DATA6	W22
ADDR7	D19		DATA7	V20
ADDR8	C20		DATA8	Y19
ADDR9	C21		DATA9	W19
ADDR10	F18		DATA10	V19
ADDR11	G18		DATA11	Y20
ADDR12	G19		DATA12	Y12
ADDR13	E18		DATA13	Y22
ADDR14	F19		DATA14	W20
ADDR15	F20		DATA15	W21
ADDR16	E19		DATA16	M17
ADDR17	F21		DATA17	L17
			DATA18	M19
BE#0	K21		DATA19	M18
BE#1	K22		DATA20	M20
BE#2	G22		DATA21	N19
BE#3	K20		DATA22	M21
			DATA23	N20
SRAM_CS#	G21		DATA24	T22
			DATA25	U18
R_W#	K19		DATA26	T18
			DATA27	R18
OE#	G17		DATA28	T17
			DATA29	N21
			DATA30	N22
			DATA31	M22

Table 2 - SRAM FPGA Pin-out

3.2.2 Serial EEPROM

Non-Volatile data storage is provided for in the form of an Atmel serial EEPROM device, part number: AT24C256W-10SI. A two wire I2C interface allows the user to read and write to this memory device. Once programmed the data can be secured by installing a shunt on the write protect header "JP13".

EEPROM PIN Name	Signal Name	FPGA pin#
SDA	FPGA_D0	AA14
SCL	FPGA_INIT#	W12

Table 3 - EEPROM FPGA Pin-out

3.3 RS-232 Transceiver

The RS-232 transceiver is a 3222 available from Harris/Intersil (ICL3222CA) and Analog Devices (ADM3222). This transceiver is operating at 3.3V for VCC with an internal charge pump to create the RS-232 compatible output levels.

The RS-232 console interface is brought out on the DB9 connector labeled "P3". Though the level converter supports two channels, only TX and RX are connected to the FPGA. The other pair is connected to the DB9 connector as RTS and CTS but on the logic level side of the converter these are attached to test points only.

A straight through serial cable should be used to plug "J10" into a standard PC serial port (male DB9). The following tables show the pin-outs for the FPGA and connector interfaces.

Signal Name	FPGA pin#	Xcvr pin#	DB9 (P3)
Primary channel Transmit (RS232TX)	C3	13	2
Primary channel Receive (RS232RX)	C4	15	3

Table 4 - RS-232 FPGA Pin-out

3.4 10/100 Ethernet

To support networking functions a 10/100 Ethernet PHY, National Semiconductor part # DP83846A, was added to the Spartan-3 Evaluation board. Specific operating modes can be selected by moving the resistor jumpers JT14, JT15 and JT16 but by default the PHY is set to auto negotiate a link with a peer. The use of this port requires an Ethernet MAC core to be instantiated in the FPGA project. The example projects that include network support utilize licensed IP cores from Xilinx. A Valid license for this IP may be required to regenerate the projects.

Signal Name	FPGA pin#		Signal Name	FPGA pin#
MII_MDC	C17		MII_CRS	E12
MII_MDIO	B17		MII_COL	D13
MII_TXD0	B13		MII_RXD0	B15
MII_TXD1	A13		MII_RXD1	A15
MII_TXD2	C13		MII_RXD2	D15
MII_TXD3	D12		MII_RXD3	E15
MII_TXEN	E14		MII_RXDV	B14
MII_TXERR	D14		MII_RXERR	A14
MII_TX_CLK	C12		MII_RXCLK	B12

Table 5 - Ethernet FPGA Pin-out

3.5 RGB Video

Digital RGB Video can be driven to a VGA monitor from the Spartan-3 FPGA via an Analog Devices ADV7123 Triple Video DAC. The output from the DAC is attached to a DB15 connector in a standard pinout to support most commercially available video monitors. The following tables show the pin-outs for the FPGA interfaces.

Signal Name	FPGA pin#		Signal Name	FPGA pin#
Green			Red	
DVD_G0	F10		DVD_R0	D6
DVD_G1	D10		DVD_R1	C6
DVD_G2	A10		DVD_R2	B6
DVD_G3	D9		DVD_R3	D5
DVD_G4	A9		DVD_R4	A5
DVD_G5	B9		DVD_R5	B5
DVD_G6	A8		DVD_R6	C5
DVD_G7	B8		DVD_R7	B4
Blue				
DVD_B0	E9		Misc	
DVD_B1	F9		DVD_BLANK	A4
DVD_B2	D7		DVD_CSYNC	A3
DVD_B3	C7		VIDEO_CLK	B11
DVD_B4	E7		VSYNC	D11
DVD_B5	F7		HSYNC	E11
DVD_B6	E6			
DVD_B7	F6			

Table 6 - Video FPGA Pin-out

3.6 PS2 Keyboard and Mouse

Two mini-din 6 (PS2) connectors are included on the board to provide interface from the Spartan-3 FPGA to a keyboard and/or mouse device. A Texas Instruments SN74CBTLV3125 logic device has been added to clamp the 5V signals from the keyboard and mouse to 3.3V to protect the I/O logic cells of the FPGA.

Signal Name	FPGA pin#	JS1 pin#		Signal Name	FPGA pin#	JS2 pin#
KBDATA	U16	1		MSDATA	W13	1
KBCLK	U17	5		MSCLK	W14	5

Table 7– PS2 FPGA Pin-out

3.7 Analog I/O

Analog I/O was added to the board according to the circuitry described in the Xilinx Application notes XAPP154 and XAPP155.

The DAC function is accomplished by adding a passive filter circuit to an FPGA I/O pin and using PWM logic to create the analog output.

The A/D requires a second DAC circuit as described above to provide a variable voltage reference to the negative input of an analog comparator IC. The positive input is connected to the analog input and the output is connected to an FPGA I/O pin providing an edge when the voltages match.

The three analog signals can be accessed at the 6-pin header "JP10" and are connected to the FPAG as listed below.

FPGA pin#	Net Name	Comment	Signal Name	JP10 pin#		Signal Name
N/A		Analog Input to A/D	ANALOG_IN	1	2	GND
U13	ANA_REF	PWM Output to A/D Vref	DAC_REF	3	4	GND
Y16	ANA_OUT	PWM Output to DAC	ANALOG_OUT	5	6	GND
V18	CMP_OUT	A/D Comparator Output to the FPGA				

Table 8 – Analog I/O Pin-out

3.8 User I/O

Basic user I/O is provided for on the Spartan-3 Evaluation Board in the form of switches and LED indicators. These peripherals have been added to give the user the ability to monitor and control the execution of a project early in development.

3.8.1 Push Buttons

Two momentary closure push buttons have been installed on the board and attached to the FPGA. These buttons can be programmed by the user and are ideal for logic reset and similar functions. Pull down resistors hold the signals low (0) until the switch closure pulls it high (1).

Part #	Signal Name	FPGA pin#
SW3	SWITCH_PB1	Y1
SW4	SWITCH_PB1	W2

Table 9 - Pushbutton FPGA Pin-out

3.8.2 DIP-switch

A four-position DIP-switch (SPST) has been installed on the board and attached to the FPGA. These switches provide digital inputs to user logic as needed. The signals are pulled low (0) by 10K ohm resistors when the switch is open and tied to 3.3V (1) when the switch is closed.

Switch #	Signal Name	FPGA pin#
SW2-1	SWITCH0	W4
SW2-2	SWITCH1	W3
SW2-3	SWITCH2	Y3
SW2-4	SWITCH3	Y2

Table 10 – DIP-switch FPGA Pin-out

3.8.3 Discrete LEDs

Eight discrete LEDs are installed on the board and can be used to display the status of the internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic (1) and are off when the pin is either Low (0) or not driven.

LED #	Signal Name	FPGA pin#
D4	LED0	U12
D5	LED1	V12
D6	LED2	Y12
D7	LED3	Y13
D8	LED4	AB13
D9	LED5	AA13
D10	LED6	V13
D11	LED7	AB14

Table 11 - LED FPGA Pin-out

3.8.4 Character LED Display

A dual character 7segment LED display (MAN6141C) is on the board for use in user applications. The individual segments are attached to the FPGA as shown below and are lit by forcing the associated FPGA I/O pin to a logic (1) and are off when the pin is either Low (0) or not driven.

U6 Segment #	Signal Name	FPGA pin#
A1	SIG1_A	AA18
B1	SIG1_B	Y18
C1	SIG1_C	AA15
D1	SIG1_D	V14
E1	SIG1_E	U14
F1	SIG1_F	V17
G1	SIG1_G	AB18
Dp1	SIG1_Dp	AB15
A2	SIG2_A	AB20
B2	SIG2_B	AA20
C2	SIG2_C	AA17
D2	SIG2_D	W16
E2	SIG2_E	V16
F2	SIG2_F	W18
G2	SIG2_G	Y17
Dp2	SIG2_Dp	W17

Table 12 – Character Display FPGA Pin-out

3.9 PCI Interface

The Spartan-3 Evaluation board is built in a 32bit universal PCI form factor supporting 3.3V and 5V PCI Backplanes. Though the board is not 100% compliant to the PCI specification it is compatible and will function in most systems. Third party or custom IP is required to use this interface.

FPGA pin#	Signal Name	Pin Name	PCI Pin #		Pin Name	Signal Name	FPGA pin#
	JTAG_TRST	TRST#	A1	B1	-12V	-12V_PCI	
	+12V_PCI	+12V	A2	B2	TCK	JTAG_TCK	
	JTAG_TMS	TMS	A3	B3	GND	GND_SIGNAL	
	JTAG_TDI	TDI	A4	B4	TDO	JTAG_TDO	
	5.0V	+5V	A5	B5	+5V	5.0V	
M6	PCI_INT**	INTA#	A6	B6	+5V	5.0V	
M6	PCI_INT**	INTC#	A7	B7	INTB#	PCI_INT**	M6
	5.0V	+5V	A8	B8	INTD#	PCI_INT**	M6
		N/C	A9	B9	PRSNT1#	GND_SIGNAL	

	VIO	VIO	A10		B10	N/C		
		N/C	A11		B11	PRSNT2#	GND_SIGNAL	
KEY			A12		B12	KEY		
			A13		B13			
		N/C	A14		B14	N/C		
E4	PCI_RST	RST#	A15		B15	GND	GND_SIGNAL	
	VIO	VIO	A16		B16	CLK	PCI_CLK	AA12
L5	PCI_GNT#	GNT#	A17		B17	GND	GND_SIGNAL	
	GND_SIGNAL	GND	A18		B18	REQ#	PCI_REQ#	L6
		N/C	A19		B19	VIO	VIO	
D3	PCI_AD_30	AD[30]	A20		B20	AD[31]	PCI_AD_31	D2
	3.3V_PCI	+3.3V	A21		B21	AD[29]	PCI_AD_29	E3
F4	PCI_AD_28	AD[28]	A22		B22	GND	GND_SIGNAL	
E1	PCI_AD_26	AD[26]	A23		B23	AD[27]	PCI_AD_27	E2
	GND_SIGNAL	GND	A24		B24	AD[25]	PCI_AD_25	F5
G6	PCI_AD_24	AD[24]	A25		B25	+3.3V	3.3V_PCI	
L3	PCI_IDSEL	IDSEL	A26		B26	C/BE[3]#	PCI_CBE_3	K2
	3.3V_PCI	+3.3V	A27		B27	AD[23]	PCI_AD_23	F3
F2	PCI_AD_22	AD[22]	A28		B28	GND	GND_SIGNAL	
H5	PCI_AD_20	AD[20]	A29		B29	AD[21]	PCI_AD_21	G5
	GND_SIGNAL	GND	A30		B30	AD[19]	PCI_AD_19	G2
G1	PCI_AD_18	AD[18]	A31		B31	+3.3V	3.3V_PCI	
K3	PCI_AD_16	AD[16]	A32		B32	AD[17]	PCI_AD_17	K4
	3.3V_PCI	+3.3V	A33		B33	C/BE[2]#	PCI_CBE_2	K1
L2	PCI_FRAME#	FRAME#	A34		B34	GND	GND_SIGNAL	
	GND_SIGNAL	GND	A35		B35	IRDY#	PCI_IRDY#	L1
M1	PCI_TRDY#	TRDY#	A36		B36	+3.3V	3.3V_PCI	
	GND_SIGNAL	GND	A37		B37	DEVSEL#	PCI_DEVSEL#	M2
M3	PCI_STOP#	STOP#	A38		B38	GND	GND_SIGNAL	
	3.3V_PCI	+3.3V	A39		B39	LOCK#	N/C	
	N/C	SDONE	A40		B40	PERR#	PCI_PERR#	M4
	N/C	SBO#	A41		B41	+3.3V	3.3V_PCI	
	GND_SIGNAL	GND	A42		B42	SERR#	PCI_SERR#	M5
L4	PCI_PAR	PAR	A43		B43	+3.3V	3.3V_PCI	
N3	PCI_AD_15	AD[15]	A44		B44	C/BE[1]#	PCI_CBE_1	N1
	3.3V_PCI	+3.3V	A45		B45	AD[14]	PCI_AD_14	N4
T1	PCI_AD_13	AD[13]	A46		B46	GND	GND_SIGNAL	
U2	PCI_AD_11	AD[11]	A47		B47	AD[12]	PCI_AD_12	T2
	GND_SIGNAL	GND	A48		B48	AD[10]	PCI_AD_10	U3
T4	PCI_AD_9	AD[9]	A49		B49	M66EN	3.3V_PCI*	
KEY			A50		B50	KEY		
			A51		B51			
N2	PCI_CBE_0	C/BE[0]#	A52		B52	AD[8]	PCI_AD_8	U4
	3.3V_PCI	+3.3V	A53		B53	AD[7]	PCI_AD_7	T5
T6	PCI_AD_6	AD[6]	A54		B54	+3.3V	3.3V_PCI	
V2	PCI_AD_4	AD[4]	A55		B55	AD[5]	PCI_AD_5	V1
	GND_SIGNAL	GND	A56		B56	AD[3]	PCI_AD_3	V3
V4	PCI_AD_2	AD[2]	A57		B57	GND	GND_SIGNAL	
V5	PCI_AD_0	AD[0]	A58		B58	AD[1]	PCI_AD_1	U5
	VIO	VIO	A59		B59	VIO	VIO	
	3.3V_PCI*	REQ64#	A60		B60	ACK64#	3.3V_PCI*	
	5.0V	+5V	A61		B61	+5V	5.0V	
	5.0V	+5V	A62		B62	+5V	5.0V	

Table 13 - Ethernet FPGA Pin-out

* Pulled up by 4.7k ohm

** PCI_INT is selected by resistor stuffing option R71=INTA(default), R74=INTB, R73=INTC, R76=INTD

3.10 I/O Connectors

The Spartan-3 Evaluation board is an Avalon compliant motherboard that incorporates board-to-board connectors to support Avalon expansion boards. The connection between the Spartan-3 Evaluation board and the Avalon compliant daughter boards is via the Avnet standard AvBus connectors (P4, P5, J7 and J8). The connectors on the topside of the evaluation board (P4, P5) are the host connectors, AMP part number 179031-6. The host connectors, mate with AMP part number 5-179010-6 on the bottom of AvBus daughter cards. Connectors on the bottom side (J7, J8) are AMP part number 5-179010-6 allowing the board to operate as a daughter card as well as a host.. When interfacing to other boards care must be taken to tri-state any signals that could interfere with those of the other board.

3.10.1 AvBus Connectors

The Spartan-3 FPGA is connected to two mirrored 140-pin board-to-board AvBus standard connectors. This means that each signal connected to P5 is mirrored on the opposite side of the board by the same pin number on J8. Similarly, P4 is mirrored by J7. This allows the evaluation board to serve as either motherboard or expansion board in an Avalon system. Note: When used as an expansion board, the Spartan-3 Evaluation board will receive 3.3V from the motherboard. F1 should be removed to prevent the evaluation board from driving this net.

Many of the signals connecting to the AvBus connectors serve alternate functions on the evaluation board so the use must evaluate conflicts when using this interface.

3.10.2 Header "JP7"

The 50-pin header labeled "JP1" on the Spartan-3 Evaluation board is connected to 47 I/O pins on the Spartan-3 FPGA. Pin 48 on the header provides either 3.3V or 5.0V depending on the jumper pad installation on JT6 (3.3V is the default).

3.10.2.1 LVDS

Four pairs of LVDS signals are routed to the 50pin header "JP7" and made available as user I/O. The traces for these signals are routed as differential pairs and are tightly coupled as well as with matched length trace to trace and pair to pair. The signals on the header that separate the LVDS pairs should be tied to ground in the FPGA for maximum performance of the interface. There are no termination resistors on the board so LVDS receivers should utilize DCI termination in the FPGA. LVDS is only supported at 2.5V on the Spartan-3 family FPGAs so the shunt on JP11 should be place between pins 3-4 to select that I/O voltage on Bank5 where the LVDS signals attach.

The tables below show the FPGA connections to these connectors.

Name	FPGA PIN #	Connector PIN #			FPGA PIN #	Name
ADDR0	E22	71		1	-	+5VDC
GND	-	72		2	E21	ADDR1
ADDR3	E20	73		3	D21	ADDR2
ADDR4	D22	74		4	-	GND
GND	-	75		5	D20	ADDR5
ADDR7	D19	76		6	C22	ADDR6
ADDR8	C20	77		7	-	GND
+3.3VDC	-	78		8	C21	ADDR9
ADDR11	G18	79		9	F18	ADDR10
ADDR12	G19	80		10	-	GND
GND	-	81		11	E18	ADDR13
ADDR15	F20	82		12	F19	ADDR14
ADDR16	E19	83		13	-	+5VDC
GND	-	84		14	F21	ADDR17
GPIO_B1_3	F16	85		15	F17	GPIO_B1_0
GPIO_B1_4	E16	86		16	-	GND
GND	-	87		17	E13	GPIO_B1_1
GPIO_B1_5	A12	88		18	F13	GPIO_B1_2
GPIO_B1_6	F12	89		19	-	GND
+3.3VDC	-	90		20	D11	GPIO_B0_0
GPIO_B0_4	F11	91		21	E11	GPIO_B0_1
GPIO_B0_5	C11	92		22	-	GND
GND	-	93		23	E10	GPIO_B0_2
GPIO_B0_6	B10	94		24	C10	GPIO_B0_3
DATA0	U19	95		25	-	+5VDC
GND	-	96		26	T21	DATA1
DATA3	U21	97		27	U20	DATA2
DATA4	V21	98		28	-	GND
GND	-	99		29	V22	DATA5
DATA7	V20	100		30	W22	DATA6
DATA8	Y19	101		31	-	GND
+3.3VDC	-	102		32	W19	DATA9
DATA11	Y20	103		33	V19	DATA10
DATA12	Y21	104		34	-	GND
GND	-	105		35	Y22	DATA13
DATA15	W21	106		36	W20	DATA14
DATA16	M17	107		37	-	+5VDC
GND	-	108		38	L17	DATA17
DATA19	M18	109		39	M19	DATA18
DATA20	M20	110		40	-	GND
GND	-	111		41	N19	DATA21
DATA23	N20	112		42	M21	DATA22
DATA24	T22	113		43	-	GND
+3.3VDC	-	114		44	U18	DATA25
DATA27	R18	115		45	T18	DATA26
DATA28	T17	116		46	-	GND
GND	-	117		47	N21	DATA29
DATA31	M22	118		48	N22	DATA30
GPIO_B2_0	L18	119		49	-	+5VDC
GND	-	120		50	G21	SRAM_CS#
R/W#	K19	121		51	G17	OE#
GPIO_B2_1	L19	122		52	-	GND
GND	-	123		53	B20	GPIO_B1_7
GPIO_B2_2	L20	124		54	C19	GPIO_B1_8
GPIO_B2_3	L21	125		55	-	GND
+3.3VDC	-	126		56	B19	GPIO_B1_9
BE#0	K21	127		57	A19	GPIO_B1_10
BE#1	K22	128		58	-	GND
GND	-	129		59	G22	BE#2
GPIO_B2_4	L22	130		60	K20	BE#3
GPIO_B1_13	A18	131		61	-	+5VDC
GND	-	132		62	D18	GPIO_B1_11
GPIO_B1_14	B18	133		63	C18	GPIO_B1_12
GPIO_B1_15	D17	134		64	-	GND
GND	-	135		65	E17	CLK_OUT
CLK_IN	A11	136		66	AB12	CLK_FB
AVBUS_TMS	-	137		67	-	GND
+3.3VDC	-	138		68	-	AVBUS_TDO
AVBUS_TDI	-	139		69	-	AVBUS_TCK
JTAG_TRST#	-	140		70	-	GND

Table 14 - AvBus Connector "P5" & "J8"Pin-out

Name	FPGA PIN #	Connector PIN #			FPGA PIN #	Name
DVD_G0	F10	71		1	-	+5VDC
GND	-	72		2	E9	DVD_B0
DVD_G1	D10	73		3	F9	DVD_B1
DVD_G2	A10	74		4	-	GND
GND	-	75		5	D7	DVD_B2
DVD_G3	D9	76		6	C7	DVD_B3
DVD_G4	A9	77		7	-	GND
+3.3VDC	-	78		8	E7	DVD_B4
DVD_G5	B9	79		9	F7	DVD_B5
DVD_G6	A8	80		10	-	GND
GND	-	81		11	E6	DVD_B6
DVD_G7	B8	82		12	F6	DVD_B7
DVD_R0	D6	83		13	-	+5VDC
GND	-	84		14	A4	DVD_BLANK
DVD_R1	C6	85		15	A3	DVD_CSYNC
DVD_R2	B6	86		16	-	GND
GND	-	87		17	AA18	SEG1_A
DVD_R3	D5	88		18	Y18	SEG1_B
DVD_R4	A5	89		19	-	GND
+3.3VDC	-	90		20	AA15	SEG1_C
DVD_R5	B5	91		21	V14	SEG1_D
DVD_R6	C5	92		22	-	GND
GND	-	93		23	U14	SEG1_E
DVD_R7	B4	94		24	V17	SEG1_F
GPIO_B5_0	U6	95		25	-	+5VDC
GND	-	96		26	AB18	SEG1_G
GPIO_B5_14	Y6	97		27	AB15	SEG1_Dp
GPIO_B5_3	AA6	98		28	-	GND
GND	-	99		29	AB20	SEG2_A
GPIO_B5_4	U7	100		30	AA20	SEG2_B
GPIO_B5_5	V7	101		31	-	GND
+3.3VDC	-	102		32	AA17	SEG2_C
GPIO_B5_13	W8	103		33	W16	SEG2_D
GPIO_B5_6	AA8	104		34	-	GND
GND	-	105		35	V16	SEG2_E
GPIO_B5_17	AB8	106		36	W18	SEG2_F
GPIO_B5_18	V8	107		37	-	+5VDC
GND	-	108		38	Y17	SEG2_G
GPIO_B5_19	AA9	109		39	W17	SEG2_Dp
GPIO_B5_20	AB9	110		40	-	GND
GND	-	111		41	U12	LED0
GPIO_B5_21	W9	112		42	V12	LED1
GPIO_B5_22	V9	113		43	-	GND
+3.3VDC	-	114		44	Y12	LED2
GPIO_B5_23	AB11	115		45	Y13	LED3
GPIO_B5_24	AB10	116		46	-	GND
GND	-	117		47	AB13	LED4
GPIO_B5_25	AA11	118		48	AA13	LED5
GPIO_B5_26	AA10	119		49	-	+5VDC
GND	-	120		50	V13	LED6
GPIO_B5_27	Y11	121		51	AB14	LED7
GPIO_B5_28	Y10	122		52	-	GND
GND	-	123		53	W1	GPIO_B7_0
GPIO_B5_29	W11	124		54	D1	GPIO_B7_1
GPIO_B5_30	W10	125		55	-	GND
+3.3VDC	-	126		56	D4	GPIO_B7_2
GPIO_B5_31	V11	127		57	C1	GPIO_B7_3
GPIO_B5_32	V10	128		58	-	GND
GND	-	129		59	C2	GPIO_B7_4
GPIO_B5_33	U11	130		60	U13	ANA_REF
GPIO_B5_34	U10	131		61	-	+5VDC
GND	-	132		62	Y16	ANA_OUT
MSDATA	W13	133		63	V18	CMP_OUT
MSCLK	W14	134		64	-	GND
GND	-	135		65	U17	KBCLK
N/C (TP10)	-	136		66	U16	KBDATA
N/C (TP11)	-	137		67	-	GND
+3.3VDC	-	138		68	C3	RS232TX
N/C (TP12)	-	139		69	C4	RS232RX
N/C (TP13)	-	140		70	-	GND

Table 15 - AvBus Connector "P4" & "J7" Pin-out

JP7: Header 25x2					
Pin	FPGA	Signal	Signal	FPGA	Pin
1	U6	GPIO_B5_0	GPIO_B5_7	Y4	2
3	AA5	GPIO_B5_1	GPIO_B5_8	AA3	4
5	AB5	GPIO_B5_2	GPIO_B5_14	Y6	6
7	AA6	GPIO_B5_3	GPIO_B5_9	AB4	8
9	U7	GPIO_B5_4	GPIO_B5_10	AA4	10
11	V7	GPIO_B5_5	GPIO_B5_13	W8	12
13	AA8	GPIO_B5_6	GPIO_B5_15	Y5	14
15	AB8	GPIO_B5_17	GPIO_B5_16	W5	16
17	V8	GPIO_B5_18	GPIO_B5_19	AA9	18
19	AB9	GPIO_B5_20	GPIO_B5_11	W6	20
21	W9	GPIO_B5_21	GPIO_B5_12	V6	22
23	V9	GPIO_B5_22	GPIO_B5_23	AB11	24
25	AB10	GPIO_B5_24	GPIO_B5_25	AA11	26
27	AA10	GPIO_B5_26	GPIO_B5_27	Y11	28
29	Y10	GPIO_B5_28	GPIO_B5_29	W11	30
31	W10	GPIO_B5_30	GPIO_B5_31	V11	32
33	V10	GPIO_B5_32	GPIO_B5_33	U11	34
35	U10	GPIO_B5_34	LED6	V13	36
37	AB13	LED4	LED5	AA13	38
39	Y13	LED3	SWITCH3	Y2	40
41	Y12	LED2	SWITCH2	Y3	42
43	V12	LED1	SWITCH1	W3	44
45	U12	LED0	SWITCH0	W4	46
47	AJ15	CLK_HD	3.3V/5.0V	-	48
49	-	Ground	Ground	-	50

Table 16 - Header "JP7" Pin-out

Note: Shaded pin pairs are routed for LVDS.

3.11 Power

The Spartan-3 Evaluation board uses a 5V AC/DC adapter (supplied with the kit) with center positive barrel connector. The 5V is used as the input to a TI PT5401A power module, which provides 3.3VDC. Two National Semiconductor LP3966-ADJ parts provide 2.5V and 1.2V. The barrel connector "J9" is shown below in Figure 9.

IMPORTANT:
Note that there is **no protection for reverse power supply polarity** so take necessary precautions to ensure that the center pin is 4.5V – 5.5V, and the ring is ground!

When powering the Spartan-3 evaluation board from the AvBus or PCI connectors remove the fuse F1 to prevent contention on the 3.3V rail.

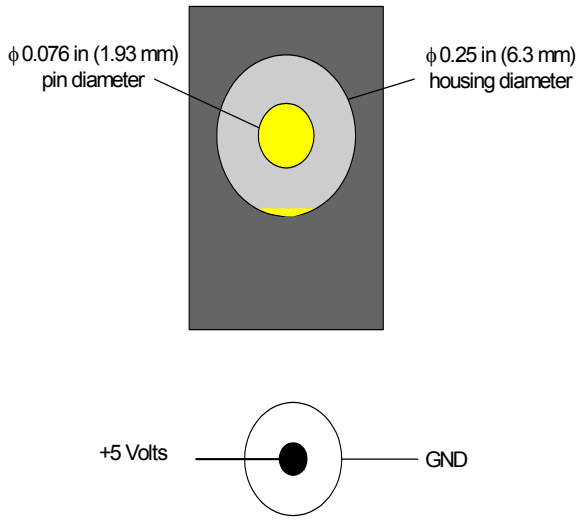


Figure 9 - Barrel Power Connector "J9"

3.12 Configuration

The Spartan-3 Evaluation board supports only Boundary-scan programming form a host and Master Serial mode programming from the PROMs. The boundary-scan chain of this board includes the FPGA and the PROM/s. Additional components attached through the AvBus or PCI connectors can be included in this chain by setting the appropriate jumpers on the board. The header "JP4" is used to include components from the AvBus and "JT7" and "JT8" are used to include PCI connected devices. Review the schematics and the table below for more information.

If the Spartan-3 evaluation board is not the host board and the JTAG chain is driven by an alternate source place a shunt on pins 4-5 of the header "JP5" to close the chain.

"JP4" JTAG Chain Selection – Jumper Settings	
Pins 2-3	**Standalone Mode** – Spartan-3 and PROM/s
Pins 1-2 and 4-5	Add AvBus P5 Connector to standalone
Pins 1-2, 3-4 and 5-6	Add AvBus J8 Connector to standalone
Pins 1-2 and 5-6	Add both AvBus Connectors to standalone

Table 17 - JTAG Chain Selection "JP15"

4.0 Source Code/EDK Projects

This section of the manual describes the source code and example projects included in the kit. The hardware interfaces discussed in the previous section can be implemented very quickly as peripherals in a processor system. Putting the Xilinx MicroBlaze™ soft processor core into the Spartan-3 FPGA and connecting the hardware interfaces to the peripheral bus of the MicroBlaze processor creates a complete test system. There are several benefits to using MicroBlaze for test purposes. Using a MicroBlaze system provides the user with a debug terminal to easily access control and data registers of multiple hardware interfaces by running very simple C code and using the UART peripheral. Hardware modules that are created with the peripheral bus interface (On-chip Peripheral Bus or OPB) are portable and can easily be re-used in later designs. Xilinx provides a standard set of peripherals for commonly used interfaces so the designer can focus his/her time and energy on the IP that differentiates the design from the competition. This kit includes complete example projects that implement MicroBlaze processor systems, but also includes VHDL/Verilog source code for the more traditional FPGA designer.

4.1 What is included

The example source code used to validate the hardware interfaces is included. Some of the source code was written in VHDL and some in Verilog. The MicroBlaze example projects included in the Spartan-3 Evaluation Kit were created in the Xilinx Embedded Development Kit (EDK) version 6.1. The examples include the Xilinx Platform Studio (XPS) project files and supporting directory structures, all of the required files to run the XPS projects. The user must have both the Xilinx Integrated Software Environment (ISE) version 6.1 and the EDK version 6.1 software installed to utilize the example projects. The following list provides an outline of the Source Code/EDK Projects section. All of the example code/projects are included on the Spartan-3 Evaluation Kit CD.

- Source Code
  - Mouse Interface (PS2)
  - Video DAC Interface (VHDL)
  - Analog Comparator (Verilog)
  - LED Segment Display (VHDL)
- XPS Example Projects
  - Hello World
  - External Memory Project
  - Multi-Peripheral Project
- Video/Mouse Game

4.2 Source Code: Mouse Interface

The Mouse Interface code retrieves the position and button information from the mouse over the standard PS2 interface. The Mouse code consists of three source files: "ps2_mouse_interface.vhd", "simple_mouse_module.vhd" and "opb_simple_mouse.vhd". The "ps2_mouse_interface.vhd" module provides the low-level interface to the mouse and contains the state machines to initialize, write commands and capture data to/from the PS2 interface. The "simple_mouse_module.vhd" source takes the captured data from the low-level module and stores it into registers for user access. The registers are accessible by a generic memory bus interface with the following memory map.

Register	Address	Type	Description
Revision	0x0000	RO	Source code revision register
Status	0x0004	RO	Mouse status
Data	0x0008	RO	Mouse position data
General Purpose	0x000C	R/W	General purpose register

Table 18 - Mouse Memory Map

The following tables provide descriptions of the user registers. The General Purpose register is not tied to any logic. It is just a placeholder in the memory map for expansion purposes.

Bits	Name	Description	Reset Value
31:0	Revision	Source code revision	0x00000005

Table 19 - Mouse Revision Register

Bits	Name	Description	Reset Value
31:4	Unused	Not used	0x0000000
3	Error_no_ack	Mouse acknowledge error flag	0
2	Left_button	Indicates left mouse click	0
1	Right_button	Indicates right mouse click	0
0	Data_ready	Data register valid indicator	0

Table 20 - Mouse Status Register

Bits	Name	Description	Reset Value
31:30	Unused	Not Used	00
29	Left_button	Indicates left mouse click	
28	Right_button	Indicates right mouse click	
27:25	Unused	Not Used	000
24:16	X_increment	Position data, x-coordinate	
15:9	Unused	Not Used	0x00
8:0	Y_increment	Position data, y-coordinate	

Table 21 - Mouse Data Register

The remaining source file "opb_simple_mouse.vhd" is an optional wrapper file that provides the address translation and handshaking signals to make the mouse design into an On-chip Peripheral Bus (OPB) peripheral for use with the MicroBlaze soft processor. This file is not necessary if the MicroBlaze processor is not being used. To see an example of the Mouse Interface code running on the Spartan-3 Evaluation Board, download the "mouse_test.bit" file to the FPGA and connect a PS2 mouse to either or both of the mini-DIN connectors on the board. Also connect a VGA monitor to the DB15 connector (P2). This bit file is from the Multi-Peripheral Project discussed below.

4.3 Source Code: Video DAC Interface

The Video DAC Interface code outputs a digital representation of RGB color bars to the on-board triple video DAC with the appropriate timing and synchronization signals for a 640 x 480 VGA monitor. The video code also displays three "boxes" of variable size and color. The Video code consists of three source files: "vbars.vhd", "simple_colorbars_module.vhd" and "opb_simple_colorbars.vhd". The "vbars.vhd" source file provides the low-level interface to the video DAC. It generates the RGB video data for the color bars on the fly and the synchronization signals for the monitor. The 640 x 480 display is essentially a 480-row by 640-column matrix that is drawn one row at a time left to right, top to bottom. Upon reaching the right extremity (n, 640) the beam is blanked (turned off), returned to the left hand edge (horizontal retrace), and positioned to draw the next line. Upon reaching the bottom right extremity (480, 640) the beam is blanked and returned to the top left (0, 0) of the screen (vertical retrace). Additional (un-displayed) overhead associated with display timing increases the 640 x 480 display to 800 x 525 "pixel times". The "vbars.vhd" code also inserts three box shapes into the color bar display. The boxes are created by specifying the x-coordinates (min and max) and y-coordinates (min and max) of where the box is to be displayed in the visible image, and a RGB value for the color of the box. The "simple_colorbars_module.vhd" file creates a register interface to "vbars" design for user access. The registers are accessible by a generic memory bus interface with the following memory map.

Register	Address	Type	Description
Revision	0x0000	RO	Source code revision register
Status	0x0004	RO	Video status
Data	0x0008	R/W	Background data
Control	0x000C	R/W	Video module control
Pointer_x_reg	0x0010	R/W	Box 1: x-coordinates
Pointer_y_reg	0x0014	R/W	Box 1: y-coordinates
Pointer_val_reg	0x0018	R/W	Box 1: color
Pointer2_x_reg	0x0020	R/W	Box 2: x-coordinates
Pointer2_y_reg	0x0024	R/W	Box 2: y-coordinates
Pointer2_val_reg	0x0028	R/W	Box 2: color
Pointer3_x_reg	0x0030	R/W	Box 3: x-coordinates
Pointer3_y_reg	0x0034	R/W	Box 3: y-coordinates
Pointer3_val_reg	0x0038	R/W	Box 3: color

Table 22 - Video Memory Map

The following tables provide descriptions of the user registers.

Bits	Name	Description	Reset Value
31:0	Revision	Source code revision	0x00000005

Table 23 - Video Revision Register

Bits	Name	Description	Reset Value
31:0	Status	Place holder for status info	0xA5A5A5A5

Table 24 - Video Status Register

Bits	Name	Description	Reset Value
31:24	Unused	Not used	0x00
23:0	Background_value	RGB value for background color	0x000000 (black)

Table 25 - Video Data Register

b

Bits	Name	Description	Reset Value
31:1	Unused	Not used	0x5A5A5A5
0	Show_colorbars	'1' – color bars, '0'- background	0x1

Table 26 - Video Control Register

Bits	Name	Description	Reset Value
31:26	Unused	Not used	0x0
25:16	X_max	Right boundary, offset from 0	0x12C (300)
15:10	Unused	Not used	0x0
9:0	X_min	Left boundary, offset from 0	0x0C8 (200)

Table 27 - Video Box 1: X-coordinates

Bits	Name	Description	Reset Value
31:26	Unused	Not used	0x0
25:16	Y_max	Top boundary, offset from 0	0x12C (300)
15:10	Unused	Not used	0x0
9:0	Y_min	Bottom boundary, offset from 0	0x0C8 (200)

Table 28 - Video Box 1: Y-coordinates

Bits	Name	Description	Reset Value
31:24	Unused	Not used	0x00
23:0	RGB_value	Box 1 Color (0xRRGGBB)	0xFFFFFF (white)

Table 29 - Video Box 1: Color

Bits	Name	Description	Reset Value
31:26	Unused	Not used	0x0
25:16	X_max2	Right boundary, offset from 0	0x00F (15)
15:10	Unused	Not used	0x0
9:0	X_min2	Left boundary, offset from 0	0x000 (0)

Table 30 - Video Box 2: X-coordinates

Bits	Name	Description	Reset Value
31:26	Unused	Not used	0x0
25:16	Y_max2	Top boundary, offset from 0	0x12C (300)
15:10	Unused	Not used	0x0
9:0	Y_min2	Bottom boundary, offset from 0	0x0C8 (200)

Table 31 - Video Box 2: Y-coordinates

Bits	Name	Description	Reset Value
31:24	Unused	Not used	0x00
23:0	RGB_value2	Box 2 Color (0xRRGGBB)	0x0000FF (blue)

Table 32 - Video Box 2: Color

Bits	Name	Description	Reset Value
31:26	Unused	Not used	0x0
25:16	X_max3	Right boundary, offset from 0	0x280 (640)
15:10	Unused	Not used	0x0
9:0	X_min3	Left boundary, offset from 0	0x271 (625)

Table 33 - Video Box 3: X-coordinates

Bits	Name	Description	Reset Value
31:26	Unused	Not used	0x0
25:16	Y_max3	Top boundary, offset from 0	0x12C (300)
15:10	Unused	Not used	0x0
9:0	Y_min3	Bottom boundary, offset from 0	0x0C8 (200)

Table 34 - Video Box 3: Y-coordinates

Bits	Name	Description	Reset Value
31:24	Unused	Not used	0x00
23:0	RGB_value3	Box 3 Color (0xRRGGBB)	0xFF0000 (red)

Table 35 - Video Box 3: Color

The remaining source file "opb_simple_colorbars.vhd" is an optional wrapper file that provides the address translation and handshaking signals to make the video design into an On-chip Peripheral Bus (OPB) peripheral for use with the MicroBlaze soft processor. This file is not necessary if the MicroBlaze processor is not being used. To see an example of the Video Interface code running on the Spartan-3 Evaluation Board, download the "video_test.bit" file to the FPGA and connect a VGA monitor to the DB15 connector (P2). This bit file is from the Multi-Peripheral Project discussed below.

4.4 Source Code: Analog Comparator

The Analog Comparator code implements the Delta-Sigma Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) discussed in Xilinx application notes 154 and 155 (XAPP154 and XAPP155), respectively. The synthesizable Delta-Sigma DAC only requires two external components, a resistor and capacitor for a first-order low-pass filter. The ADC design requires an external analog comparator like the National Semiconductors LMV7235 populated on the Spartan-3 Evaluation board and a first-order low-pass filter. The output of the DAC is used for the negative input to the comparator (reference voltage). The user supplies an analog signal to the positive input of the comparator via JP10 pin 1. The output of the comparator is then converted by the ADC and fed back to the input of the DAC. The Analog Comparator code consists of four source files: "dac.v", "adc.v", "adc_module.vhd" and "opb_adc_comp.vhd". The "dac.v" module was taken from a Xilinx application note, see "XAPP154: Virtex Synthesizable Delta-Sigma DAC" for more information. Likewise, the "adc.v" module is from a Xilinx application note, see "XAPP155: Virtex Analog to Digital Converter" for more information. Please use the source files included on the CD and not directly from the application note. The source code embedded in the appnote has some minor syntax errors and font conversion issues that have been corrected in the files on the CD. The "adc_module.vhd" is a wrapper file around the "dac.v" and "adc.v" modules, which provides a register interface to the design for user control and access. The registers are accessible by a generic memory bus interface with the following memory map.

Register	Address	Type	Description
Control	0x0000	R/W	ADC control register
Data	0x0004	RO	ADC sample data register

Table 36 - Analog Comparator Memory Map

The following tables provide descriptions of the user registers.

Bits	Name	Description	Reset Value
31:6	Unused	Not used	0x000000
5:2	Fstm	Filter settle time multiplier	0x4
1	ADCsampled	Indicates ADC data ready	0
0	Sample	Indicates MSB is being sampled	0

Table 37 - Analog Comparator Control Register

Bits	Name	Description	Reset Value
31:7	Unused	Not used	0x000000
6:0	ADCout	ADC output data	0x00

Table 38 - Analog Comparator Data Register

Since the wrapper file was written in VHDL and the design files are Verilog, a mixed-mode synthesis tool is required to synthesize the design that includes the user registers. An alternative would be to use the "adc" design in netlist form (synthesize it separately with a Verilog synthesis tool) along with the VHDL wrapper in a VHDL synthesis tool. The netlist for the "adc" design is included on the CD in NGC format.

The remaining source file "opb_adc_comp.vhd" is an optional wrapper file that provides the address translation and handshaking signals to make the analog comparator design into an On-chip Peripheral Bus (OPB) peripheral for use with the MicroBlaze soft processor. This file is not necessary if the MicroBlaze processor is not being used. To see an example of the Analog Comparator code running on the Spartan-3 Evaluation Board, download the "analog_test.bit" file to the FPGA and connect an analog signal to JP10 pin 1 (voltage level must be between 0 and 3.3V). Connect the board to a serial port of a PC and open a terminal session configured for 19200 baud. This bit file is from the Multi-Peripheral Project discussed below.

4.5 Source Code: LED Segment Display Interface

The LED Segment Display code drives the necessary LED segments to display either decimal or hexadecimal numbers. The LED Segment Display code consists of three source files: "vec2display.vhd", "dual_7_seg_module.vhd" and "opb_dual_7_seg.vhd". The "vec2display.vhd" module does the number conversion from binary to either decimal or hexadecimal depending on the mode selected by the user. A third mode bypasses the conversion and directly drives the LED segments. The "dual_7_seg_module.vhd" source provides a register interface for user control and data. The registers are accessible by a generic memory bus interface with the following memory map.

Register	Address	Type	Description
Data	0x0000	R/W	LED Data (byte) register
Mode	0x0004	R/W	Conversion mode register

Table 39 - LED Display Memory Map

The following tables provide descriptions of the user registers.

Bits	Name	Description	Reset Value
31:16	Unused	Not used	0x0000
15:8	Display1	Data to be displayed (bypass only)	0x00
7:0	Display	Data to be displayed (hex/dec conv.)	0x00

Table 40 - LED Display Data Register

Bits	Name	Description	Reset Value
31:2	Unused	Not used	0x000000
1:0	Mode	"00"-decimal, "01"-hex, "10"-bypass	0x00

Table 41 - LED Display Mode Register

The "Display1" portion of the Data Register is only used during bypass mode to directly drive the tens digit. For decimal or hexadecimal conversion modes, only the least significant byte of the Data Register ("Display") is converted and displayed.

The remaining source file "opb_dual_7_seg.vhd" is an optional wrapper file that provides the address translation and handshaking signals to make the LED segment display design into an On-chip Peripheral Bus (OPB) peripheral for use with the MicroBlaze soft processor. This file is not necessary if the MicroBlaze

processor is not being used. To see an example of the LED Segment Display code running on the Spartan-3 Evaluation Board, download the "led_test.bit" file to the FPGA. Connect the board to a serial port of a PC and open a terminal session configured for 19200 baud. Type 'help' at the prompt for a list of commands. This bit file is from the Multi-Peripheral Project discussed below.

4.6 EDK Project: Hello World

This example is intended to be as simple as possible in order to introduce the user to the board and Xilinx Platform Studio (XPS) tools. The design consists primarily of the processor and a UART that is set up as the standard I/O device. This will allow print commands to be displayed on a terminal interface.

The entire tool flow is within the XPS environment. The user may generate a netlist for the hardware system, compile the test software and create a bit file updated with the software all from within XPS. The user may even download the bit file to the evaluation board from XPS using a download cable. See Section 2.2 for instructions on how to set up a download cable for configuration. The user can make a change to the software, re-compile and re-generate a bit file without having to run through synthesis and implementation over again. To do this, select "Compile Program Sources" and then "Update Bitstream". Finally just download the bit file to the board using the "Download" option.

A datasheet has been created for each example project. See the "Hello World" datasheet for more information on how to the use the Hello World Project.

4.7 EDK Project: External Memory Project

This example uses the On-chip Peripheral Bus (OPB) to interface with the External Memory Controller (EMC), which is a standard peripheral included in the EDK. The peripheral handles all transactions between the OPB and the off-chip SRAM memory, allowing the MicroBlaze to access the 1 MB memory. The timing parameters of the EMC peripheral have been specifically set up for the Cypress SRAM device on the Spartan-3 Evaluation board. The OPB clock frequency is set for 66MHz, since the 66MHz oscillator input is being used. The timing parameters stay the same regardless of the bus frequency. The peripheral automatically generates the specified timing using the specified bus frequency.

The External Memory Project includes simple C code that is executed by the MicroBlaze processor to perform testing of the SRAM memory and report the results to a terminal interface. The code also provides the ability to do basic read and write transactions. Internal Block RAM (BRAM) in the Spartan-3 FPGA is used for instruction and data code storage. The BRAM is connected to the Local Memory Bus (LMB) of the MicroBlaze processor and controlled by the BRAM Controller peripheral, which is another standard peripheral in EDK. Two instances of the BRAM controller are needed for the instruction and data sides of the LMB. The memory map for the peripherals in this project is shown below.

Processor Bus	Peripheral	Address Location
LMB	BRAM Controller (ILMB)	0x00000000 – 0x00003FFF
	BRAM Controller (DLMB)	0x00000000 – 0x00003FFF
OPB	EMC	0x85000000 – 0x850FFFFF
	UART (lite)	0xFFFF8000 – 0xFFFF80FF

Table 42 - External Memory Project - Memory Map

Like the Hello World Project, the processor system for the Memory Project is a top-level design. This means that the entire design flow is within XPS. However, XPS does use ISE in the background to perform implementation functions so the ISE tool must be installed.

The zero bit is the left-most or most significant bit on a MicroBlaze bus. Therefore busses in the hardware description file are defined as 0 to 31, for example. To align the busses properly with the external memory,

the SRAM bus signals were swapped end-for-end or mirrored in the user constraint file (system.ucf file in the "data" folder) of the External Memory Project. This is transparent to the software.

A datasheet has been created for each example project. See the "External Memory Example" datasheet for more information on how to use the External Memory Project.

4.8 EDK Project: Multi-Peripheral Project

This project makes use of several custom OPB peripherals designed by Avnet Design Services to enable the MicroBlaze processor to access the various hardware interfaces on the Spartan-3 Evaluation board. The optional OPB wrapper code was applied to the source code discussed in the previous sections to add an OPB interface to the user registers of the designs. When combined with the required peripheral definition files (MPD, PAO, BBD), the designs become OPB peripherals. See the Embedded Systems Tools Guide (EST Guide) in the \EDK\doc folder for more information about creating peripherals. The custom peripherals that are being used in this project can be found in the "pcores" folder. The memory-map for all of the peripherals in this project, both custom and standard, is shown below.

Processor Bus	Peripheral	Address Location
LMB	BRAM Controller (ILMB)	0x00000000 – 0x00003FFF
	BRAM Controller (DLMB)	0x00000000 – 0x00003FFF
	BRAM Controller2 (ILMB)	0x00004000 – 0x00005FFF
	BRAM Controller2 (DLMB)	0x00004000 – 0x00005FFF
OPB	EMC (SRAM)	0x85000000 – 0x850FFFFF
	Simple Mouse	0x86000000 – 0x860000FF
	Simple Mouse2	0x87000000 – 0x870000FF
	Dual 7-Segment LED	0x88000000 – 0x880000FF
	Simple Color Bars	0x89000000 – 0x890000FF
	ADC Comparator	0x90000000 – 0x900000FF
	GPIO (LEDs)	0xFFFF0100 – 0xFFFF01FF
	GPIO2 (Switches)	0xFFFF0200 – 0xFFFF02FF
	UART (lite)	0xFFFF8000 – 0xFFFF80FF

Table 43 - Multi-Peripheral Project Memory-Map

To use the Multi-Peripheral design, download the "multi_periphal.bit" file to the FPGA and connect the board to a PC via a serial cable. Open a terminal session (19200-8-N-1-N) and type 'help' <enter> at the prompt to see a list of commands. The "Multi-Peripheral Project" document in the Multi-Peripheral Project directory discusses the memory map and use of the custom peripherals in greater detail.

4.9 Video/Mouse Game

The Video/Mouse Game demonstrates how the video and mouse source code can be used to create a simple application using the MicroBlaze processor. To run the demo, plug two PS2 mouse devices into the two PS2 connectors (JS1 and JS2). Next plug a VGA monitor into the DB15 connector (P2) and connect the board to a PC via a serial cable. Download the "video_game.bit" file to the FPGA and connect the board to a PC via a serial cable. Open a terminal session (19200-8-N-1-N) and type 'pong' <enter> at the prompt to start the game.

The EDK project for the Video/Mouse Game is included on the CD under the "Demo" folder for reference. It is also possible to network two Spartan-3 Evaluation boards together using Ethernet. On the terminal session for the second board, type 'pong2' <enter> to join the game session.

5.0 List of partners