# Flash Expansion Module User Guide



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# 1.0 Introduction

The purpose of this manual is to provide the information required to implement a functional design using the AvBus FLASH Expansion Module from Avnet Electronics Marketing. This document includes a description of the hardware and a pin-out for the AvBus connector.

### 1.1 Description

The AvBus Flash Expansion Module provides non-volatile storage of data for compatible host boards. This document will talk only about the AvBus Flash Expansion Module itself and not the host boards because it is compatible with any AvBus host connector that has the required interface signals available.

### 1.2 Features

### **Board I/O Connectors**

— 140-pin general-purpose I/O expansion connectors (AvBus)

### Memory

- 16 MB Flash
  - o Micron MT28F640J3 Q-Flash or
  - TE28F640J3 Strata Flash

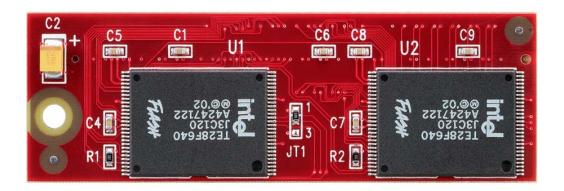


Figure 1 - AvBus Flash Expansion Module Picture

## 1.3 Ordering Information

The following table lists the evaluation kit part numbers and available software options. Internet link at <a href="http://www.em.avnet.com/ads">http://www.em.avnet.com/ads</a>

Part Number	Hardware		
ADS-FLASH-DAU	AvBus Flash Expansion Memory		

**Table 1 - Ordering Information** 

# 2.0 User Information

This section provides the user with information on how to get started using the AvBus Flash Expansion Module with a compatible host board.

### 2.1 Memory

The AvBus Flash Expansion Module is populated with two 64Mb Flash memory devices configured as 4Mx32bit. The board was designed to support the 128Mb devices as well but will not be offered in that configuration.

Write protection is provided for on this board via a 3-pin surface mount resistor jumper (JT1). To protect the programmed data, use a soldering iron to move the 0 ohm resistor from the default position across pins 2-3 to pins 1-2.

### 2.2 AvBus I/O Connector

The AvBus Flash Expansion Module is an Avnet Avenue compliant daughter card with a standard memory bus pin out to allow its use with a variety of host boards. The Avnet standard AvBus receptacle connector (P1) is a Tyco (AMP) part number 5-179010-6 which when mated with the plug connector Tyco (AMP) part number 179031-6 provides a 16mm stacking height above the host board. If this stacking height interferes with other boards or connectors in your system the receptacle connector can be replaced with either 5-179009-6 or 177983-6 to provide 12mm or 8mm stacking heights respectively.

Table 2 on the following page shows the connections between the AvBus connector and the Flash components. The two Flash components are strapped in Word mode for 32-bit data accesses (the BYTE# mode pins are tied to VCC and the least significant address pins are tied to GND). This addressing mode is typically used for 32-bit microprocessors or applications with a 32-bit data bus and no byte selects. The AvBus signal "ADDR2" becomes the least significant address bit (wired to Flash address pin A1). Please note that the AvBus data bus signals are bit swapped with respect to the Flash pin names. Reference the included schematic for further details.

Figure 2 provides additional information for the specific case where the host board is running an embedded processor in a Xilinx FPGA and interfacing to the Flash Module using the "External Memory Controller" peripheral included in the Xilinx Embedded Development Kit (EDK) software. Note: The pin LOCs in your UCF file for the Flash ports are intuitive except for the address pins, which are bit-swapped and connect like this: (ADDR24 is not used for 64 Mb devices) "xx Mem A pin<8>"=ADDR23, "xx Mem A pin<9>"=ADDR22, ..., "xx Mem A pin<29>"=ADDR2.

```
#·Flash
PORT fpga_0_FLASH_Mem_DQ_pin = fpga_0_FLASH_Mem_DQ, DIR = INOUT, VEC = [0:31]
PORT fpga_0_FLASH_Mem_A_pin = fpga_0_FLASH_Mem_A, DIR = OUTPUT, VEC = [8:29]
PORT fpga_0_FLASH_Mem_WEN_pin = fpga_0_FLASH_Mem_WEN, DIR = OUTPUT
 ·<mark>PORT</mark>·fpga_0_FLASH_Mem_OEN_pin·=·fpga_0_FLASH_Mem_OEN,·DIR·=·OUTPUT,·VEC·=·[0:0]
 ·<u>PORT</u>·fpga_0_FLASH_Mem_CEN_pin·=·fpga_0_FLASH_Mem_CEN,·DIR·=·OUTPUT,·VEC·=·[0:0]
 ·PORT fpga_0_FLASH_Mem_RPN_pin = fpga_0_FLASH_Mem_RPN, DIR = OUTPUT
BEGIN opb_emc
 ·<del>PARAMETER</del>·INSTANCE·=·my_flash
·PARAMETER·HW_VER·=·2.00.a
·PARAMETER·C_OPB_CLK_PERIOD_PS·=·10000
·PARAMETER·C_SYNCH_MEM_0·=·0
PARAMETER C_NUM_BANKS_MEM = 1
PARAMETER C_TAVDV_PS_MEM_0 = 120000
PARAMETER C_TAVDV_PS_MEM_0 = 120000
PARAMETER C_TWP_PS_MEM_0 = 120000
PARAMETER C_TWC_PS_MEM_0 = 120000
PARAMETER C_THZCE_PS_MEM_0 = 35000
PARAMETER C_TLZWE_PS_MEM_0 = 35000
PARAMETER C_THZOE_PS_MEM_0 = 15000
PARAMETER C_FAMILY = VIRTEX4
 ·PARAMETER·C_MAX_MEM_WIDTH·=·32
PARAMETER C_MEMO_WIDTH = 32
PARAMETER C_INCLUDE_DATAWIDTH_MATCHING_0 = 0
PARAMETER C_MEMO_BASEADDR = 0x94000000
PARAMETER C_MEMO_HIGHADDR = 0x94ffffff
 ·<del>PORT</del>·Mem_A·=·fpga_O_FLASH_Mem_A_split
·PORT·Mem_DQ·=·fpga_0_FLASH_Mem_DQ
· PORT · Mem_CEN · = · f pga_0_FLASH_Mem_CEN
· PORT · Mem_OEN · = · fpga_O_FLASH_Mem_OEN
 ·<del>PORT</del>·Mem_WEN·=·fpga_0_FLASH_Mem_WEN
 ·<del>PORT</del>·Mem_RPN·=·fpga_0_FLASH_Mem_RPN
·BUS_INTERFACE · SOPB · = · mb_opb
END
BEGIN util_bus_split
• PARAMETER · INSTANCE · = · FLASH_util_bus_split_0
PARAMETER HW_VER = 1.00.a
PARAMETER C_SIZE_IN = 32
PARAMETER C_LEFT_POS = 8
PARAMETER C_SPLIT = 30
·PORT·Sig·=·fpga 0 FLASH Mem A split
·PORT·Out1·=·fpga_0_FLASH_Mem_A
END
```

Figure 2 - Example MHS Instance (EMC)

The JTAG signals (TDI, TDO, TCK, TMS & TRST#) depicted in the following table are not used on the board. They are provided for reference only.

Signal Name	FLASH PIN#	AvBu	AvBus PIN#		FLASH PIN#	Signal Name
ADDR0	N/C	71		1	-	+5VDC
GND	-	72		2	N/C	ADDR1
ADDR3	U1/2-27	73		3	U1/2-28	ADDR2
ADDR4	U1/2-26	74		4	- III/2 25	GND
GND ADDR7	- U1/2-23	75 76		5 6	U1/2-25 U1/2-24	ADDR5 ADDR6
ADDR7	U1/2-23 U1/2-22	77		7	-	GND
+3.3VDC	-	78		8	U1/2-20	ADDR9
ADDR11	U1/2-18	79		9	U1/2-19	ADDR10
ADDR12	U1/2-17	80		10	-	GND
GND	-	81		11	U1/2-13	ADDR13
ADDR15	U1/2-11	82		12	U1/2-12	ADDR14
ADDR16 GND	U1/2-10	83 84		13 14	- U1/2-8	+5VDC ADDR17
ADDR19	U1/2-6	85		15	U1/2-7	ADDR17
ADDR20	U1/2-5	86		16	-	GND
GND	-	87		17	U1/2-4	ADDR21
ADDR23	U1/2-1	88		18	U1/2-3	ADDR22
ADDR24	U1/2-30	89		19	-	GND
+3.3VDC	- NI/C	90		20	N/C	ADDR25
ADDR27 ADDR28	N/C N/C	91 92		21 22	N/C	ADDR26 GND
GND	-	93		23	N/C	ADDR29
ADDR31	N/C	94		24	N/C	ADDR30
DATA0	U2-52	95		25	-	+5VDC
GND	-	96		26	U2-50	DATA1
DATA3	U2-45	97		27	U2-47	DATA2
DATA4	U2-41	98		28	-	GND
GND DATA7	U2-34	99 100		29 30	U2-39	DATA5 DATA6
DATA/	U2-54 U2-51	100		31	U2-36	GND
+3.3VDC	-	102		32	U2-49	DATA9
DATA11	U2-44	103		33	U2-46	DATA10
DATA12	U2-40	104		34	-	GND
GND	-	105		35	U2-38	DATA13
DATA15	U2-33	106		36	U2-35	DATA14
DATA16 GND	U1-52	107 108		37 38	- U1-50	+5VDC DATA17
DATA19	U1-45	109		39	U1-47	DATA17 DATA18
DATA20	U1-41	110		40	-	GND
GND	-	111		41	U1-39	DATA21
DATA23	U1-34	112		42	U1-36	DATA22
DATA24	U1-51	113		43	-	GND
+3.3VDC	- TT1 44	114		44	U1-49	DATA25 DATA26
DATA27 DATA28	U1-44 U1-40	115 116		45 46	U1-46	GND
GND	-	117		47	U1-38	DATA29
DATA31	U1-33	118		48	U1-35	DATA30
N/C		119		49		+5VDC
GND	-	120		50		N/C
R/W#	U1/2-55	121		51	U1/2-54	OE#
N/C GND	-	122 123		52 53	- U1/2-14	GND Flash_CS#
N/C	-	123		53	U1/2-14 U1/2-16	Flash Reset#
N/C		125		55	-	GND
+3.3VDC	-	126		56		N/C
N/C		127		57		N/C
N/C		128		58	-	GND
GND	-	129		59		N/C
N/C N/C		130 131		60		N/C +5VDC
GND	_	131		62	-	+5VDC N/C
N/C		133		63		N/C
N/C		134		64	-	GND
GND	-	135		65		N/C
N/C		136		66		N/C
TMS	-	137		67	-	GND
+3.3VDC TDI	-	138 139		68 69	-	TDO TCK
TRST#	-	140		70	-	GND
1130111	1	2.10		, 0	1	0.10

Table 2 - AvBus P1 Pin-out