SRAM Expansion Module
User Guide

AVNET electronics marketing

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1.0 Introduction

The purpose of this manual is to provide the information required to implement a functional design using the AvBus SRAM Expansion Module from Avnet Electronics Marketing. This document includes a description of the hardware and a pin-out for the AvBus connector.

1.1 Description

The AvBus SRAM Expansion Module provides high speed synchronous data storage for compatible host boards. This document will talk only about the AvBus SRAM Expansion Module itself and not the host boards because it is compatible with any AvBus host connector that has the required interface signals available.

1.2 Features

Board I/O Connectors

— 140-pin general-purpose I/O expansion connectors (AvBus)

Memory

— Sync Burst SRAM – 1MByte

- GSI Technologies - GS88032BT-150

Figure 1 - AvBus SRAM Expansion Module Picture

1.3 Ordering Information

The following table lists the evaluation kit part numbers and available software options.
Internet link at http://www.em.avnet.com/ads

Part Number	Hardware
ADS-SRAM-DAU	AvBus SRAM Expansion Module

Table 1 - Ordering Information

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2.0 User Information

This section provides the user with information on how to get started using the AvBus SRAM Expansion Module with a compatible host board. There are no movable jumpers on this board.

2.1 Memory

The AvBus SRAM Expansion Module is populated with an 8Mb Synchronous Burst SRAM memory device configured as 256Kx32bit. The board was designed to potentially support larger devices by connecting all available address pins on the TQFP package. However, the Expansion Module will not be offered in any other configuration.

Each unique address selects a 32-bit Word. The sleep mode pin “ZZ” is tied low in hardware so the only way to invoke sleep mode is to stop the clock. The chip enables pins “E2” and “E3#” are tied high and low, respectively. The -150 speed grade supports cycle times of 6.7 ns in pipeline mode (3-1-1-1) and 7.5 ns in flow-through mode (2-1-1-1).

The tables below are from the GSI data sheet.

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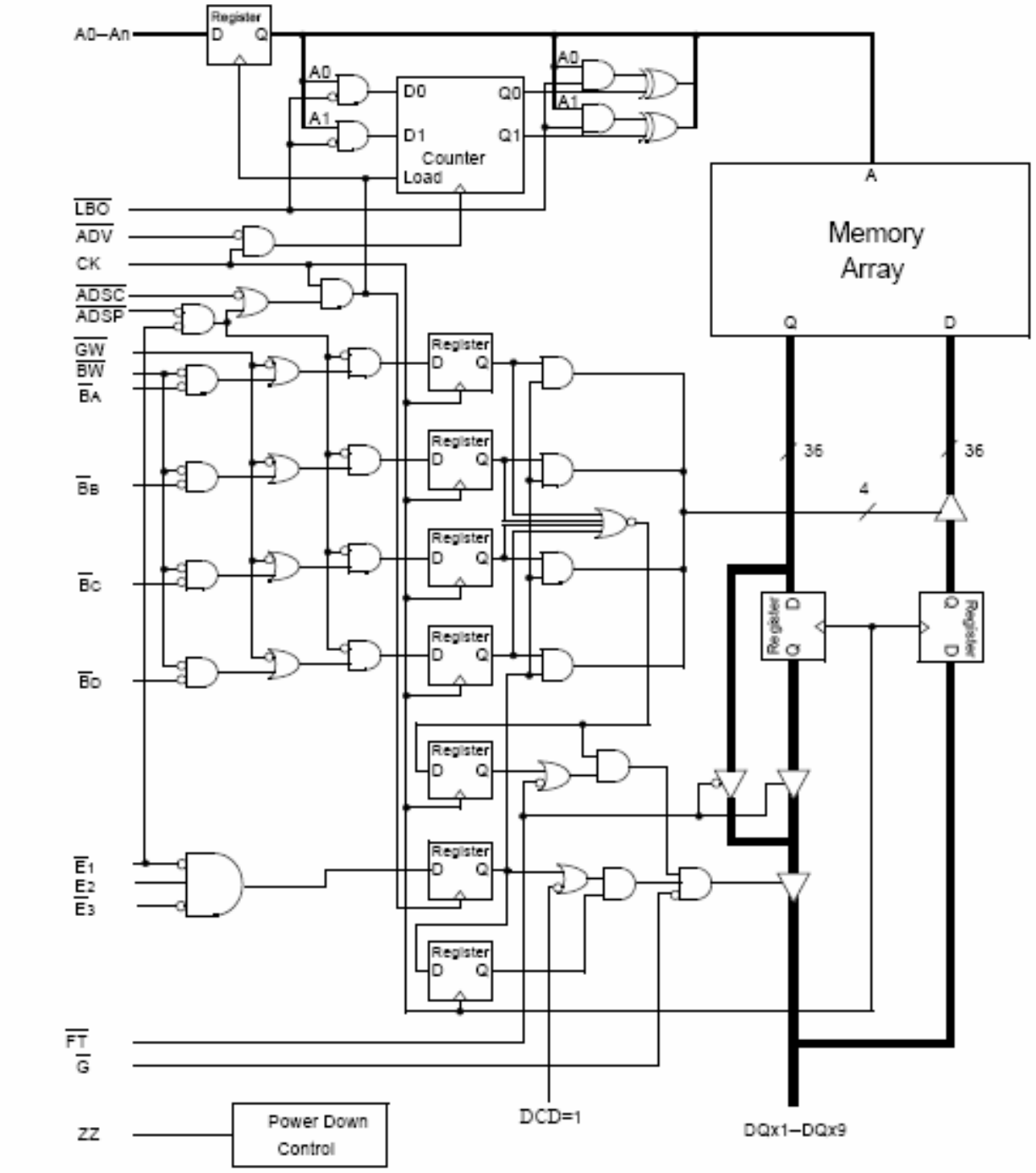
GS88018/32/36A Block Diagram



Note: Only x36 version shown for simplicity.

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Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-down device on the ZZ pin, so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:
The burst counter wraps to initial state on the 5th clock.

Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B_A}$	$\overline{B_B}$	$\overline{B_C}$	$\overline{B_D}$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$ and/or $\overline{B_D}$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "c" and "d" are only available on the x32 and x36 versions.

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Synchronous Truth Table

Operation	Address Used	State Diagram Key[5]	$\overline{E}_1$	E^2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}^3$	DQ[4]
Deselect Cycle, Power Down	**None**	**X**	**H**	**X**	**X**	**L**	**X**	**X**	**High-Z**
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	**None**	**X**	**L**	**F**	**H**	**L**	**X**	**X**	**High-Z**
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	**External**	**R**	**L**	**T**	**H**	**L**	**X**	**F**	**Q**
Write Cycle, Begin Burst	**External**	**W**	**L**	**T**	**H**	**L**	**X**	**T**	**D**
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

Notes:

1. X = Don't Care, H = High, L = Low
2. E = T (True) if E_2 = 1; E = F (False) if E_2 = 0
3. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

2.2 AvBus I/O Connector

The AvBus SRAM Expansion Module is an Avnet Avenue compliant daughter card with a standard memory bus pin out to allow its use with a variety of host boards. The Avnet standard AvBus receptacle connector (P1) is a Tyco (AMP) part number 5-179010-6 which when mated with the plug connector Tyco (AMP) part number 179031-6 provides a 16mm stacking height above the host board. If this stacking height interferes with other boards or connectors in your system the receptacle connector can be replaced with either 5-179009-6 or 177983-6 to provide 12mm or 8mm stacking heights respectively.

The chart below shows the connections between the AvBus connector and the SRAM component. Reference the included schematic for further details.

The JTAG signals (TDI, TDO, TCK, TMS & TRST#) depicted in the following table are not used on the board. They are provided for reference only.

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Name	SRAM PIN #	Connector PIN #			SRAM PIN #	Name
ADDR0	37	71		1	-	+5VDC
GND	-	72		2	36	ADDR1
ADDR3	34	73		3	35	ADDR2
ADDR4	33	74		4	-	GND
GND	-	75		5	32	ADDR5
ADDR7	99	76		6	100	ADDR6
ADDR8	82	77		7	-	GND
+3.3VDC	-	78		8	81	ADDR9
ADDR11	45	79		9	44	ADDR10
ADDR12	46	80		10	-	GND
GND	-	81		11	47	ADDR13
ADDR15	49	82		12	48	ADDR14
ADDR16	50	83		13	-	+5VDC
GND	-	84		14	43	ADDR17
ADDR19	39	85		15	42	ADDR18
ADDR20	38	86		16	-	GND
GND	-	87		17		N/C
N/C		88		18		N/C
N/C		89		19	-	GND
+3.3VDC	-	90		20	83	ADV#
ADSC#	85	91		21	31	LBO#
ADSP#	84	92		22	-	GND
GND	-	93		23	14	FT#
N/C	N/C	94		24	87	BW#
DATA0	52	95		25	-	+5VDC
GND	-	96		26	53	DATA1
DATA3	57	97		27	56	DATA2
DATA4	58	98		28	-	GND
GND	-	99		29	59	DATA5
DATA7	63	100		30	62	DATA6
DATA8	68	101		31	-	GND
+3.3VDC	-	102		32	69	DATA9
DATA11	73	103		33	72	DATA10
DATA12	74	104		34	-	GND
GND	-	105		35	75	DATA13
DATA15	79	106		36	78	DATA14
DATA16	2	107		37	-	+5VDC
GND	-	108		38	3	DATA17
DATA19	7	109		39	6	DATA18
DATA20	8	110		40	-	GND
GND	-	111		41	9	DATA21
DATA23	13	112		42	12	DATA22
DATA24	18	113		43	-	GND
+3.3VDC	-	114		44	19	DATA25
DATA27	23	115		45	22	DATA26
DATA28	24	116		46	-	GND
GND	-	117		47	25	DATA29
DATA31	29	118		48	28	DATA30
N/C		119		49	-	+5VDC
GND	-	120		50	98	SRAM_CS#
R/W#	88	121		51	86	OE#
N/C		122		52	-	GND
GND	-	123		53		N/C
N/C		124		54		N/C
N/C		125		55	-	GND
+3.3VDC	-	126		56		N/C
BE#0	93	127		57		N/C
BE#1	94	128		58	-	GND
GND	-	129		59	95	BE#2
N/C		130		60	96	BE#3
N/C		131		61	-	+5VDC
GND	-	132		62		N/C
N/C		133		63		N/C
N/C		134		64	-	GND
GND	-	135		65	89	SRAM_CLK
N/C		136		66		N/C
TMS	-	137		67	-	GND
+3.3VDC	-	138		68	-	TDO
TDI	-	139		69	-	TCK
TRST#	-	140		70	-	GND

Table 2 - AvBus P1 Pin-out

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