



# 256K x 16 Static RAM

## Features

- **High speed**  
—  $t_{AA} = 15 \text{ ns}$
- **Low active power**  
— 612 mW (max.)
- **Low CMOS standby power (Commercial L version)**  
— 1.8 mW (max.)
- **2.0V Data Retention (600  $\mu\text{W}$  at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**

## Functional Description

The CY7C1041V33 is a high-performance CMOS Static RAM organized as 262,144 words by 16 bits.

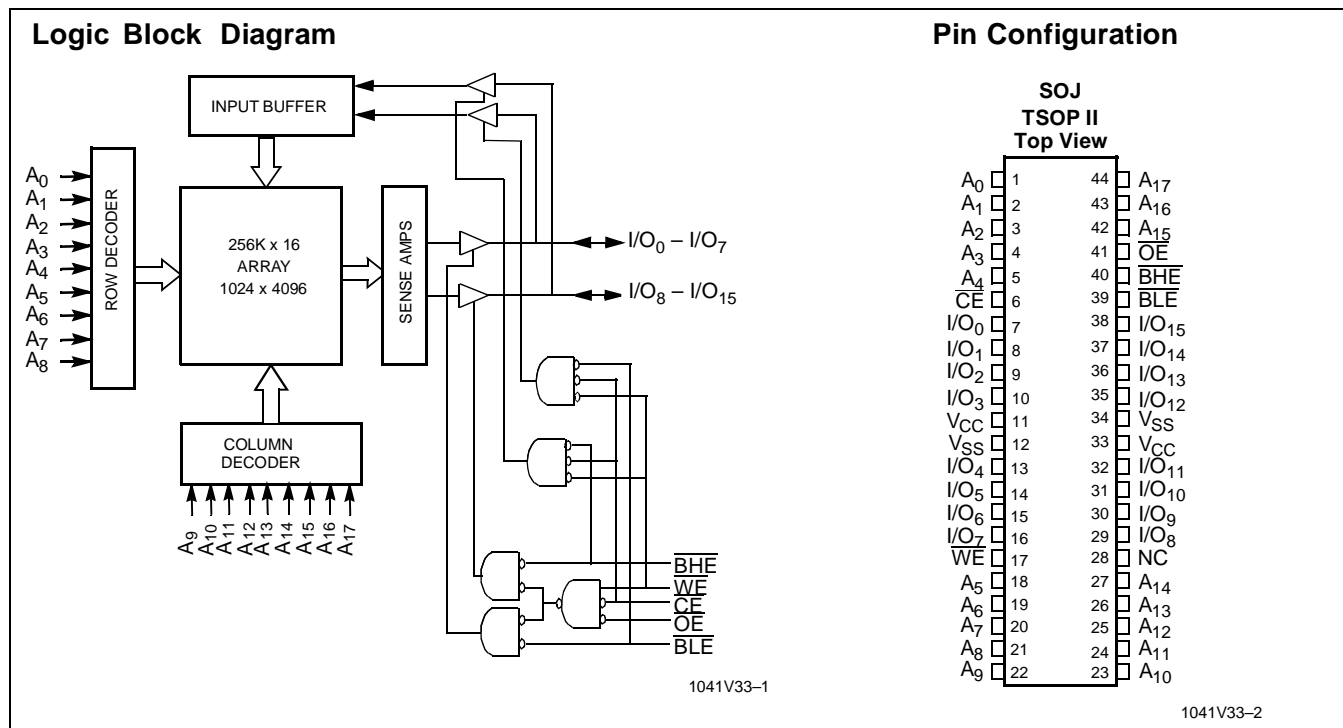
Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ), is

written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), the  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  are disabled ( $\overline{\text{BHE}}, \overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1041V33 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.



## Selection Guide

		1041V33-12	1041V33-15	1041V33-17	1041V33-20	1041V33-25
Maximum Access Time (ns)		12	15	17	20	25
Maximum Operating Current (mA)		190	170	160	150	130
Maximum CMOS Standby Current (mA)	Com'l/Ind'l	8	8	8	8	8
	Com'l L	0.5	0.5	0.5	0.5	0.5

Shaded areas contain preliminary information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C1041-12V33		7C1041V33-15		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$		190		170	mA
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		40		40	mA
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f=0$	Com'I/Ind'I			8	mA
			Com'I	L		0.5	mA

Shaded areas contain preliminary information.

**Notes:**

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.

**Electrical Characteristics** Over the Operating Range (continued)

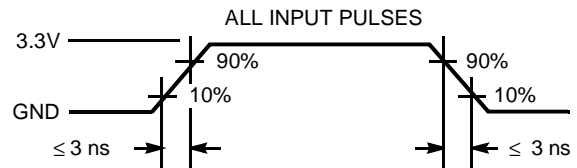
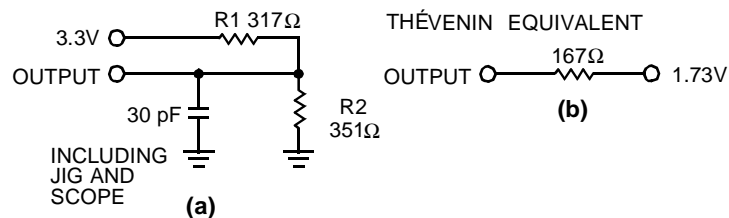
Parameter	Description	Test Conditions	1041V33-17		1041V33-20		1041V33-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	-1	+1	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.},$ $f = f_{\text{MAX}} = 1/t_{RC}$		160		150		130	mA
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{\text{MAX}}$		40		40		40	mA
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ , or $V_{IN} \leq 0.3\text{V}$ , $f=0$	Com'I/Ind'I			8		8	mA
			Com'I	L		0.5		0.5	mA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3\text{V}$	8	pF
$C_{OUT}$	I/O Capacitance		8	pF

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


1041V33-3

1041V33-4

**Switching Characteristics<sup>[4]</sup>** Over the Operating Range

Parameter	Description	1041V33-12		1041V33-15		1041V33-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t <sub>RC</sub>	Read Cycle Time	12		15		17		ns
t <sub>AA</sub>	Address to Data Valid		12		15		17	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15		17	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		6		7		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		6		7		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15		17	ns
t <sub>DBE</sub>	Byte Enable to Data Valid		6		7		7	ns
t <sub>LZBE</sub>	Byte Enable to Low Z	0		0		0		ns
t <sub>HZBE</sub>	Byte Disable to High Z		6		7		8	ns
WRITE CYCLE <sup>[7, 8]</sup>								
t <sub>WC</sub>	Write Cycle Time	12		15		17		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	10		12		12		ns
t <sub>AW</sub>	Address Set-Up to Write End	10		12		12		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	10		12		12		ns
t <sub>SD</sub>	Data Set-Up to Write End	7		8		9		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		6		7		8	ns
t <sub>BW</sub>	Byte Enable to End of Write	10		12		12		ns

Shaded areas contain preliminary information.

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Characteristics<sup>[4]</sup>** Over the Operating Range (continued)

Parameter	Description	1041V33-20		1041V33-25		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t <sub>RC</sub>	Read Cycle Time	20		25		ns
t <sub>AA</sub>	Address to Data Valid		20		25	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		5		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		20		25	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		8		10	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		8		10	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		8		10	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		20		25	ns
t <sub>DBE</sub>	Byte Enable to Data Valid		8		10	ns
t <sub>LZBE</sub>	Byte Enable to Low Z	0		0		ns
t <sub>HZBE</sub>	Byte Disable to High Z		8		10	ns
WRITE CYCLE <sup>[7,8]</sup>						
t <sub>WC</sub>	Write Cycle Time	20		25		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	13		15		ns
t <sub>AW</sub>	Address Set-Up to Write End	13		15		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	13		15		ns
t <sub>SD</sub>	Data Set-Up to Write End	9		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		8		10	ns
t <sub>BW</sub>	Byte Enable to End of Write	13		15		ns

**Data Retention Characteristics** Over the Operating Range (For L version only)

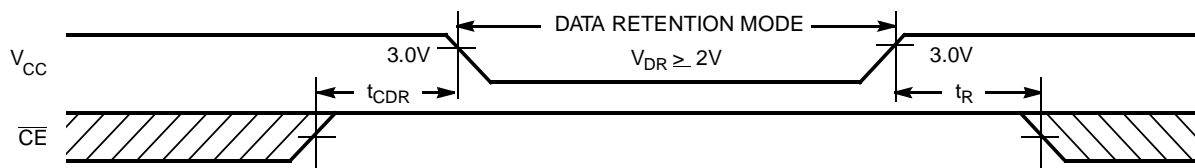
Parameter	Description	Conditions <sup>[10]</sup>	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		330	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[9]}$	Operation Recovery Time		$t_{RC}$		ns

**Notes:**

9.  $t_r \leq 3$  ns for the -12 and -15 speeds.  $t_r \leq 5$  ns for the -20 and slower speeds.

10. No input may exceed  $V_{CC} + 0.5V$ .

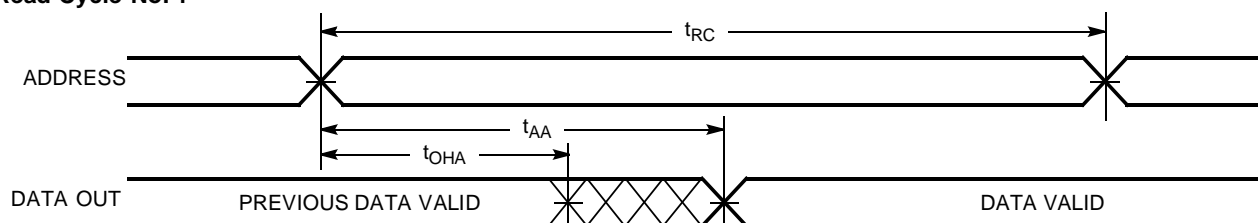
## Data Retention Waveform



1041V33-5

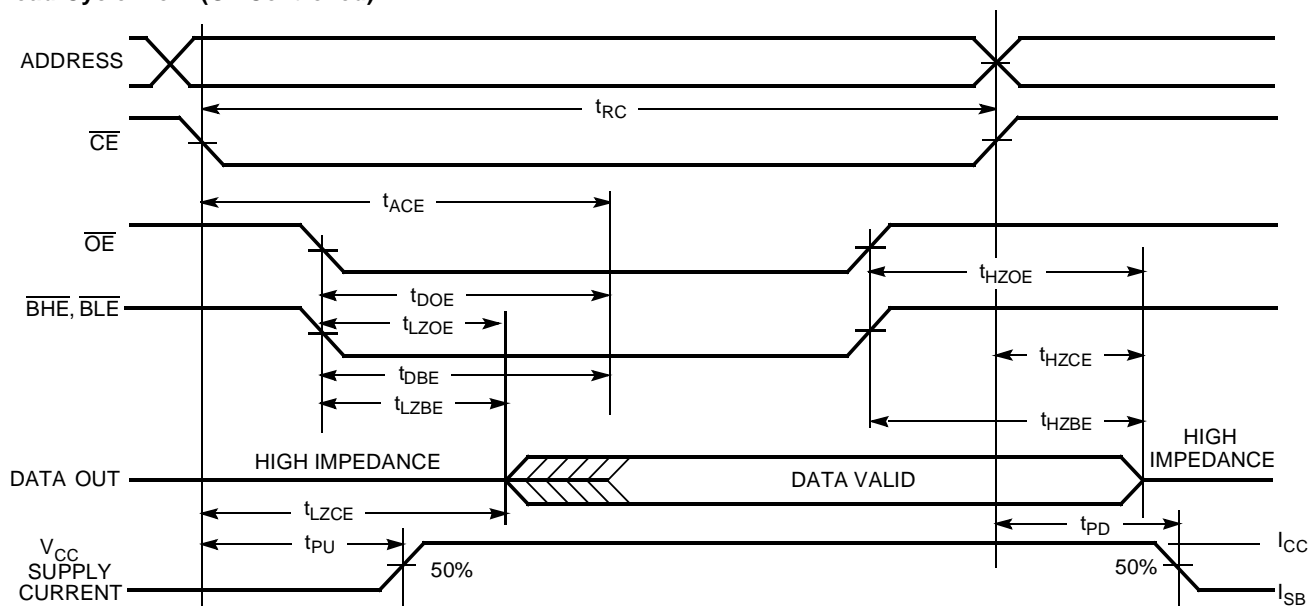
## Switching Waveforms

### Read Cycle No. 1<sup>[11, 12]</sup>



1041V33-6

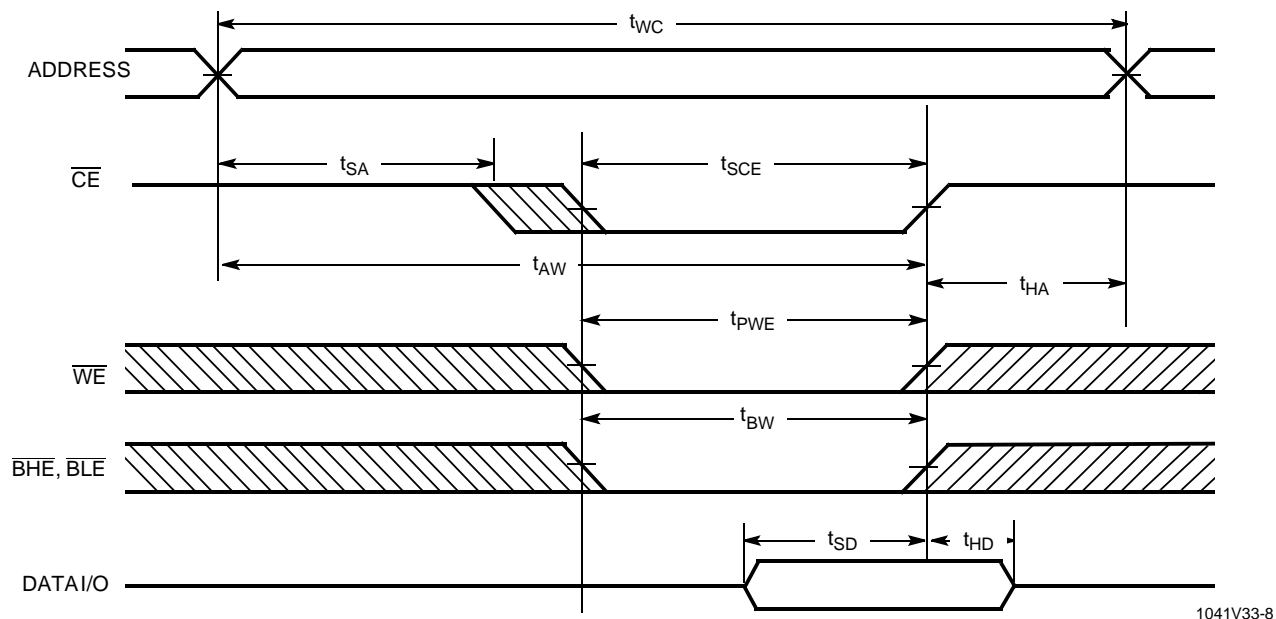
### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[12, 13]</sup>



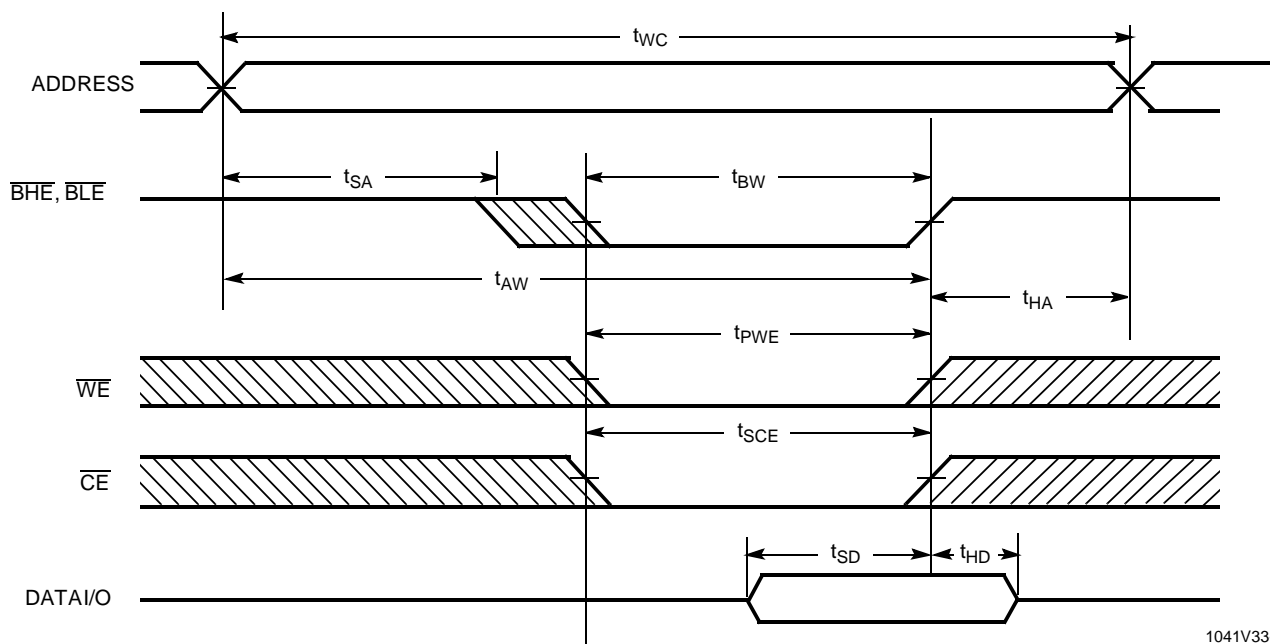
1041V33-7

#### Notes:

11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[14, 15]</sup>**


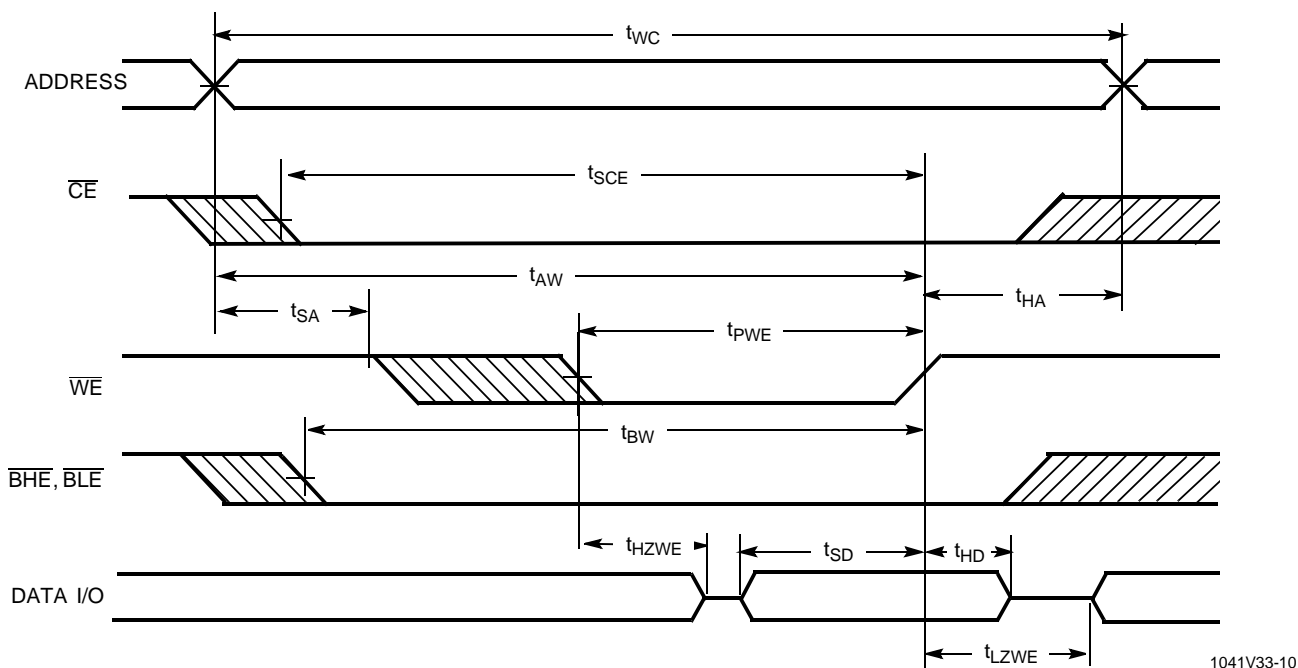
1041V33-8

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**


1041V33-9

**Notes:**

14. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No.3 ( $\overline{\text{WE}}$  Controlled, LOW)**

**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby ( $I_{\text{SB}}$ )
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active ( $I_{\text{CC}}$ )
L	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active ( $I_{\text{CC}}$ )
L	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active ( $I_{\text{CC}}$ )
L	X	L	L	L	Data In	Data In	Write All Bits	Active ( $I_{\text{CC}}$ )
L	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active ( $I_{\text{CC}}$ )
L	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active ( $I_{\text{CC}}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{\text{CC}}$ )



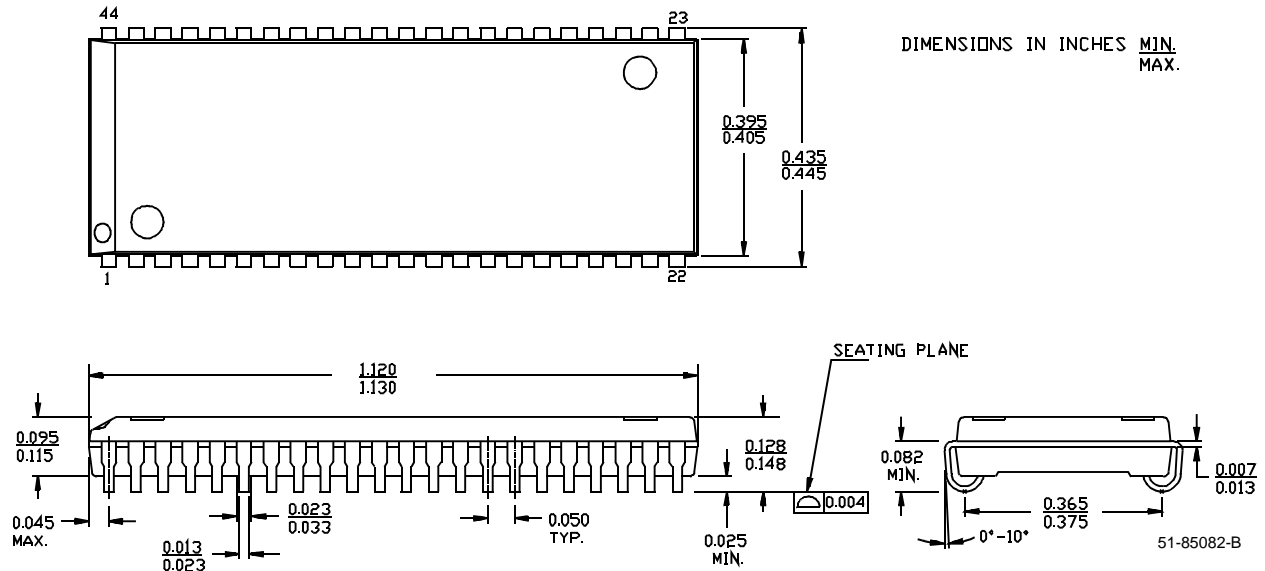
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1041V33 -12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1041V33L-12VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33 - 12ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041V33L-12ZC	Z44	44-Pin TSOP II Z44	
15	CY7C1041V33 -15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33L-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33 - 15ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041V33L-15ZC	Z44	44-Pin TSOP II Z44	
17	CY7C1041V33 - 17VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33L-17VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33 - 17ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041V33L-17ZC	Z44	44-Pin TSOP II Z44	
20	CY7C1041V33 - 20VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33L-20VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33 - 20ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041V33L-20ZC	Z44	44-Pin TSOP II Z44	
25	CY7C1041V33 - 25VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33L-25VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041V33 - 25ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041V33L-25ZC	Z44	44-Pin TSOP II Z44	

Document #: 38-00645-B

## Package Diagrams

### 44-Lead (400-Mil) Molded SOJ V34



### 44-Pin TSOP II Z44

DIMENSION IN MM (INCH)  
MAX  
MIN.

