SDRAM Expansion Module
User Guide

AVNET electronics marketing

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1.0 Introduction

The purpose of this manual is to provide the information required to implement a functional design using the AvBus SDRAM Expansion Module from Avnet Design Services. This document includes a description of the hardware and a pin-out for the AvBus connector.

1.1 Description

The AvBus SDRAM Expansion Module provides additional data storage for compatible host boards. This document will talk only about the AvBus SDRAM Expansion Module itself and not the host boards because it is compatible with any AvBus host connector that has the required interface signals available.

1.2 Features

Board I/O Connectors

— 140-pin general-purpose I/O expansion connectors (AvBus)

Memory

— SDRAM – 64MByte

- Micron MT48LC16M16 SDRAM

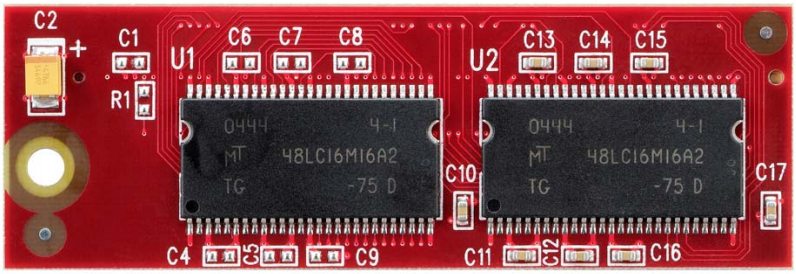

Figure 1 - AvBus SDRAM Expansion Module Picture

1.3 Ordering Information

The following table lists the evaluation kit part numbers and available software options. Internet link at http://www.em.avnet.com/ads

Part Number	Hardware
ADS-SDRAM-DAU	AvBus SDRAM Expansion Module

Table 1 - Ordering Information

2.0 User Information

This section provides the user with information on how to get started using the AvBus SDRAM Expansion Module with a compatible host board. There are no movable jumpers on this board.

2.1 Memory

The AvBus SDRAM Expansion Module is populated with two 256Mb SDRAM memory devices configured as 16Mx32bit. The Expansion Module supports the 54-pin TSOP-II package with a single +3.3V power supply. The memory device has LVTTL-compatible inputs and outputs. The timing parameters associated with the devices installed on the board are shown in Table 2.

MT48LC16M16A2TG-75:D: Timing Parameters	Time (ps) or Number
Load Mode Register time (TMRD)	2
Write Recovery time (TWR)	17500
R/W Command to R/W Command time (TCCD)	1
Delay between ACT and PRE Commands (TRAS)	44000
Delay after ACT before another ACT (TRC)	66000
Delay after AUTOREFRESH Command (TRFC)	66000
Delay after ACT before READ/WRITE (TRCD)	20000
Delay after ACT before another row ACT (TRRD)	15000
Delay after PRECHARGE Command (TRP)	20000
Refresh Period (TREF)	64
Refresh Number Rows (NUMROWS)	8192
CAS Latency @ 100 MHz/133 MHz	2/3
Memory Data Width (DWIDTH) (x2 devices)	32
Row Address Width (AWIDTH)	13
Column Address Width (COL_AWIDTH)	9
Bank Address Width (BANK_AWIDTH)	2
Memory Range (64 MB total)	0x3FFFFFF

Table 2 - SDRAM Timing Parameters

2.2 AvBus I/O Connector

The AvBus SDRAM Expansion Module is an Avalon compliant daughter card with a standard memory bus pin out to allow its use with a variety of host boards. The Avnet standard AvBus receptacle connector (P1) is a Tyco (AMP) part number 5-179010-6 which when mated with the plug connector Tyco (AMP) part number 179031-6 provides a 16mm stacking height above the host board. If this stacking height interferes with other boards or connectors in your system the receptacle connector can be replaced with either 5-179009-6 or 177983-6 to provide 12mm or 8mm stacking heights respectively.

Table 2 on the following page shows the connections between the AvBus connector and the SDRAM components. The AvBus address signals ADDR[2:14] are connected to the SDRAM address A[0:12]. AvBus address ADDR[15:16] are connected to the SDRAM bank address pins BA[0:1]. The chip select signal enables both devices (shared chip select). The clock enable pin is tied to VCC on the board. Please note that the AvBus data bus signals are bit swapped with respect to the SDRAM data pin names. Reference the included schematic for further details.

Figure 2 provides additional information for the specific case where the host board is running an embedded processor in a Xilinx FPGA and interfacing to the SDRAM Module using the “OPB SDRAM Controller” peripheral included in the Xilinx Embedded Development Kit (EDK) software. Note: The pin LOCs in your UCF file for most of the SDRAM ports are intuitive except for the address and bank address pins, which are bit-swapped and connect like this:

Address: “SDRAM_Addr<0>”=ADDR14, “SDRAM_Addr<1>”=ADDR13, …, “SDRAM_Addr<12>”=ADDR2
Bank Address: “SDRAM_BankAddr<0>=ADDR16 & “SDRAM_BankAddr<1>=ADDR15

```
# Using the EDK OPB_SDRAM peripheral v1_00_e:

- Core parameters:
  - C_USE_POSEDGE_OUTREGS    = 1
  - C_INCLUDE_HIGHSPEED_PIPE = 0
  - C_INCLUDE_BURST_SUPPORT  = 1

- Core ports:
  - CLKEN not used (tied to VCC on board)
  - SDRAM_Clk not used (generate clk to memory with DDR flop)*
  - SDRAM_Clk_IN = CLK0 out of DCM (sys_clk_s)
  - OPB_Clk      = CLK0 out of DCM (sys_clk_s)

- OPB_SDRAM Peripheral notes:
  - SDRAM_Clk (out) <= SDRAM_Clk_IN (clk_gen.vhd), will have different clk-to-out delay than
    all other SDRAM sigs, which is why the DDR flop is used to align the clock
    to the memory with the data/addr/cntl
  - SDRAM_Clk_IN & OPB_Clk should be CLK0 out of a DCM (BUFGed)
  - Setting either POSEDGE_OUTREGS or HIGHSPEED_PIPE to 1 adds 1-clk to CAS latency:
    read data is latched one clk later than CAS_LAT parameter

*
  - If: clk_period - clk to out (SDRAM DQ ) < required SDRAM setup time (tds) :
    - Invert the clock: Port D0 = net_gnd, Port D1 = net_vcc
  - Else:
    - Port D0 = net_vcc, Port D1 = net_gnd
```

Figure 2 - Design Notes for OPB_SDRAM

The JTAG signals (TDI, TDO, TCK, TMS & TRST#) depicted in the following table are not used on the board. They are provided for reference only.

Name	SDRAM PIN #	Connector PIN #			SDRAM PIN #	Name
ADDR0	N/C	71		1	-	+5VDC
GND	-	72		2	N/C	ADDR1
ADDR3	U1/2-24	73		3	U1/2-23	ADDR2
ADDR4	U1/2-25	74		4	-	GND
GND	-	75		5	U1/2-26	ADDR5
ADDR7	U1/2-30	76		6	U1/2-29	ADDR6
ADDR8	U1/2-31	77		7	-	GND
+3.3VDC	-	78		8	U1/2-32	ADDR9
ADDR11	U1/2-34	79		9	U1/2-33	ADDR10
ADDR12	U1/2-22	80		10	-	GND
GND	-	81		11	U1/2-35	ADDR13
ADDR15	U1/2-20	82		12	U1/2-36	ADDR14
ADDR16	U1/2-21	83		13	-	+5VDC
GND	-	84		14	N/C	ADDR17
ADDR19	N/C	85		15	N/C	ADDR18
ADDR20	N/C	86		16	-	GND
GND	-	87		17	N/C	ADDR21
ADDR23	N/C	88		18	N/C	ADDR22
ADDR24	N/C	89		19	-	GND
+3.3VDC	-	90		20	N/C	ADDR25
ADDR27	N/C	91		21	N/C	ADDR26
ADDR28	N/C	92		22	-	GND
GND	-	93		23	N/C	ADDR29
ADDR31	N/C	94		24	N/C	ADDR30
DATA0	U2-53	95		25	-	+5VDC
GND	-	96		26	U2-51	DATA1
DATA3	U2-48	97		27	U2-50	DATA2
DATA4	U2-47	98		28	-	GND
GND	-	99		29	U2-45	DATA5
DATA7	U2-42	100		30	U2-44	DATA6
DATA8	U2-13	101		31	-	GND
+3.3VDC	-	102		32	U2-11	DATA9
DATA11	U2-8	103		33	U2-10	DATA10
DATA12	U2-7	104		34	-	GND
GND	-	105		35	U2-5	DATA13
DATA15	U2-2	106		36	U2-4	DATA14
DATA16	U1-53	107		37	-	+5VDC
GND	-	108		38	U1-51	DATA17
DATA19	U1-48	109		39	U1-50	DATA18
DATA20	U1-47	110		40	-	GND
GND	-	111		41	U1-45	DATA21
DATA23	U1-42	112		42	U1-44	DATA22
DATA24	U1-13	113		43	-	GND
+3.3VDC	-	114		44	U1-11	DATA25
DATA27	U1-8	115		45	U1-10	DATA26
DATA28	U1-7	116		46	-	GND
GND	-	117		47	U1-5	DATA29
DATA31	U1-2	118		48	U1-4	DATA30
N/C		119		49	-	+5VDC
GND	-	120		50		N/C
R/W#	U1/2-16	121		51		N/C
N/C		122		52	-	GND
GND	-	123		53		N/C
N/C		124		54		N/C #
N/C		125		55	-	GND
+3.3VDC	-	126		56	U1/2-19	SDRAM_CS#
BE#0	U2-39	127		57		N/C
BE#1	U2-15	128		58	-	GND
GND	-	129		59	U1-39	BE#2
N/C		130		60	U1-15	BE#3
N/C		131		61	-	+5VDC
GND	-	132		62	U1/2-17	CAS#
N/C		133		63	U1/2-18	RAS#
N/C		134		64	-	GND
GND	-	135		65	U1/2-38	SDRAM_CLK
N/C		136		66		N/C
TMS	-	137		67	-	GND
+3.3VDC	-	138		68	-	TDO
TDI	-	139		69	-	TCK

Table 3 - AvBus P1 Pin-out