Master Clock

File: clock.kicad_sch

Main CPU

File: CPUA.kicad_sch

Audio CPU

File: aucpu.kicad_sch

CPU Wait States

File: cpu_wait.kicad_sch

Horizontal Pixel Counters

File: pixels.kicad_sch

Vertical Pixel Counters

File: vpixels.kicad_sch

Foreground Layer

File: foreground.kicad_sch

Background Layer

File: background.kicad_sch

Sprite RAM

File: SpriteRAM.kicad_sch

Sprite ROM

File: SpriteROM.kicad_sch

Sprite Addressing

File: spradd.kicad_sch

Sprite Line Buffer

File: spLinebuff.kicad_sch

Video Output

File: video_out.kicad_sch

Connectors

File: Connectors.kicad_sch

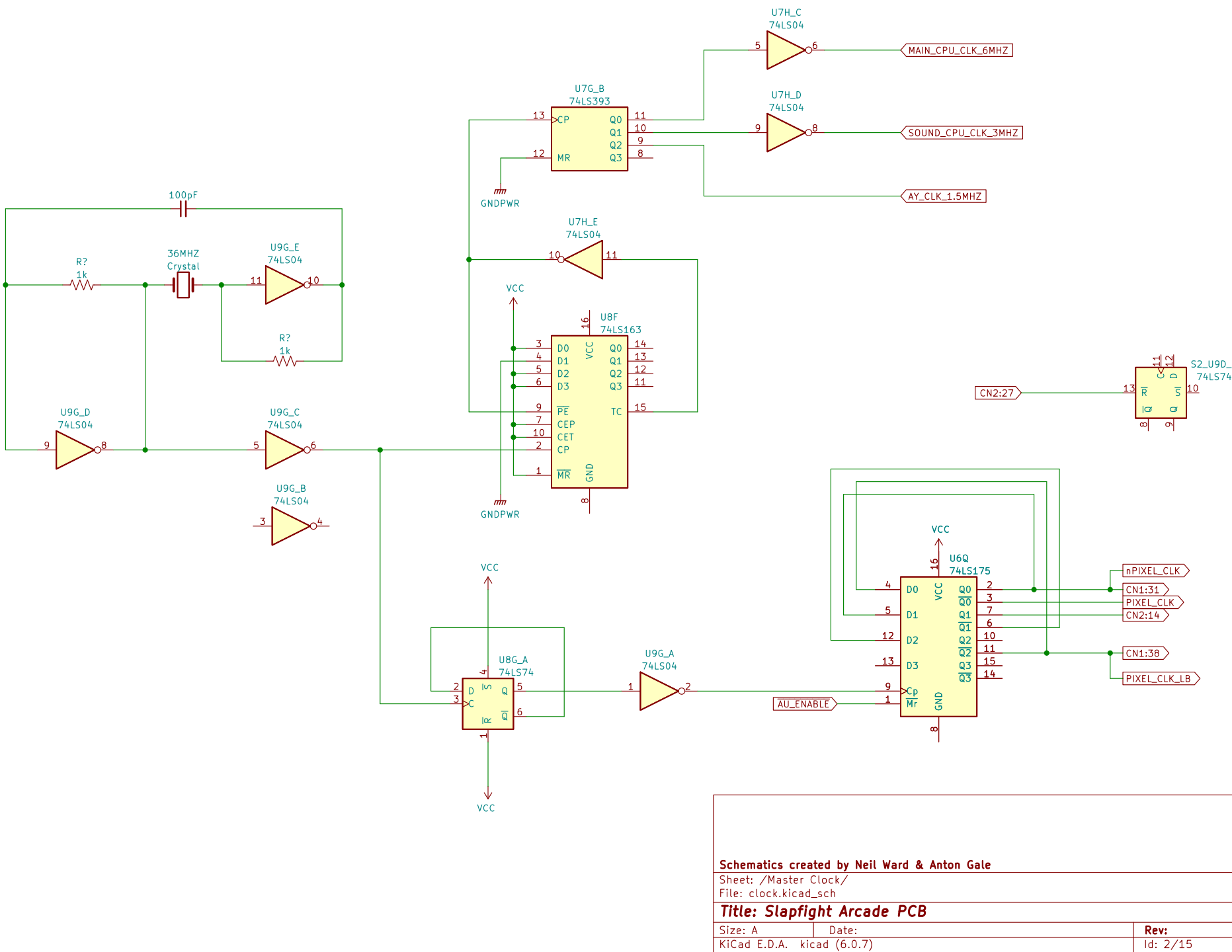
Schematics created by Neil Ward & Anton Gale

Sheet: /

File: SlapFight.kicad_sch

Title: Slapfight Arcade PCB

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.7)		Id: 1/15



Schematics created by Neil Ward & Anton Gale

Sheet: /Master Clock/

File: clock.kicad_sch

Title: Slapfight Arcade PCB

Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.7)		Id: 2/15

C4
47uF

U9N_C
74LS14

U9N_B
74LS14

RESET

MAIN_CPU_CLK_6MHZ

Z80M_INT

Z80M_WAIT

Z80M_MAIN_RD

Z80M_MAIN_WR

Z80M_MREQ

Z80M_IOREQ

U8Q
Z80M (MAIN CPU)

Z80M_A[0..15]

Z80M_D[0..7]

U9P_B
74LS139
decoder

Z80M_MREQ

Z80M_A15

SYSTEM RAM
0xC000 – 0xC7FF

U8M
RAM_2016
A[10] RAM 2kB

Z80M_MAIN_RD

Z80M_MAIN_WR

U9K
74LS138
address decoder

Z80M_A11

Z80M_A12

Z80M_A13

0xC000–0xC7FF

0xC800–0xCFFF

0xD000–0xD7FF

0xD800–0xDFFF

0xE000–0xE7FF

0xE800–0xEFFF

0xF000–0xF7FF

0xF800–0xFFFF

AUDIO_CPU_PORT

BACKGRAM_1

BACKGRAM_2

SPRITE_RAM

MCU_PORT

CHARAM

ATRRAM

U8N
27C256 – A77–01–1

ROM_BANK_SH

MAIN PROGRAM ROM: A77–01–1
0x8000 – 0xBFFF

U8P
27C256 – A77–00–1

U9A_A
74LS08

MAIN PROGRAM ROM: A77–00–1
0x0000 – 0x7F00

Z80 IO PORT A

U9J
74LS259

Z80M_IOREQ

Z80M_MAIN_WR

RESET

0x00 – 0x01

0x02 – 0x03

0x04 – 0x05

0x06 – 0x07

0x08 – 0x09

0x0C – 0x0D

0x0E – 0x0F

CN2:27

AU_ENABLE

IO_2_SCREEN_FLIP

IO_4_CPU_RAM

INT_ENABLE

ROM_BANK_SH

IO_C_SPRITE_COLOUR

68705_RESET

U9L
74LS367

LINE_CLK2

68705_RD_BUFFER_FULL

68705_WR_BUFFER_FULL

U9L_B
74LS32

U9L_A
74LS32

U9M_D
74LS32

U9P_A
74LS139
decoder

MCU_PORT

0xE800_H_SCRL_LO

0xE801_H_SCRL_HI

0xE802_V_SCRL

MCU_PORT_WR

Schematics created by Neil Ward & Anton Gale

Sheet: /Main CPU/

File: CPUA.kicad_sch

Title: Slapfight Arcade PCB

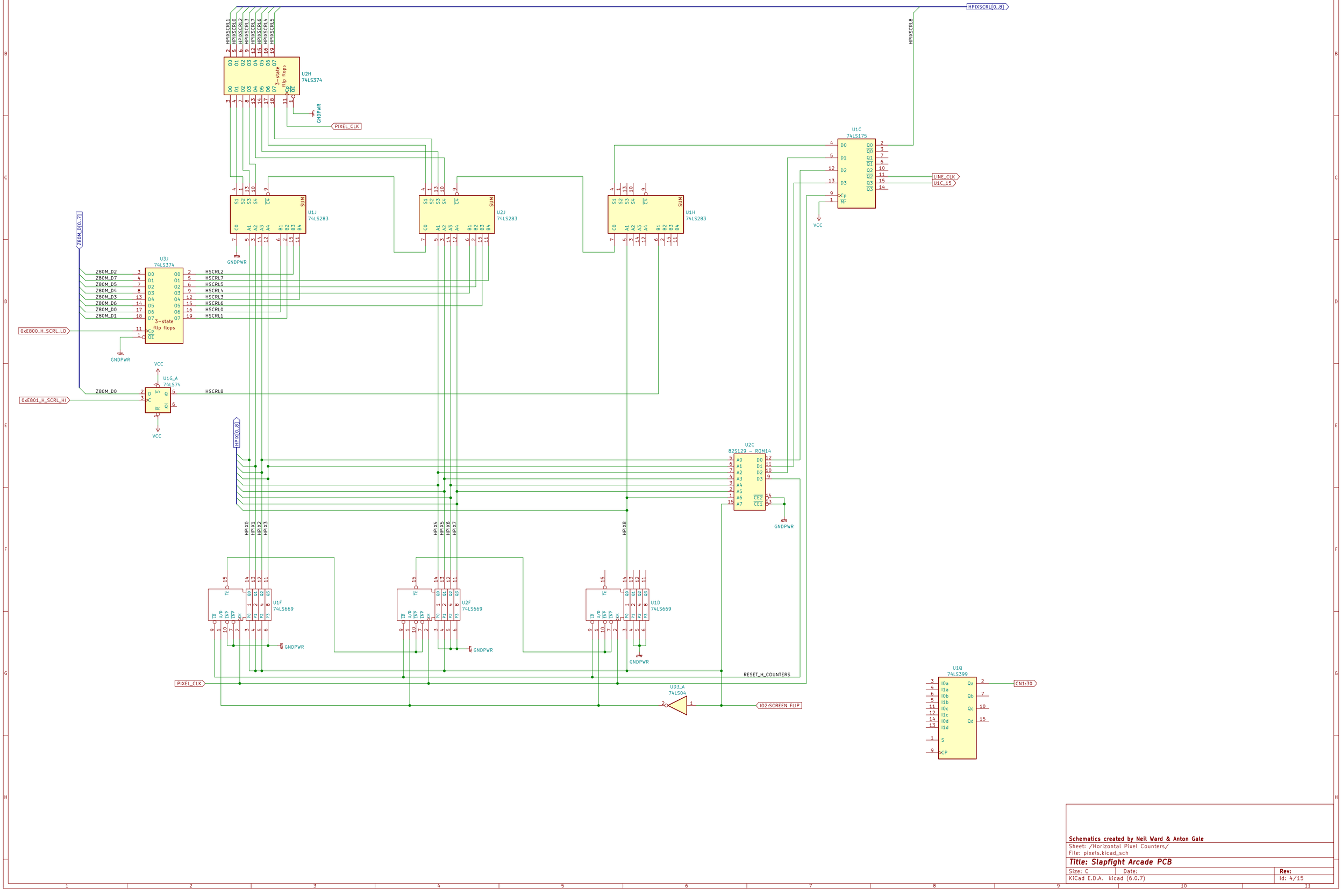
Size: B

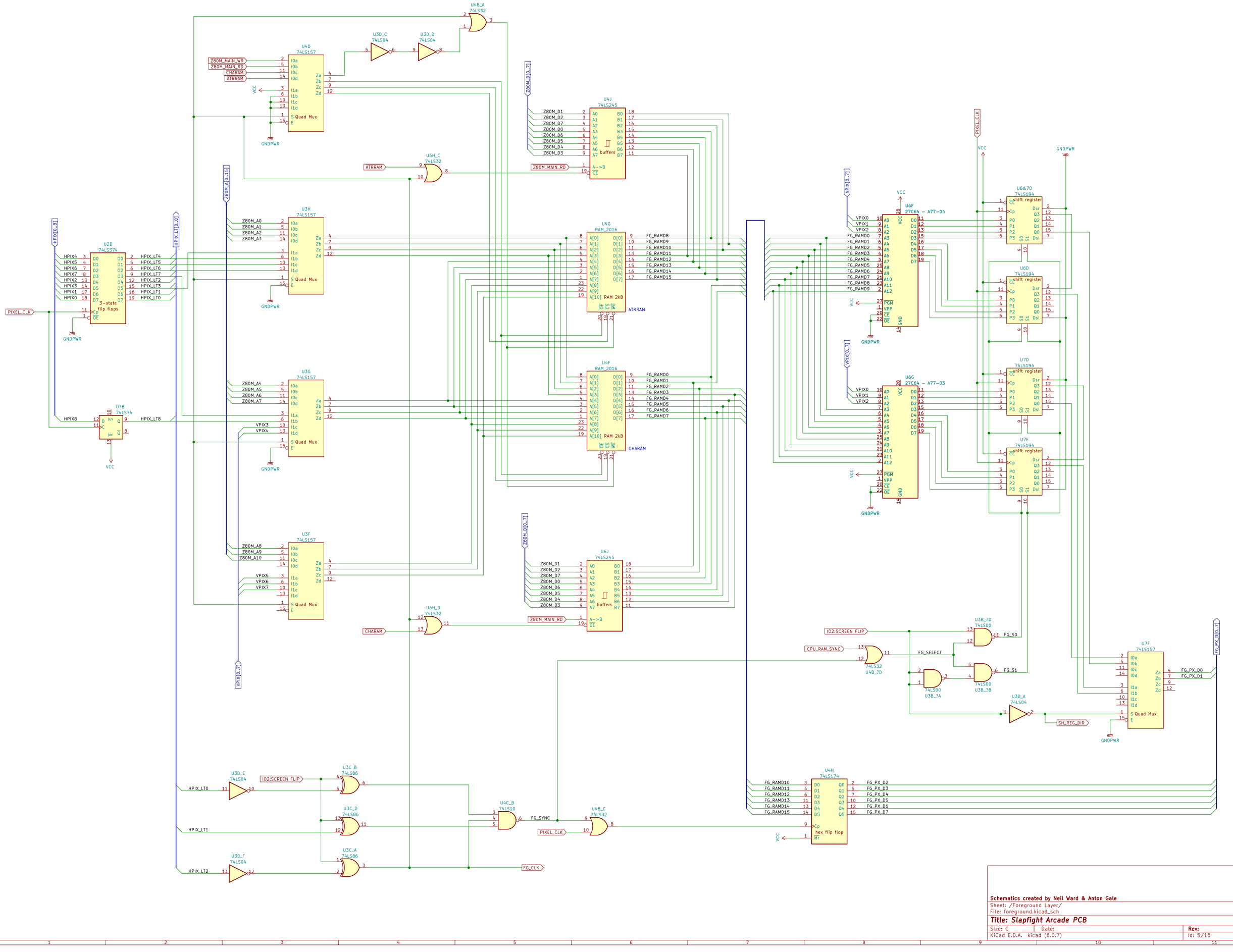
Date:

Rev:

KiCad E.D.A. kicad (6.0.7)

Id: 3/15


HPIXSCRL[0..8]
HPIXSCRL8
HPIXSCRL1
HPIXSCRL0
HPIXSCRL2
HPIXSCRL3
HPIXSCRL7
HPIXSCRL6
HPIXSCRL4
HPIXSCRL5
U2H
74LS374
3-state
flip flops
GNDPWR
PIXEL_CLK
U1C
74LS175
VCC
LINE_CLK
U1C_15
U1J
74LS283
U2J
74LS283
U1H
74LS283
SUM
GNDPWR
Z80M_D[0..7]
U3J
74LS374
Z80M_D2
Z80M_D7
Z80M_D5
Z80M_D4
Z80M_D3
Z80M_D6
Z80M_D0
Z80M_D1
HSCRL2
HSCRL7
HSCRL5
HSCRL4
HSCRL3
HSCRL6
HSCRL0
HSCRL1
0xE800_H_SCRL_LO
GNDPWR
VCC
U1G_A
74LS74
Z80M_D0
HSCRL8
0xE801_H_SCRL_HI
VCC
HPIX[0..8]
U2C
82S129 - ROM14
GNDPWR
HPIX0
HPIX1
HPIX2
HPIX3
HPIX4
HPIX5
HPIX6
HPIX7
HPIX8
U1F
74LS669
U2F
74LS669
U1D
74LS669
GNDPWR
RESET_H_COUNTERS
PIXEL_CLK
UD3_A
74LS04
!02:SCREEN FLIP
U1Q
74LS399
CN1:30
Schematics created by Neil Ward & Anton Gale
Sheet: /Horizontal Pixel Counters/
File: pixels.kicad_sch
Title: Slapfight Arcade PCB
Size: C
Date:
Rev:
KiCad E.D.A. kicad (6.0.7)
Id: 4/15



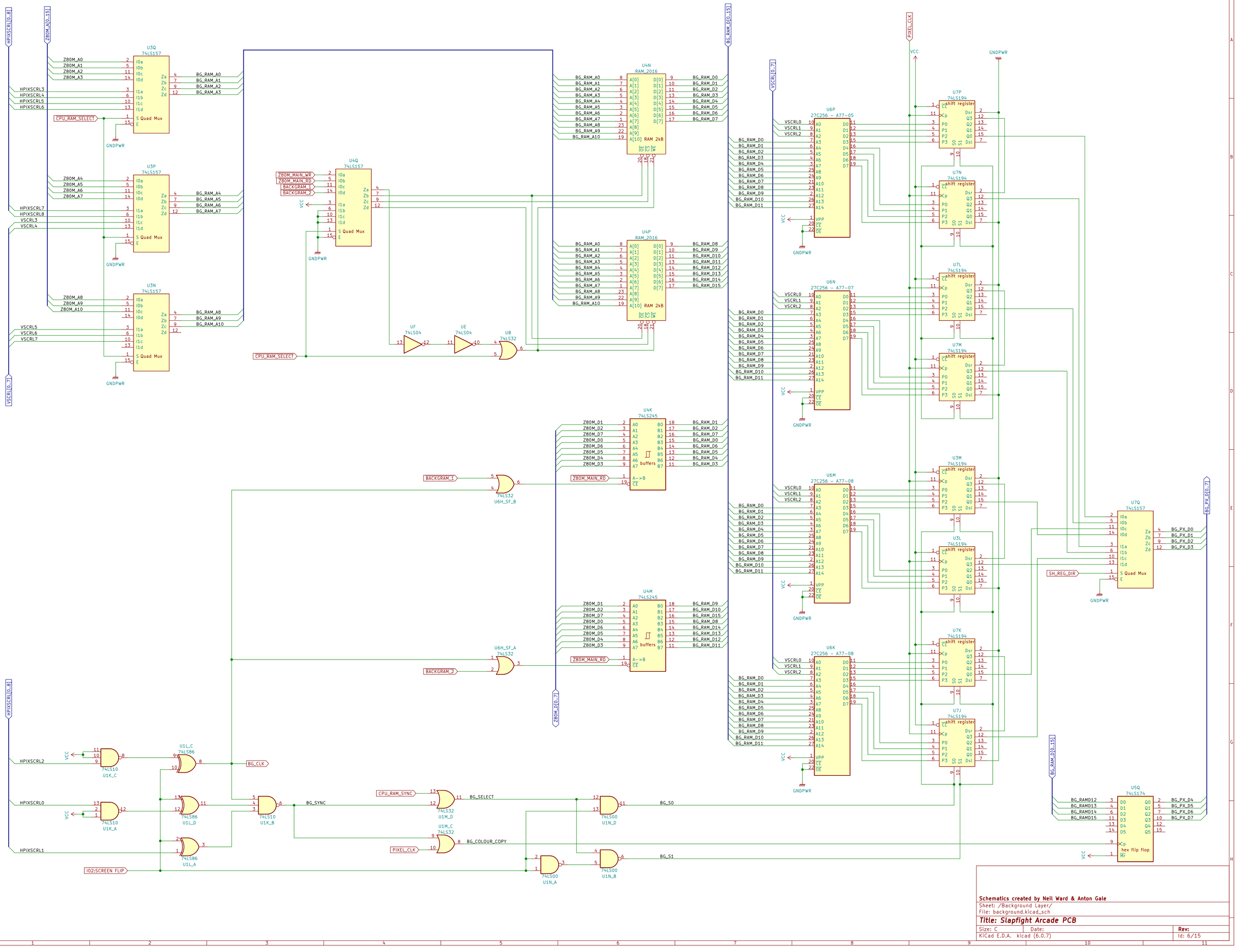
Schematics created by Neil Ward & Anton Gale

Sheet: /Foreground Layer/

File: foreground.kicad_sch

Title: Slapfight Arcade PCB

Size: C	Date:	Rev:
KiCad E.D.A. kicad (6.0.7)		Id: 5/15



Schematics created by Neil Ward & Anton Gale
Sheet: /Background Layer/
File: background.kicad_sch

Title: Slapfight Arcade PCB

Size: C	Date:	Rev:
KiCad E.D.A. kicad (6.0.7)		Id: 6/15

U?
74LS175
U?
74LS273
flip flops
SP_PX
FG_PX
PIXEL_CLK
2_U11T_B
74LS32
2_U11T_A
74LS32
U2_U11T_D
74LS32
2_U11R_D
74LS32
2_U10R_A
74LS74
2_U10R_B
74LS74
2_U11R_A
74LS32
2_U11R_B
74LS32
VCC
BG_PX_D[0..7]
FG_PX_D[0..7]
2_U11M
74LS374 – BACKGROUND
2_U11P
74LS374 – FOREGROUND
2_U12S
74LS374 – SPRITES
3-state
flip flops
2_U12Q
82S129 – ROM21
2_U12P
82S129 – ROM19
2_U12N
82S129 – ROM20
R46
2.2k
R47
1k
R48
470
R49
220
R50
470
JAMMA:12:RED
R41
2.2k
R42
1k
R43
470
R44
220
R45
470
JAMMA:13:BLUE
R36
2.2k
R37
1k
R38
470
R39
220
R40
470
JAMMA:N:GREEN
2_U8FB
74LS08
CN1:36
CN1:37
R9
47
JAMMA:P:SYNC
U8R
74LS373
CN1:38

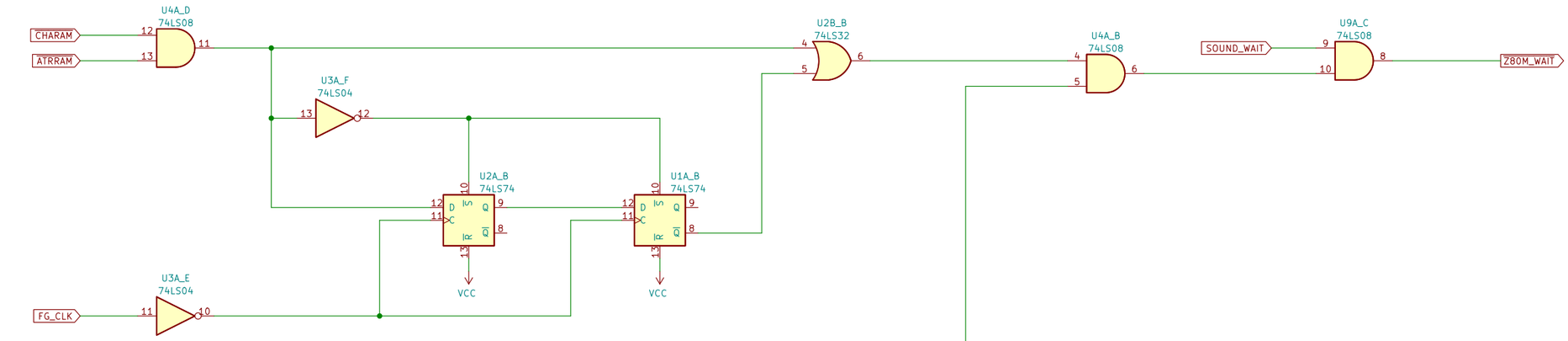
Schematics created by Neil Ward & Anton Gale

Sheet: /Video Output/
File: video_out.kicad_sch

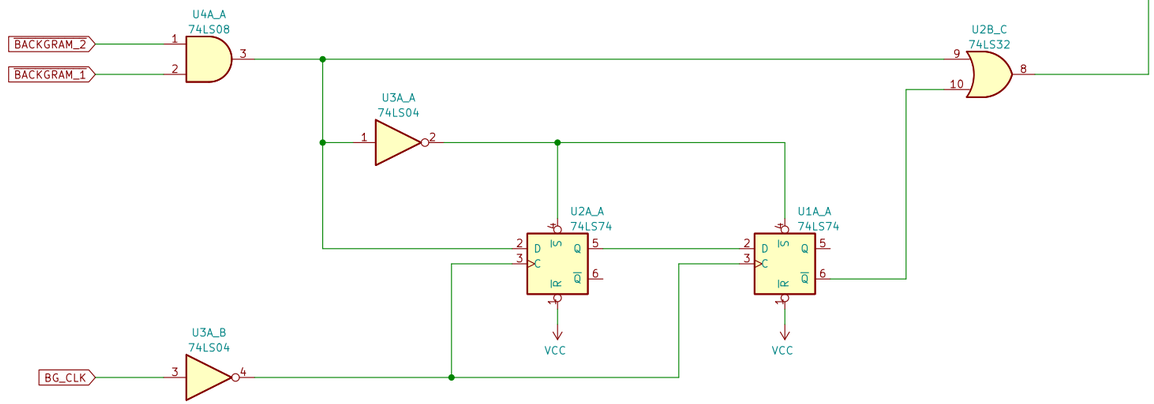
Title: Slapfight Arcade PCB

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.7)		Id: 7/15

FOREGROUND LAYER RAM ACCESS WAIT STATES



BACKGROUND LAYER RAM ACCESS WAIT STATES



Schematics created by Neil Ward & Anton Gale

Sheet: /CPU Wait States/

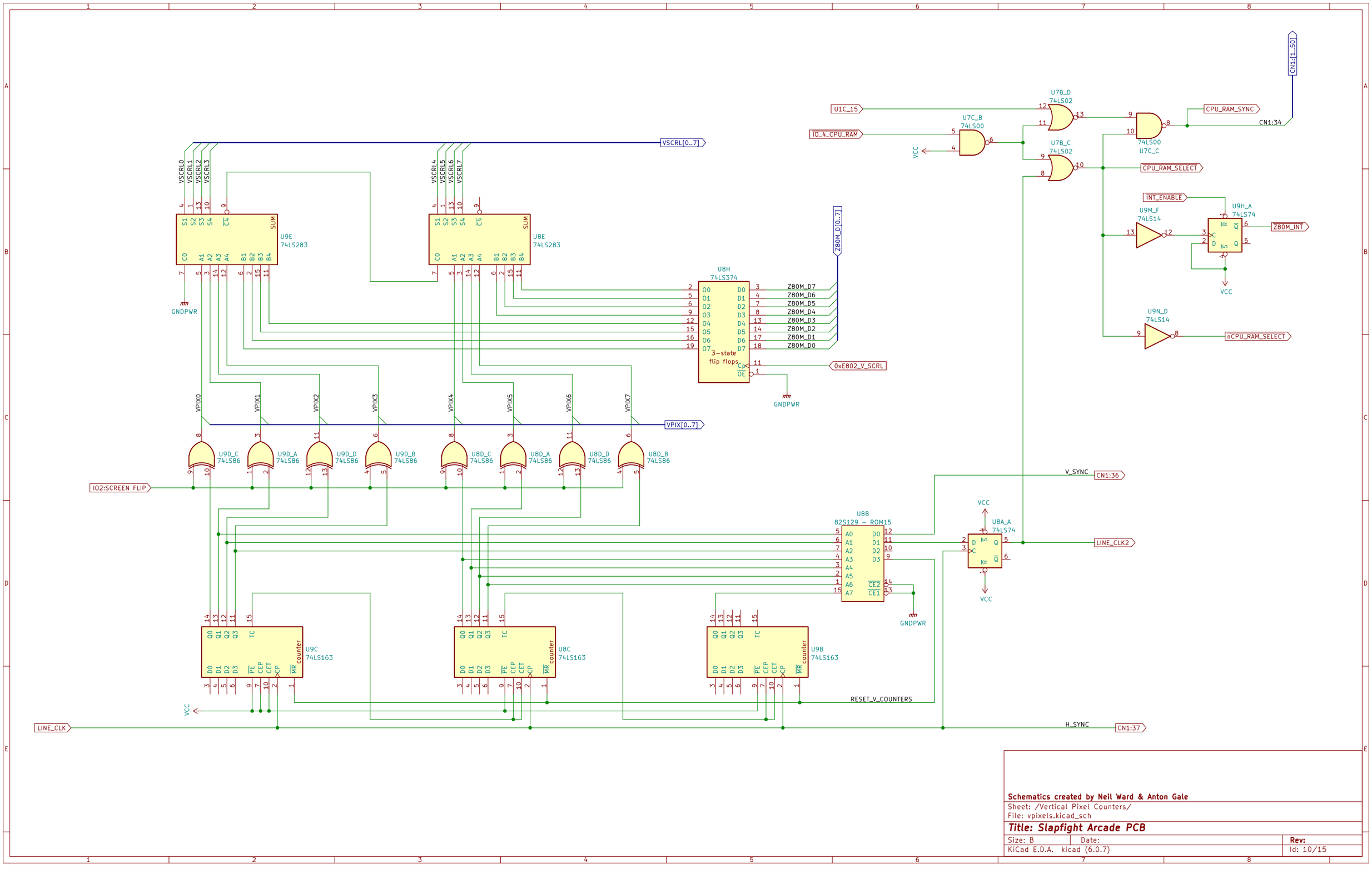
File: cpu_wait.kicad_sch

Title: Slapfight Arcade PCB

Size: B	Date:	Rev:
KiCad E.D.A. kicad (6.0.7)		Id: 8/15

S2_U9A_A
74LS74
VCC
MAIN_CPU_CLK_6MHZ
AUDIO_CPU_PORT
AUDIO_CPU_BUSACK
S2_U9B_A
74LS32
S2_U9B_B
74LS32
S2_U9B_C
74LS32
AUDIO_CPU_PORT
CN2:29
SOUND_WAIT
Z80M_MAIN_RD
Z80M_MREQ
Z80M_MAIN_WR
S2_U9C
74LS367
AURD
AUIMREQ
AUWR
Z80M_A[0..15]
AUA[0..15]
S2_U13A
74LS244
Z80M_A7
Z80M_A5
Z80M_A3
Z80M_A1
Z80M_A0
Z80M_A2
Z80M_A4
Z80M_A6
AUA7
AUA5
AUA3
AUA1
AUA0
AUA2
AUA4
AUA6
S2_U12A
74LS244
Z80M_A12
Z80M_A13
Z80M_A14
Z80M_A15
Z80M_A8
Z80M_A9
Z80M_A10
Z80M_A11
AUA12
AUA13
AUA14
AUA15
AUA8
AUA9
AUA10
AUA11
S2_U11F
74LS245
Z80M_D0
Z80M_D1
Z80M_D2
Z80M_D3
Z80M_D4
Z80M_D5
Z80M_D6
Z80M_D7
AUD0
AUD1
AUD2
AUD3
AUD4
AUD5
AUD6
AUD7
buffers
Z80M_D[0..7]
Z80M_MAIN_RD
AUD[0..7]
S2_U12B
Z80AU (AUDIO CPU)
AU_ENABLE
SOUND_CPU_CLK_3MHZ
AUDIO_CPU_NMI
AURD
AUWR
AUIMREQ
AUIORQ
AUDIO_CPU_PORT
AUDIO_CPU_BUSACK
S2_U12D
27C64
AU_ROM_CS
AURD
AUDIO RAM
0xC000 → 0xDFFF
S2_U11B
RAM_2kB
S2_U11D
74LS138
address decoder
AUA13
AUA14
AUA15
0x0000-0x1FFF
AU_ROM_CS
0xC000-0xDFFF
GNDPWR
S2_U11E
74LS138
AUA4
AUA5
AUA6
AUA7
0xA000-0xBFFF
AUIMREQ
S2_U9D_B
74LS74
S2_U7A
4020
SOUND_CPU_CLK_3MHZ
AU_ENABLE
S2_U9E_D
74LS02
AUDIO_CPU_NMI
S2_U11F
74LS245
AUD0
AUD1
AUD2
AUD3
AUD4
AUD5
AUD6
AUD7
AY_D0
AY_D1
AY_D2
AY_D3
AY_D4
AY_D5
AY_D6
AY_D7
buffers
AURD
S2_U9F_A
74LS02
S2_U9F_B
74LS02
S2_U9F_C
74LS02
AUA1
AUA2
AUA0
AY_1_SEL
AY_1_BC1
AY_1_BC2
AY_1_BDIR
S2_U11G
AY-3-8910 (AY_1)
LIVES1
LIVES0
DIFFICULTY1
DIFFICULTY0
UNUSED SW2:4
UNUSED SW2:3
UNUSED SW2:2
UNUSED SW2:1
COINAGE2
COINAGE1
COINAGE0
DEMO SOUNDS
CABINET
FLIP SCREEN
SERVICE
UNUSED SW1:1
DIP SWITCH READ
AU_CLK_1.5MHZ
RA3
3.3k
SW2
SW_DIP_x08
SW1
SW_DIP_x08
RA5
3.3k
GNDPWR
S2_U9E_A
74LS02
S2_U9E_B
74LS02
S2_U9E_C
74LS02
AY_2_SEL
AY_2_BC1
AY_2_BC2
AY_2_BDIR
S2_U11J
AY-3-8910 (AY_2)
P1_BUTTON2
P1_BUTTON1
P2_BUTTON2
P2_BUTTON1
P1_START
P2_START
P1_COIN
P2_COIN
P1_UP
P1_DOWN
P1_RIGHT
P1_LEFT
P2_UP
P2_DOWN
P2_RIGHT
P2_LEFT
CONTROLS READ
RA4
3.3k
RA6
3.3k
S2_JAMMA:23
S2_JAMMA:22
S2_JAMMA:a
S2_JAMMA:Z
S2_JAMMA:17
S2_JAMMA:U
S2_JAMMA:16
S2_JAMMA:T
S2_JAMMA:18
S2_JAMMA:19
S2_JAMMA:21
S2_JAMMA:20
S2_JAMMA:V
S2_JAMMA:W
S2_JAMMA:Y
S2_JAMMA:X

Schematics created by Neil Ward & Anton Gale
Sheet: /Audio CPU/
File: aucpu.kicad_sch
Title: Slapfight Arcade PCB
Size: C
Date:
Rev:
KiCad E.D.A. kicad (6.0.7)
Id: 9/15



Schematics created by Neil Ward & Anton Gale

Sheet: /Vertical Pixel Counters/

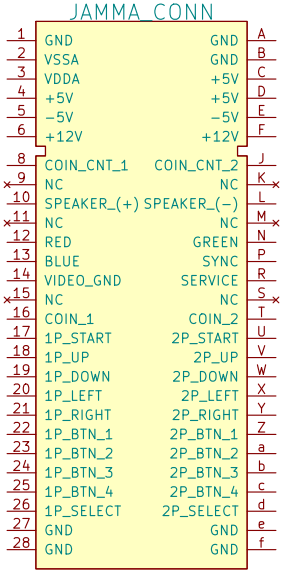
File: vpixels.kicad_sch

Title: Slapfight Arcade PCB

Size: B	Date:	Rev:
KiCad E.D.A. kicad (6.0.7)		Id: 10/15

S2_JAMMA

JAMMA_CONN



Schematics created by Neil Ward & Anton Gale

Sheet: /Connectors/
File: Connectors.kicad_sch

Title: Slapfight Arcade PCB

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.7)		Id: 11/15

U3K
74LS245
Z80M_D[0..7]
Z80M_D1
Z80M_D2
Z80M_D7
Z80M_D0
Z80M_D6
Z80M_D5
Z80M_D4
Z80M_D3
A0
A1
A2
A3
A4
A5
A6
A7
buffers
A->B
CE
B0
B1
B2
B3
B4
B5
B6
B7
SPRITE_RAM_D1
SPRITE_RAM_D2
SPRITE_RAM_D7
SPRITE_RAM_D0
SPRITE_RAM_D6
SPRITE_RAM_D5
SPRITE_RAM_D4
SPRITE_RAM_D3
SPRITE_RAM_D[0..7]
U2K_C
74LS32
Z80M_MREQ
SPRITE_RAM
Z80M_MAIN_RD
SPRITE RAM
0xE000-0xE7FF
U2L
RAM_2016
SPR_A[0..15]
SPR_A0
SPR_A1
SPR_A2
SPR_A3
SPR_A4
SPR_A5
SPR_A6
SPR_A7
SPR_A8
SPR_A9
SPR_A10
A[0]
A[1]
A[2]
A[3]
A[4]
A[5]
A[6]
A[7]
A[8]
A[9]
A[10] RAM 2kB
OE
CS
WE
D[0]
D[1]
D[2]
D[3]
D[4]
D[5]
D[6]
D[7]
SPRITE_RAM_D0
SPRITE_RAM_D1
SPRITE_RAM_D2
SPRITE_RAM_D3
SPRITE_RAM_D4
SPRITE_RAM_D5
SPRITE_RAM_D6
SPRITE_RAM_D7
SPR_RD
Z80M_MAIN_WR
SPRITE_RAM
SPR_CNT[0..11]
Z80M_A[0..15]
SPR_A[0..11]
S2_U2Q
74LS157
S2_U2P
74LS157
S2_U2N
74LS157
Z80M_A0
Z80M_A1
Z80M_A2
Z80M_A3
Z80M_A4
Z80M_A5
Z80M_A6
Z80M_A7
Z80M_A8
Z80M_A9
Z80M_A10
Z80M_MAIN_RD
SPR_CNT0
SPR_CNT1
SPR_CNT2
SPR_CNT3
SPR_CNT4
SPR_CNT5
SPR_CNT6
SPR_CNT7
SPR_CNT8
SPR_CNT9
SPR_CNT10
I0a
I0b
I0c
I0d
I1a
I1b
I1c
I1d
S Quad Mux
E
Za
Zb
Zc
Zd
U1N_C
74LS00
VCC
CPU_RAM_SELECT
GNDPWR
S2_U1B_A
74LS393
S2_U1B_B
74LS393
U6Q:2
CN1:31
CP
MR
Q0
Q1
Q2
Q3
S2_U4C_D
74LS32
RST_REG_CTR
SPR_CPU_RAM_SELECT
S2_1C
82S129 - ROM17
S2_1E
82S129 - ROM16
A0
A1
A2
A3
A4
A5
A6
A7
D0
D1
D2
D3
CE2
CE1
S2_U1F
74LS174
PIXEL_CLK
hex flip flop
Cp
Mr
D0
D1
D2
D3
D4
D5
Q0
Q1
Q2
Q3
Q4
Q5
S2_U1A_B
74LS04
TP?
TestPoint
S2_U1G
74LS138
address
decoder
E3
E2
E1
O0
O1
O2
O3
O4
O5
O6
O7
SPR_LAT_HPOS
SPR_LAT_XDAT
SPR_LAT_VPOS
SPR_LAT_INDX
S2_U1G_10
S2_U1G_9
S2_U1G_7
S2_U1A_A
74LS04
nCPU_RAM_SELECT
S2_U4B
74LS161
S2_U2C
74LS161
PE
CEP
CET
TC
counter
nCPU_RAM_SYNC
S2_U2B
N82S123N - ROM18
S2_U2A
74LS175
SPR_REG_OE
SPR_RAM_OE
SPR_LB_LD
SPR_8HPIX
2_U11R_C
74LS32
SPR_ROM_LD
CPU_RAM_SYNC
S2_U4A
74LS175
2_4A_3
2_4A_6
2_4A_10
2_4A_11
S2_U5B_A
74LS04
U1Q_A
74LS393
U1Q_B
74LS393
U1P_B
74LS393
SPR_CNT[0..11]
Schematics created by Neil Ward & Anton Gale
Sheet: /Sprite RAM/
File: SpriteRAM.kicad_sch
Title: Slapfight Arcade PCB
Size: B
Date:
Rev:
KiCad E.D.A. kicad (6.0.7)
Id: 12/15

S2_U7H
27C256 - A77-09
S2_U7G
74LS166
S2_U7K
74LS166
S2_U7J
27C256 - A77-11
S2_U8H
27C256 - A77-10
S2_U9G
74LS166
S2_U9K
74LS166
S2_U9K
27C256 - A77-12
S2_U3H
HM6264
S2_U3J
HM6264
S2_U3K
HM6264
S2_U3L
HM6264
SPR_8HPIX
SPR_VPIX0
SPR_VPIX1
SPR_VPIX2
SPR_VPIX3
SPR_IDX_D0
SPR_IDX_D1
SPR_IDX_D2
SPR_IDX_D3
SPR_IDX_D4
SPR_IDX_D5
SPR_IDX_D6
SPR_IDX_D7
SPR_IDX_D8
SPR_IDX_D9
SPR_ROM_LD
PIXEL_CLK
SPR_PIX_A
SPR_PIX_B
SPR_PIX_C
SPR_PIX_D
SPR_32K_A[0..14]
SPR_VPIX[0..3]
SPR_IDX_D[0..9]
SPR_COL_D[0..3]
SPR_HPOS_D[0..7]
SPR32_WR
SPR_RAM_OE
SPR_HPOS_D8
SPR_COL_D0
SPR_COL_D1
SPR_COL_D2
SPR_COL_D3
SPR_EXTRA_D5
SPR_HPOS_D0
SPR_HPOS_D1
SPR_HPOS_D2
SPR_HPOS_D3
SPR_HPOS_D4
SPR_HPOS_D5
SPR_HPOS_D6
SPR_HPOS_D7
VCC
GNDPWR

Schematics created by Neil Ward & Anton Gale

Sheet: /Sprite ROM/
File: SpriteROM.kicad_sch

Title: Slapfight Arcade PCB

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.7)		Id: 13/15

S2_U1G_10
S2_U7B_A
74LS74
GNDPWR
S2_U1G_9
S2_U5B_D
74LS04
SPR32_CLK
S2_U9B_D
74LS32
S2_U7B_B
74LS74
VCC
S2_U7C
74LS161
GNDPWR
SPR32_CLK
VCC
counter
S2_U5C
74LS367
SPR_VPIX[0..3]
SPR_VPIX0
SPR_VPIX1
SPR_VPIX2
SPR_VPIX3
SPR_REG_OE
S2_U1H
74LS374
SPRITE_RAM_D1
SPRITE_RAM_D3
SPRITE_RAM_D5
SPRITE_RAM_D7
SPRITE_RAM_D6
SPRITE_RAM_D4
SPRITE_RAM_D2
SPRITE_RAM_D0
SPR_VPOS_D1
SPR_VPOS_D3
SPR_VPOS_D5
SPR_VPOS_D7
SPR_VPOS_D6
SPR_VPOS_D4
SPR_VPOS_D2
SPR_VPOS_D0
3-state
flip flops
SPR_LAT_VPOS
SPR_REG_OE
SPRITE MONITOR
V POSITION
SPR_VPOS_D[0..7]
SPR_IDX_D[0..9]
S2_U1J
74LS374
SPR_IDX_D1
SPR_IDX_D3
SPR_IDX_D5
SPR_IDX_D7
SPR_IDX_D6
SPR_IDX_D4
SPR_IDX_D2
SPR_IDX_D0
SPR_LAT_INDX
SPR_REG_OE
SPRITE BITMAP
INDEX
SPR_COL_D[0..3]
S2_U1K
74LS374
SPR_COL_D0
SPR_COL_D2
SPR_IDX_D9
SPR_IDX_D8
SPR_COL_D3
SPR_COL_D1
SPR_HPOS_D8
SPR_LAT_XDAT
SPR_REG_OE
SPRITE EXTRA
DATA
S2_U1L
74LS374
SPR_HPOS_D1
SPR_HPOS_D3
SPR_HPOS_D5
SPR_HPOS_D7
SPR_HPOS_D6
SPR_HPOS_D4
SPR_HPOS_D2
SPR_HPOS_D0
SPR_LAT_HPOS
SPR_REG_OE
SPRITE MONITOR
H POSITION
SPRITE_RAM_D[0..7]
SPR_HPOS_D[0..7]
SPR_VPOS_D[0..7]
S2_U5F
74LS161
SPR_VPOS_D0
SPR_VPOS_D1
SPR_VPOS_D2
SPR_VPOS_D3
SPR32_CLK
counter
VPIX[0..7]
S2_U5E
74LS157
VPIX0
VPIX1
VPIX2
VPIX3
S Quad Mux
SPR_32K_A0
SPR_32K_A1
SPR_32K_A2
SPR_32K_A3
SPR_32K_A[0..11]
SPRITE RAM ADDRESS GENERATION
S2_U7F
74LS161
SPR_VPOS_D4
SPR_VPOS_D5
SPR_VPOS_D6
SPR_VPOS_D7
SPR32_CLK
counter
nCPU_RAM_SYNC
S2_U7E
74LS157
VPIX4
VPIX5
VPIX6
VPIX7
S Quad Mux
SPR_32K_A4
SPR_32K_A5
SPR_32K_A6
SPR_32K_A7
GNDPWR
SPR_32K_A[0..11]
S2_U4F
74LS283
SPR_32K_A8
SPR_32K_A9
SPR_32K_A10
SPR_32K_A11
SUM
S2_U2E
74LS367
S2_U4E
74LS174
SPR_32K_A8
SPR_32K_A9
SPR_32K_A10
SPR_32K_A11
hex flip flop
S2_U4C_B
74LS32
S2_U1G_9
2_4A_3
S2_U5A_A
74LS08
S2_U2F
HM6148
SPR_32K_A0
SPR_32K_A1
SPR_32K_A2
SPR_32K_A3
SPR_32K_A4
SPR_32K_A5
SPR_32K_A6
SPR_32K_A7
SPR32_BUF_WR
S2_U4C_C
74LS32
S2_U1G_7
2_4A_6
S2_U5A_B
74LS08
SPR32_BUF_WR
S2_U8F_A
74LS08
SPR32_WR
S2_U4C_A
74LS32
S2_U1G_10
S2_U8F_D
74LS08
SPR32_CLK

Schematics created by Neil Ward & Anton Gale

Sheet: /Sprite Addressing/
File: spradd.kicad_sch

Title: Slapfight Arcade PCB

Size: B	Date:	Rev:
KiCad E.D.A. kicad (6.0.7)		Id: 14/15

S2_U1A_F 74LS04
S2_U1A_E 74LS04
SPR_LB_LD
S2_U5A_D 74LS08
2_4A_11
S2_U1M 74LS669
PIXEL_CLK
SPR_HPOS_D0
SPR_HPOS_D1
SPR_HPOS_D2
SPR_HPOS_D3
LNBF_CNT0
LNBF_CNT1
LNBF_CNT2
LNBF_CNT3
S2_U2M 74LS669
SPR_HPOS_D4
SPR_HPOS_D5
SPR_HPOS_D6
SPR_HPOS_D7
LNBF_CNT4
LNBF_CNT5
LNBF_CNT6
LNBF_CNT7
S2_U3M 74LS669
SPR_HPOS_D8
LNBF_CNT8
GNDPWR
SPR_HPOS_D[0..8]
LNBF_CNT[0..8]
SPR_LINEA
S2_U1T_A 74LS08
LNBF_CNT8
HPIX_LT8
S2_U8F_C 74LS08
SPR_LINEB
S2_U1P_A 74LS32
S2_U2T 74LS157
HPIX_LT0
HPIX_LT1
HPIX_LT2
HPIX_LT3
S Quad Mux
U1C_15
S2_U4T 74LS157
HPIX_LT4
HPIX_LT5
HPIX_LT6
HPIX_LT7
HPIX_LT[0..8]
S2_U5T HM6148
LINEBUF_A_A0
LINEBUF_A_A1
LINEBUF_A_A2
LINEBUF_A_A3
LINEBUF_A_A4
LINEBUF_A_A5
LINEBUF_A_A6
LINEBUF_A_A7
LINEBUF_A_D0
LINEBUF_A_D1
LINEBUF_A_D2
LINEBUF_A_D3
S2_U5R HM6148
LINEBUF_A_D4
LINEBUF_A_D5
LINEBUF_A_D6
LINEBUF_A_D7
SP_PX_SEL[0..3]
S2_U7P 74LS244
SP_PX_SEL_D0
SP_PX_SEL_D2
SP_PX_SEL_D3
SP_PX_SEL_D1
S2_U5L 74LS174
SPR_COL_D[0..3]
SP_COL_D0
SP_COL_D1
SP_COL_D2
SP_COL_D3
SP_PX_SEL_D0
SP_PX_SEL_D1
SP_PX_SEL_D2
SP_PX_SEL_D3
SP_PX_SEL[0..3]
SPR_EXTRA_D5
SPR_ROM_LD
VCC
hex flip flop
S2_U7R 74LS373
LE
OE
S2_U10T 74LS273
SP_PX
SP_PX_D1
SP_PX_D3
SP_PX_D5
SP_PX_D6
SP_PX_D7
SP_PX_D4
SP_PX_D2
SP_PX_D0
flip flops
S2_U7L_D 74LS08
SPR_PIX_A
S2_U7L_C 74LS08
SPR_PIX_B
S2_U7M_B 74LS02
S2_U7L_B 74LS08
SPR_PIX_D
S2_U7L_A 74LS08
SPR_PIX_C
S2_U7M_A 74LS02
S2_U8M_A 74LS00
S2_U1R_A 74LS10
S2_U4A_10
S2_U1T_D 74LS08
S2_U1P_D 74LS32
S2_U2R 74LS157
S2_U4R 74LS157
S2_U5M HM6148
S2_U5P HM6148
LINEBUF_B_A0
LINEBUF_B_A1
LINEBUF_B_A2
LINEBUF_B_A3
LINEBUF_B_A4
LINEBUF_B_A5
LINEBUF_B_A6
LINEBUF_B_A7
LINEBUF_B_D0
LINEBUF_B_D1
LINEBUF_B_D2
LINEBUF_B_D3
LINEBUF_B_D4
LINEBUF_B_D5
LINEBUF_B_D6
LINEBUF_B_D7
S2_U8R 74LS373
S2_U8L_D 74LS08
S2_U8L_C 74LS08
S2_U8L_B 74LS08
S2_U8L_A 74LS08
S2_U8P 74LS244
PIXEL_CLK_LB
S2_U7M_C 74LS02
S2_U7M_D 74LS02
S2_U8M_C 74LS00
S2_U1R_B 74LS10
S2_U1T_C 74LS08
S2_U1P_C 74LS32
S2_U8C 74HC164
nCPU_RAM_SYNC
S2_U9D_A 74LS74

Schematics created by Neil Ward & Anton Gale
Sheet: /Sprite Line Buffer/
File: spLinebuff.kicad_sch
Title: Slapfight Arcade PCB
Size: C
Date:
Rev:
KiCad E.D.A. kicad (6.0.7)
Id: 15/15