100V, 1A High Efficiency Synchronous Buck Converter

1 Features

- Designed for Reliable and Rugged Applications
  - Wide Input Voltage Range: 7V to 100V
  - Junction Temperature Range: -40˚C to +150˚C
  - Peak and Valley Cycle-by-cycle Current Limit
  - VIN UVLO and Thermal Shutdown Protection
  - Open-drain Power Good Indicator
- Suited for Scalable Industrial Power Supplies and Battery Packs
  - Low Minimum on- and off-times of 50ns Supporting Wide Duty-cycle Range
  - Adjustable Switching Frequency up to 1.5MHz
  - 1% Internal Reference Voltage Accuracy
  - High Efficiency PSM in Light load (KP521001)
  - Forced-PWM in Light Load (KP521009)
  - 65μA No-load Input Quiescent Current
  - 3μA Shutdown Quiescent Current
- Integration Reduces Solution Size and Cost
  - CMCOT Control Architecture
  - Integrated 0.58Ω and 0.28Ω NFETs
  - Fixed 3ms Internal Soft-start Time
  - No Loop Compensation Components
  - Internal VCC Bias Regulator and Boot Diode
  - Optimized Pin-out for Single-layer Layout

2 Applications

- Appliances, Power and Garden Tools
- BMS (E-Bike, E-Scooter)
- Motor Drives, Drones, Telecom

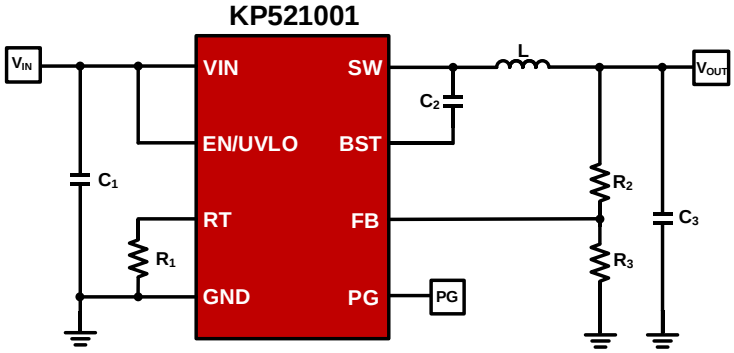
3 Description

The KP52100X is a synchronous buck converter operating over a wide input voltage range from 7V to 100V. A minimum controllable on-time of 50ns supports large step-down conversion ratios, enabling the direct step-down from a high-voltage BUS to low-voltage rails for reduced system complexity and solution cost. With integrated high-side and low-side MOSFETs, the KP52100X delivers up to 1A of output current with 3μA of shutdown current, making it an excellent choice for high cell count battery pack applications.

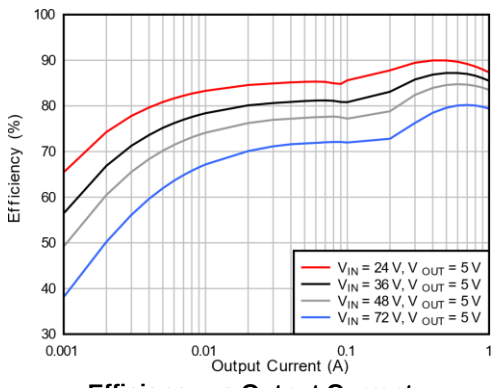
The KP52100X adopts Current Mode Constant On-Time (CMCOT) control architecture to achieve excellent load and line transient response. The KP52100x includes auto power-save-mode (PSM) operation for high light-load efficiency, programmable switching frequency from 100kHz to 1.5MHz for the flexibility to optimize either efficiency or external component size, an open-drain PGOOD indicator providing sequencing, fault reporting, and output voltage monitoring.

The KP52100X provides cycle-by-cycle current limit, over temperature protection, output over-voltage protection, output under-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin SOP-8 or ESOP-8 package.

Typical Application



Simplified Schematic



Efficiency vs Output Current

4 Ordering Information

Order Number[(1)]	Light Load Operation	Package	Eco Plan	MSL Rating	Packing	Device Marking
KP521001SGA	PSM	SOP-8	Halogen Free	3	T&R, 4000Pcs/Reel	KP521001
KP521009SGA	FPWM	SOP-8	Halogen Free	3	T&R, 4000Pcs/Reel	KP521009
KP521001ESGA	PSM	ESOP-8	Halogen Free	3	T&R, 4000Pcs/Reel	KP521001E
KP521009ESGA	FPWM	ESOP-8	Halogen Free	3	T&R, 4000Pcs/Reel	KP521009E

(1) KP521001 S G A

- Packing Code: A: Tape & Reel
- Eco Plan: G: Halogen Free
- Package Code: S: SOP-8 ES: ESOP-8
- Part Number

5 Marking Information

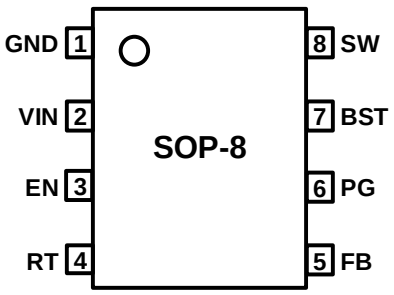
KP521001 — Device Marking

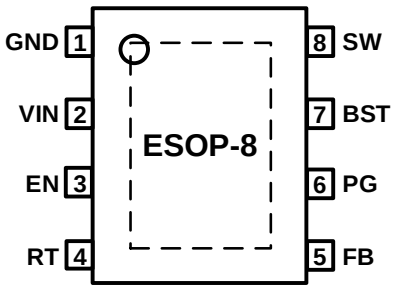
XXXXXX — Wafer Lot Code

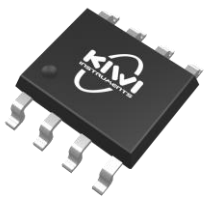
YWWZZF — Y: Year Code WW: Week Code ZZ: Serial Number F : Control Number[(1)]

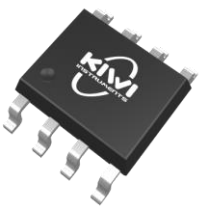
(1) Wafer Lot Code, Year Code, Week Code, Serial Number, and Control Number are numbers or letters

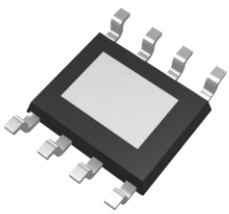
6 Pin Configuration











6.1 Pin Description

Pin Number	Pin Name	Type[(1)]	Description
1	GND	G	**System ground**. GND should be placed as close to the output capacitor as possible to avoid the high current switch paths. Connect the exposed pad to GND plane for optimal thermal performance.
2	VIN	P/I	**Supply voltage**. VIN supplies power to all of the internal control circuitries. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes.
3	EN/UVLO	I	**Enable control**. Driving EN high or leaving this pin floating enables the converter. An external resistor divider can be used to imply an adjustable VIN UVLO function.
4	RT	I	**Frequency programming input**. Float for 400 kHz, tie to GND for 800 kHz, or connect to an RT timing resistor.
5	FB	I	**Feedback Input**. Sense output voltage through the resistor divider for setting and controlling the output voltage.
6	PG	O	**Power good indicator**. This pin is an open-drain output pin. Connect to a source voltage through an external pullup resistor between 10kΩ to 100kΩ.
7	BST	P/I	**Bootstrap gate-drive supply**. Required to connect a high-quality 100nF ceramic capacitor between BST and SW to bias the internal high-side gate driver.
8	SW	P	**Switch node**. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
-	EP	-	**Exposed pad of the package**. No internal electrical connection. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

(1) G – Ground; I – Input; O – Output; P – Power

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40˚C to 125˚C (unless otherwise noted). [(1)]

Parameter		Min	Max	Unit
Voltage	VIN, EN	-0.3	105	V
	SW (DC)	-0.3	105	
	SW (AC, less than 20ns)	-3	105	V
	BST	-0.3	SW + 6	V
	BST to SW	-0.3	6	V
	RT, FB	-0.3	6	V
	PG	-0.3	16	V
T_J[(2)]	Operating Junction Temperature	-40	150	˚C
T_{STG}	Storage Temperature Range	-65	150	˚C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

7.2 ESD Rating

Parameter		Value	Unit
V_{ESD_HBM}	Human-body Mode (HBM)(1)	±2000	V
V_{ESD_CDM}	Charged-device (CDM)(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40˚C to 125˚C (unless otherwise noted).

Parameter		Min	Max	Unit
V_{IN}	Input supply voltage range	7	100	V
V_{OUT}	Output voltage range	1	30	V
I_{OUT}	Output current range	0	1	A
Voltage	SW (DC)	-0.1	100	V
	SW (AC, less than 20ns)	-3	100	V
	BST	-0.1	SW + 5.5	V
	BST to SW	-0.1	5.5	V
	EN, FB	-0.1	5.5	V
T_J	Operating Junction Temperature	-40	150	˚C
T_{STG}	Storage Temperature Range	-65	150	˚C

7.4 Thermal Information

Parameter		KP52100X	KP52100X	Unit
		ESOP-8	SOP-8	
$R_{\theta JA(EVM)}$(1)	Junction to Ambient Thermal Resistance (specific EVM)	48	60	˚C/W

(1) $R_{\theta JA(EVM)}$ is based on the thermal resistance information measured during the actual operation of the corresponding evaluation Module. EVM information: 60mm x 45mm, FR-4, TG150, 1.6mm thickness, 2-layer 2-Oz Cu copper. Operating Condition: V_{IN} = 48V, V_{OUT} = 5V I_{OUT} = 1A, T_A = 25˚C. This thermal resistance information is for reference only. The actual thermal resistance depends on PCB board, layout, and test environment conditions.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40˚C to +125˚C, unless otherwise stated. Minimum and maximum limits are specified through test design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25˚C and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 7V to 100V.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
V_{IN}	Operation input voltage		7		100	V
$V_{UVLO(R)}$	VIN UVLO rising threshold		6	6.5	7	V
$V_{UVLO(F)}$	VIN UVLO falling threshold		5.5	6	6.5	V
$I_{Q(SLEEP)}$	VIN quiescent current	V_{EN} = 2.5V, V_{FB} = 1.5V, I_{OUT} = 0mA		65		μA
$I_{Q(SD)}$	VIN shutdown current	V_{EN} = 0V, V_{IN} = 48V		3		μA
Enable and Soft-start						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.14	1.18	1.28	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	1.02	1.12	1.16	V
$I_{EN(P)}$	EN pin sourcing current pre EN rising threshold	V_{EN} = 1.0V	0.95	1.3	1.7	μA
$I_{EN(H)}$	EN pin sourcing current hysteresis	V_{EN} = 1.5V	2.5	3.1	3.81	μA
t_{SS}	Internal fixed soft-start time	From 1st switching pulse until target V_{OUT}		3		ms
Reference Voltage						
V_{FB}	Feedback voltage	T_J = 25˚C	1.188	1.2	1.212	V
		T_J = -40˚C to 125˚C		1.2		V
$I_{FB(LKG)}$	Feedback leakage current		-100	10	100	nA
Power Switches						
$R_{DSON(HS)}$	High-side MOSFET On-resistance	T_J = 25˚C, V_{IN} = 48V, V_{BST-SW} = 5 V		580		mΩ
$R_{DSON(LS)}$	Low-side MOSFET On-resistance	T_J = 25˚C, V_{IN} = 48V		280		mΩ
Switching Frequency and Timing						
f_{SW}	Switching frequency range		100		1500	kHz
$t_{ON(min)}$	Minimum ON pulse width			50		ns
$t_{OFF(min)}$	Minimum OFF pulse width			190		ns

Current Limit						
$I_{HS(OC)}$	High-side peak current limit	Peak current limit on HSF	1.3	1.5	1.7	A
$I_{LS(OC)}$	Low-side valley current limit	Valley current limit on LSF, V_{IN} = 48V	1	1.2	1.4	A
$I_{LS(NOC)}$	Low-side negative current limit for FPWM	Sink current limit on LSF, V_{IN} = 48V		0.6		A
Output UVP and OVP						
$V_{UVP(F)}$	UVP falling threshold	V_{FB} falling	61	65	69	$\%V_{FB}$
$V_{UVP(R)}$	UVP rising threshold	V_{FB} rising	66	70	74	$\%V_{FB}$
$V_{OVP(R)}$	OVP rising threshold	V_{FB} rising	112	116	120	$\%V_{FB}$
$V_{OVP(F)}$	OVP falling threshold	V_{FB} falling	107	111	115	$\%V_{FB}$
$t_{HIC(WAIT)}$	Wait time before entering Hiccup			120		μs
$t_{HIC(RE)}$	Hiccup time before restart			6		Cycles
Power Good						
V_{PGTH}	Power Good threshold	FB falling, PG from high to low	82	87	92	$\%V_{FB}$
		FB rising, PG from low to high	87	92	97	$\%V_{FB}$
		FB falling, PG from low to high	107	111	115	$\%V_{FB}$
		FB rising, PG from high to low	112	116	120	$\%V_{FB}$
$V_{PG(OL)}$	PG pin output low-level voltage	I_{PG} = 5.5mA			0.4	V
R_{PG}	PG pulldown resistance	V_{FB} = 1V		72		Ω
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 15V	-1		1	μA
$t_{PG(R)}$	PG delay going from low to high			96		μs
$t_{PG(F)}$	PG delay going from high to low			48		μs
	Minimum VIN for valid output(1)	$V_{PG/SS}$ < 0.4V at 1mA		2	2.5	V
Over Temperature Protection(1)						
$T_{J(SD)}$	Thermal shutdown threshold			160		˚C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		˚C

(1) Not production test, guaranteed by design.

7.6 Typical Characteristics

Unless otherwise noted, the following conditions apply: V_{IN} = 48V, T_A = 25°C.

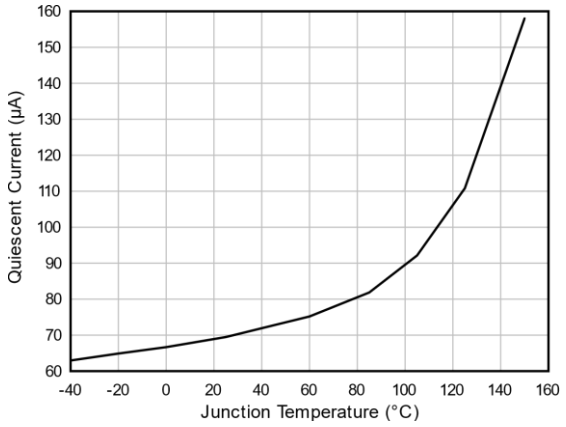


Figure 1. VIN Quiescent Current (KP521001) vs Junction Temperature

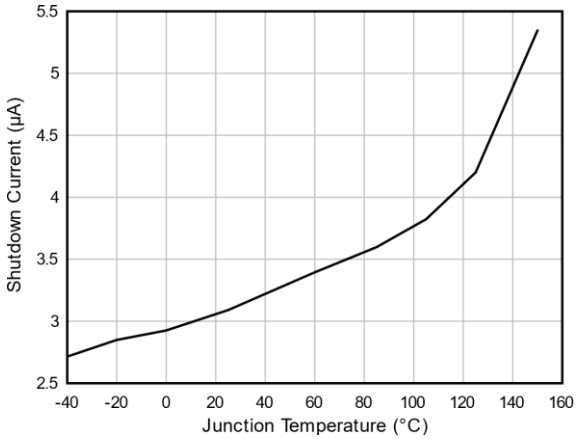


Figure 2. VIN Shutdown Current vs Junction Temperature

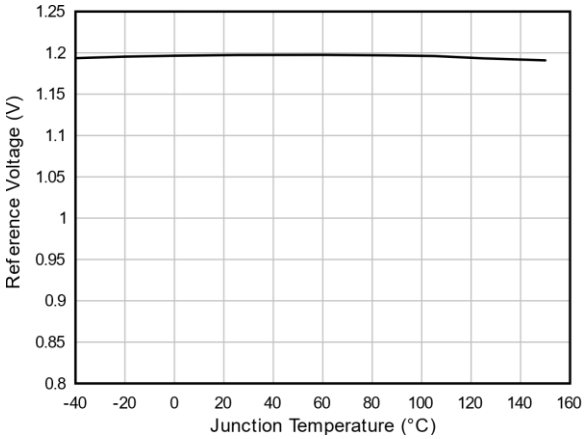


Figure 3. Reference Voltage vs Junction Temperature

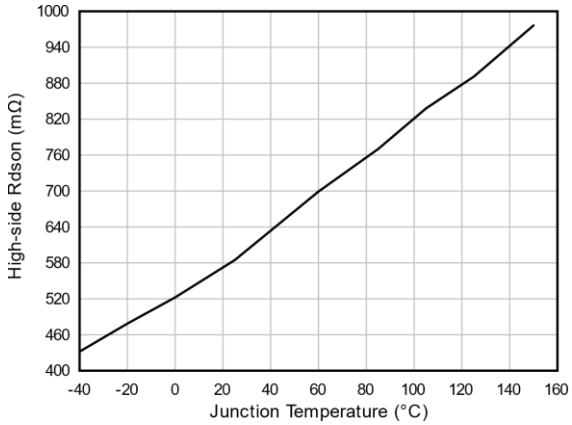


Figure 4. High-side MOSFET On-resistance vs Junction Temperature

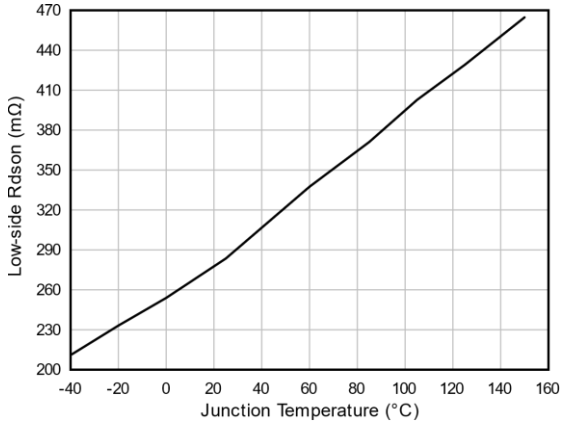


Figure 5. Low-side MOSFET On-resistance vs Junction Temperature

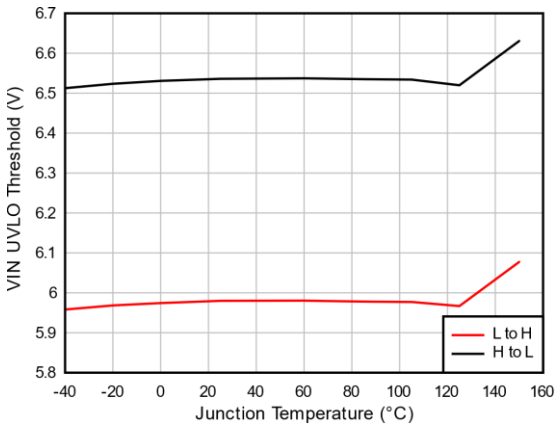


Figure 6. VIN UVLO Threshold vs Junction Temperature

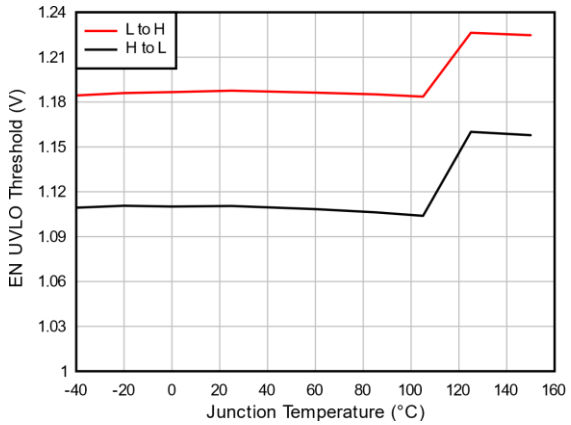


Figure 7. EN Threshold vs Junction Temperature

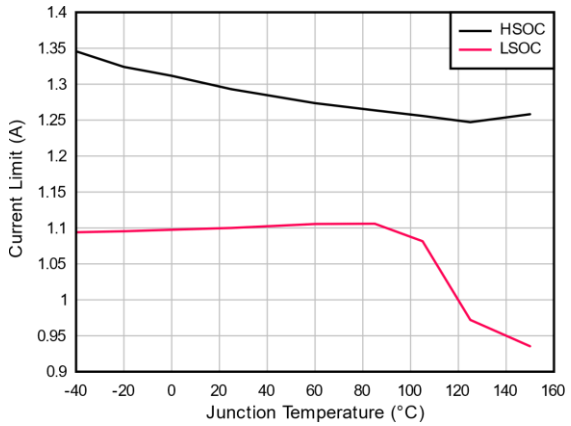


Figure 8. Peak and Valley Current Limit Threshold vs Junction Temperature

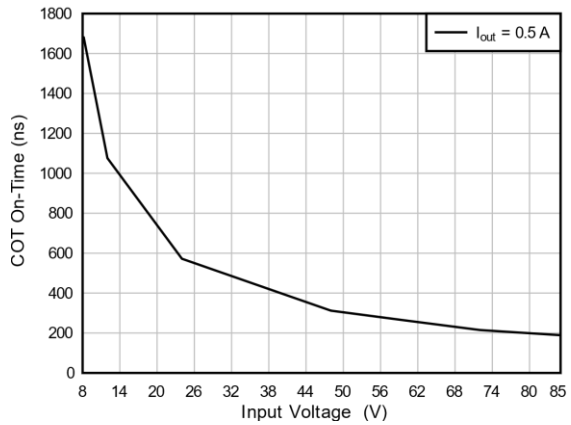
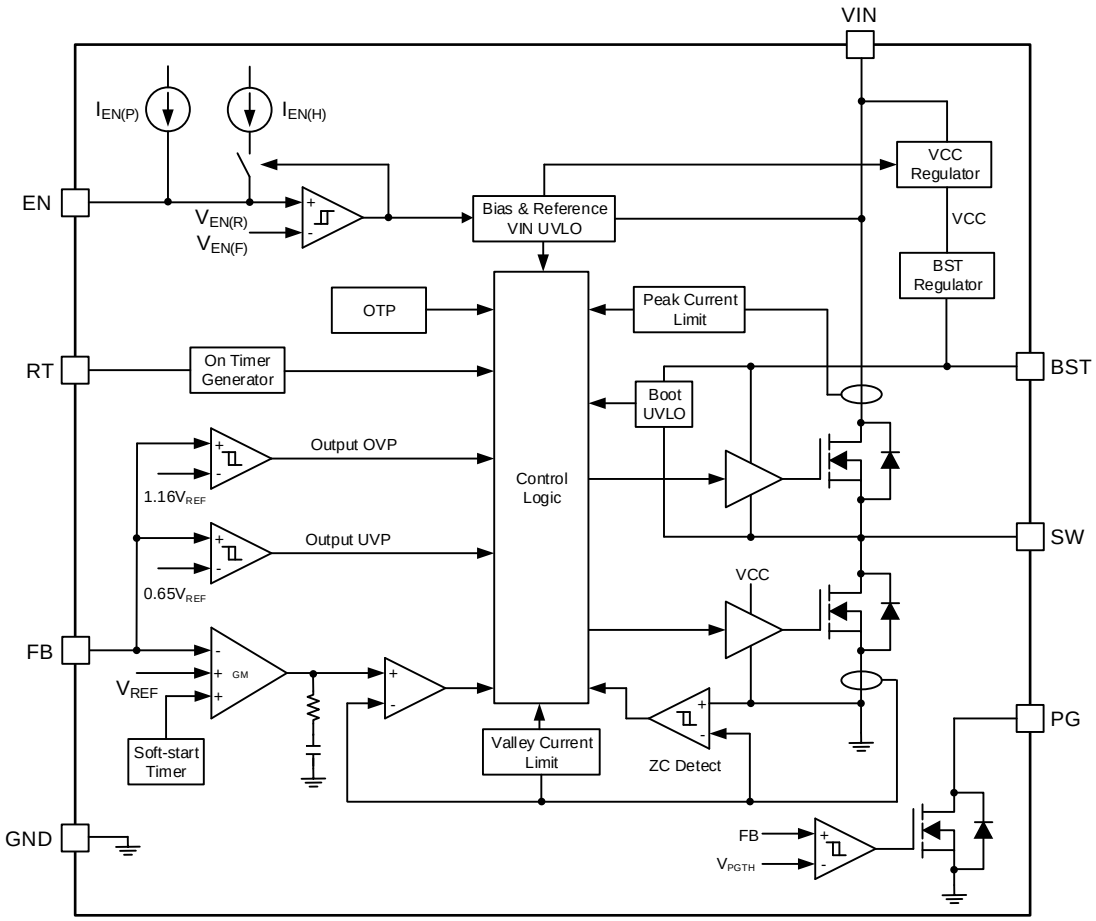


Figure 9. COT On-Time vs V_{IN}

8 Block Diagram



9 Operation Description

The KP52100X is a synchronous, step-down switching converter with integrated power MOSFETs. It provides high efficiency via current mode constant on time (CMCOT) control for fast loop response and easy loop stabilization. The device features a wide input voltage range (7V to 100V), open-drain PGOOD indicator, internal soft-start (SS) control, and precise current limiting.

9.1 Current Mode Constant On-Time Mode Control

The KP52100X step-down switching converter employs a CMCOT control scheme. The CMCOT control scheme sets a fixed on-time t_{ON} of the high-side MOSFET (HSF) using a timing resistor (RT). The t_{ON} is adjusted as Vin changes and is inversely proportion to input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). CMCOT converters also contain a current sense and error amplifier. The error amplifier EA adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 1.2V reference. After expiration of t_{ON}, the high side FET remains off until the falling slope of the current crossed with the COMP voltage. Current is therefore sensed in the lower MOSFET which is much easier to do and less prone to noise pick-up, especially in low duty-cycle conditions. The fact that the system does not need to wait for a next clock-cycle makes it possible to react more quickly to sudden step loads; as soon as the output voltage drops and the error amplifier voltage rises above the falling current slope, a new ON time is triggered and converter current rises again.

9.2 Power Save Mode (PSM, KP521001 Only)

The KP521001 automatically enters power saving mode (PSM) at light-load conditions to maintain high efficiency. As the load current decreases, the inductor current ripple valley eventually touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET (LSF) is turned off when the zero-inductor current is detected. In this case, the output capacitor is only discharged by load current so that the switching frequency decreases. As the result, the light-load efficiency can be enhanced due to lower switching loss.

9.3 Force Pulse Width Modulation (FPWM) Mode (KP521009 Only)

The KP521009 operates in FPWM mode at light-load conditions to maintain tight output voltage ripples. The LSF is forced on when the HSF is in its off state and after the dead time of 10ns, until the next cycle HSF turns on. This mode allows inductor current flowing from output capacitor to the switching node through LSF's drain-to-source terminals, which is called negative current. In this case, the switching frequency nearly keeps constant over full range of load current achieving tight output voltage ripples.

9.4 Switching Frequency

The switching frequency is set by the condition of the RT input. The condition of this input is detected when the device is first enabled. Once the converter is running, the switching frequency selection is fixed and cannot be changed until the next power-on cycle or EN toggle.

In resistor setting frequency mode, a resistor placed between RT pin to the ground sets the switching frequency over a wide range from 100kHz to 1.5MHz. Use Equation **(1)** to determine the resistance for a switching frequency needed. The RT pin can be float or tied to GND to set the switching frequency at 400kHz or 800kHz.

$$\mathbf{R_{RT}(k\Omega)} = \frac{\mathbf{48000}}{\mathbf{F_{SW}(kHz)}} \quad (1)$$

Table 1Design Example Parameters

RT Pin Status	Switching Frequency
Floating	400kHz
Tie to GND	800kHz
External RT Resistor	100~1500kHz

9.5 Bootstrap Voltage Regulator

An external bootstrap capacitor between BST pin and SW pin powers the floating gate driver to HSF. The bootstrap capacitor voltage is charged from an integrated voltage regulator when HSF is off and LSF is on.

9.6 Precise Enable Control and Under-voltage Lock-out Adjustment

The KP52100x provides an EN pin, as an external IC enable control, to enable or disable the device. When the EN pin voltage rises above the rising threshold voltage ($V_{EN(R)}$) while the VIN voltage is higher than VIN under-voltage lock-out threshold ($V_{UVLO(R)}$), the device turns on. If the EN pin voltage is pulled below the falling threshold voltage ($V_{EN(F)}$), the regulator stops switching and enters the shutdown mode, that is, the regulator is disabled and switching is inhibited even if the VIN voltage is above VIN under-voltage lock-out threshold ($V_{UVLO(R)}$). During shutdown mode, the supply current can be reduced to $I_{Q(SD)}$ (typical 3μA).

The EN pin has an internal pullup source current, which allows users to float the EN pin to enable the device. If an application requires control of the EN pin, external control logic interface like open drain or open-collector output logic can be connected to the EN pin.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

VIN under-voltage lock-out (UVLO) protects the IC from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold ($V_{UVLO(R)}$) is about 6.5V, while its falling threshold ($V_{UVLO(F)}$) is 6V. If V_{EN} rises above $V_{EN(R)}$ first, switching will still be inhibited until the V_{IN} rises

above $V_{UVLO(F)}$. After the device is powered up, if the input voltage V_{IN} goes below $V_{UVLO(F)}$, this switching will be inhibited. If V_{IN} rises above $V_{UVLO(R)}$, the device will resume normal operation with a complete soft-start.

If an application requires a higher VIN UVLO threshold, EN pin can be configured as shown in **Figure 10**. When using the external VIN UVLO function, setting the hysteresis at a value greater than 500mV is recommended.

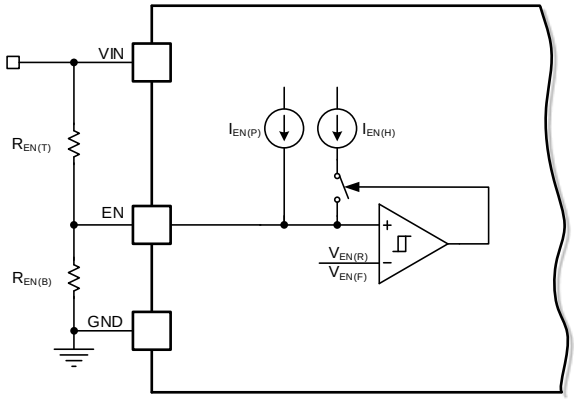


Figure 10 Adjustable VIN Under-Voltage Lock-Out

The EN pin has a small pull-up current ($I_{EN(P)}$), which sets the default state of the EN pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the external VIN UVLO function because it increases by $I_{EN(H)}$ when the EN pin voltage rises above the EN rising threshold $V_{EN(R)}$. Use below equations to calculate the values of $R_{EN(TOP)}$ and $R_{EN(BOT)}$ for a specified VIN UVLO threshold, where $V_{IN(START)}$ and $V_{IN(STOP)}$ are the expected input voltage enabling/disabling the device.

$$R_{EN(T)} = \frac{V_{IN(START)}\frac{V_{EN(F)}}{V_{EN(R)}} - V_{IN(STOP)}}{I_{EN(P)}\left(1-\frac{V_{EN(F)}}{V_{EN(R)}}\right)+I_{EN(H)}} \quad (2)$$

$$R_{EN(B)} = \frac{R_{EN(T)}V_{EN(F)}}{V_{IN(STOP)}-V_{EN(F)}+R_{EN(T)}(I_{EN(P)}+I_{EN(H)})} \quad (3)$$

Where,

- $V_{IN(START)}$ is the start operation voltage
- $V_{IN(STOP)}$ is the stop operation voltage
- $I_{EN(P)}$ = 1.2μA, $I_{EN(H)}$ = 2.9μA
- $V_{EN(R)}$ = 1.2V, $V_{EN(F)}$ = 1.14V

9.7 Power Good

The KP52100x provides a PGOOD flag pin to indicate when the output voltage is within the regulation level. Use the PGOOD signal for start-up sequencing of downstream converters or for fault protection and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 16 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail.

Once the FB pin voltage is between 92% and 111% of the internal reference voltage and after a deglitch time of 96μs, the PG is high impedance. The PG pin is pulled low after a deglitch time of 48μs. When the FB pin voltage is lower than UVP or greater than OVP threshold, or in events of thermal shutdown, EN shutdown, or UVLO conditions. VIN must remain present for the PG pin to stay low.

9.8 Soft Start and Pre-biased Soft Start

The KP52100X provides an internal soft-start feature to ensure inrush control and smooth output voltage ramping during power-up, and the output voltage starts to rise after a 440us delay from EN rising edge. When the IC starts, the soft-start circuitry generates a soft-start voltage (SS) ramping up from 0V. When it is below the internal reference voltage (V_{REF}), SS overrides V_{REF} so the error amplifier and comparator use SS as the reference voltage. The output voltage smoothly ramps up. Once SS rises above V_{REF}, V_{REF} regains control. At this time the soft start process ends and the KP52100x enters steady state operation. The soft start time (T_{SS}) is internal fixed at around 3ms (10% to 90%).

If the output capacitor is pre-biased at startup, the KP52100x initiates switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the converters ramp up smoothly into regulation point.

9.10 Output Under-Voltage Protection

The KP52100x includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (V_{UVP}) (typically 65% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFETs.

If the output under-voltage condition continues for a period of time ($T_{HCP(WAIT)}$), the KP52100x will enter output under-voltage protection (UVP) with hiccup mode. During hiccup mode, the IC will shut down for $T_{HICCUP(OFF)}$, and then attempt to recover automatically. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. The hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then the converter resumes normal operation as soon as the over-load or short-circuit condition is removed.

9.11 Peak and Valley Over-Current Limit

The KP52100x implements over current protection with cycle-by-cycle limiting peak and valley current to avoid inductor current running away during unexpected overload or output hard short condition.

9.12 Negative Over-Current Limit (KP521009 Only)

The KP521009 is the part which is FPWM part and allows negative current operation. In case of FPWM operation, high negative current may be generated as an external power source is tied to output terminal unexpectedly. As the risk described above, the internal circuit monitors negative current in each on-time interval of LSF and compares it with negative over-current (NOC) limit threshold (I_{NOC}). Once the negative current exceeds the NOC threshold, the LSF is turned off immediately, and then the HSF will be turned on to discharge the energy of output inductor. This behavior can keep the valley of negative current at NOC threshold to protect LSF. Note that the NOC limit is not in effect during minimum off-time period.

9.13 Output Over-Voltage Protection

The KP52100x integrates output over-voltage protection (OVP) to minimize output voltage overshoot and protect down-stream devices when recovering from output fault conditions or strong unload transients. The OVP circuitry detects overvoltage condition by monitoring the feedback voltage (V_{FB}). When V_{FB} rises above the OVP threshold (V_{OVP}), the OVP comparator output turns high and both HSF and LSF turns off to avoid V_{OUT} further rising higher. Once the V_{OUT} drops below V_{OVP}, the device starts to switch again. This function is a non-latch operation.

9.14 Over Temperature Protection

The KP52100x includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold ($T_{J(SD)}$). Once the junction temperature cools down by a thermal shutdown hysteresis ($T_{J(HYS)}$), the IC will resume normal operation with a complete soft-start.

10 Application Information

The KP52100X only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. Several features are integrated to meet system design requirements, including precision enable, input voltage UVLO, internal soft start, programmable switching frequency, and a PGOOD indicator. The external components should fulfill the needs of the application, but also the stability criteria of the device's control loop. **Figure 39** and **Table 3** can be used to simplify the output filter component selection.

10.1 Design Requirements

Detailed design procedure is described based on a design example. For this design example, use the parameters listed in **Table 2** as the design parameters.

Table 2Design Example Parameters

Parameter	Value
Input voltage	7V ~ 100V
Output voltage	5V
Maximum output current	1A
Switching frequency	400kHz
Output voltage ripple (peak to peak)	50mV
Transient response, 0.1A to 0.9A load step	ΔV=250mV

10.2 Output Voltage

As shown in **Figure 11** Output Voltage Setting. The output voltage is set by an external resistor divider connected to the FB pin.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB(T)}}{R_{FB(B)}}\right) \quad (4)$$

Where,

- V_{REF} = 1.2V

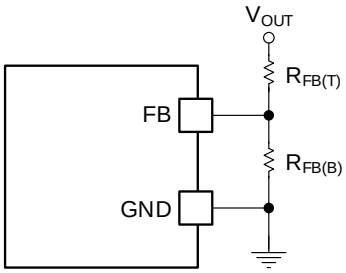


Figure 11 Output Voltage Setting

It is recommended to design from the bottom side feedback resistor $R_{FB(B)}$. Too large $R_{FB(B)}$ will make the FB pin more susceptible to external noises, while too small $R_{FB(B)}$ will increase the power loss of the resistor divider. $R_{FB(B)}$ = 10kΩ~50kΩ is recommended. And the top side feedback resistor $R_{FB(T)}$ can be calculated by the following formula:

$$R_{FB(T)} = R_{FB(B)} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \quad (5)$$

For example, in the application with 5V output voltage, First, chose $R_{FB(B)}$ as 10kΩ and then $R_{FB(T)}$ is calculated as 31.6kΩ, so the nearest nominal resistor of 31.6kΩ is chosen.

In the application scenarios where higher precision of output voltage is required, it is recommended to select a voltage resistor divider with a precision of 1% or even higher.

10.3 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation **(6)** to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} should be 20% to 50%. During an instantaneous over current operation event, the RMS and peak inductor current can be high. The inductor current rating should be a bit higher than

current limit.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \quad (6)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT\_rated} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (7)$$

Where,

- I_{OUT_rated} = 1.8A, the rated output current.

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load could be falsely triggered. It also generates more inductor core loss since the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 20.2µH. Choose the standard 22-µH ferrite inductor with a capability of 2-A RMS current and 3-A saturation current.

10.4 Output Capacitor Selection

The selection of output capacitor is related to the output voltage ripple and load transient performance. Output voltage ripple V_{RIPPLE} consists of two main parts. One is the resistive ripple $V_{RIPPLE(ESR)}$ generated by the inductive current at the equivalent series resistance ESR of the output capacitor. The other part is capacitive ripple $V_{RIPPLE(C)}$ generated by charging and discharging the output capacitor with the inductance ripple current. The calculation formula is as follows:

$$V_{RIPPLE} = \sqrt{V_{RIPPLE\_ESR}^2 + V_{RIPPLE\_C}^2} \quad (8)$$

$$V_{RIPPLE\_ESR} = \Delta i_L \times ESR \quad (9)$$

$$V_{RIPPLE\_ESR} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{sw}} \quad (10)$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

$$V_{RIPPLE} > \mathrm{Max}(V_{RIPPLE\_ESR}, V_{RIPPLE\_C})$$
$$V_{RIPPLE} < V_{RIPPLE\_ESR} + V_{RIPPLE\_C} \quad (11)$$

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. The selected output capacitor must be rated for a voltage greater than the desired output voltage plus half of the ripple voltage.

10.5 Input Capacitor Selection

The step-down converter has a discontinuous input current and requires a capacitor to supply AC current to the step-down converter while also maintaining the DC input voltage. Use low ESR capacitors as close to VIN as possible for the best performance, especially under high switching frequency applications. Due to a capacitor's de-rating under DC bias, the bias can significantly reduce capacitance. The voltage rate of the input capacitor is recommended to be twice higher than the maximum input voltage.

The RMS current through the input capacitor can be calculated with Equation **(14)**.

$$I_{IN\_AC} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (12)$$

The worst-case scenario occurs at $V_{IN} = 2V_{OUT}$, calculated with below Equation **(13)**.

$$I_{IN\_AC} = \frac{I_{OUT}}{2} \quad (13)$$

With low ESR capacitors, the input voltage ripple can be estimated with Equation **(14)**.

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{OUT}}{F_{sw} \times C_{IN} \times V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

The worst-case scenario occurs at V_{IN} = 2V_{OUT}, calculated with below Equation **(15)**.

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{sw} \times C_{IN}} \quad (15)$$

Choose an input capacitor with enough RMS current rating and enough capacitance for small input voltage ripples.

In addition, to optimize the EMI performance and ensure the reliable and stable operation of the chip, besides using the ceramic capacitor as the input capacitor C_{IN}, it is recommended to add another 0.1μF ceramic capacitor (0603/0402 package) to the VIN and GND pins as close as possible. It is important to note that although the ceramic capacitor has excellent high-frequency performance and stable lifetime, but due to the low ESR characteristics of ceramic capacitor, the actual input voltage may start ringing in some input hot-plug scenarios, and the worst input voltage even may ring to 2 times nominal voltage, thus this over-voltage ringing may breakdown IC. In this case, it is recommended to add an additional electrolytic capacitor with large ESR in parallel at the input voltage end or to add a TVS diode to limit or clamp the input over-voltage ringing.

10.6 Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between the BST to SW pin for proper operation. At least 10V X5R or X7R 0.1μF ceramic capacitor of 0603 package is recommended.

10.7 Feedforward Capacitor Selection

KP52100x adopts CMCOT control architecture to achieve ultra-fast load transient response performance. In some applications where the load transient response is more demanding, the transient response performance can be further improved by adding feedforward capacitor C_{FF} across the top FB divider resistor. It is recommended to optimize the C_{FF} selection through bench checks of load transient response and load regulation performance.

10.8 PCB Layout Guidelines

PCB design is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Place the input ceramic capacitor as close to VIN and GND pins as possible.
2. The trace of the main power loop CIN→L→COUT→GND should be as short and wide as possible to reduce trace voltage drop and improve conversion efficiency.
3. The SW node voltage is high frequency square wave. Appropriately reducing the size of SW node can improve EMI performance; On the other hand, appropriately increasing the size of SW node can optimize heat dissipation performance. Take appropriate compromise according to the actual situation is recommended.
4. The FB trace should be as far away from noise sources as possible, such as SW node and BST node.
5. The sampling point of the output voltage V_{OUT} should be placed near the end of the output capacitors and place the voltage divider resistors near the FB pin.
6. The trace and copper of VIN and GND node should be as wide as possible to help heat dissipation. In multilayer PCB designs, it is recommended to leave a complete GND layer for the GND node and to add enough vias between the GND layer and the chip layer.
7. The RT pin is sensitive to noise. Thus, locate the RT resistor as close as possible to the device and route with minimal lengths of trace.

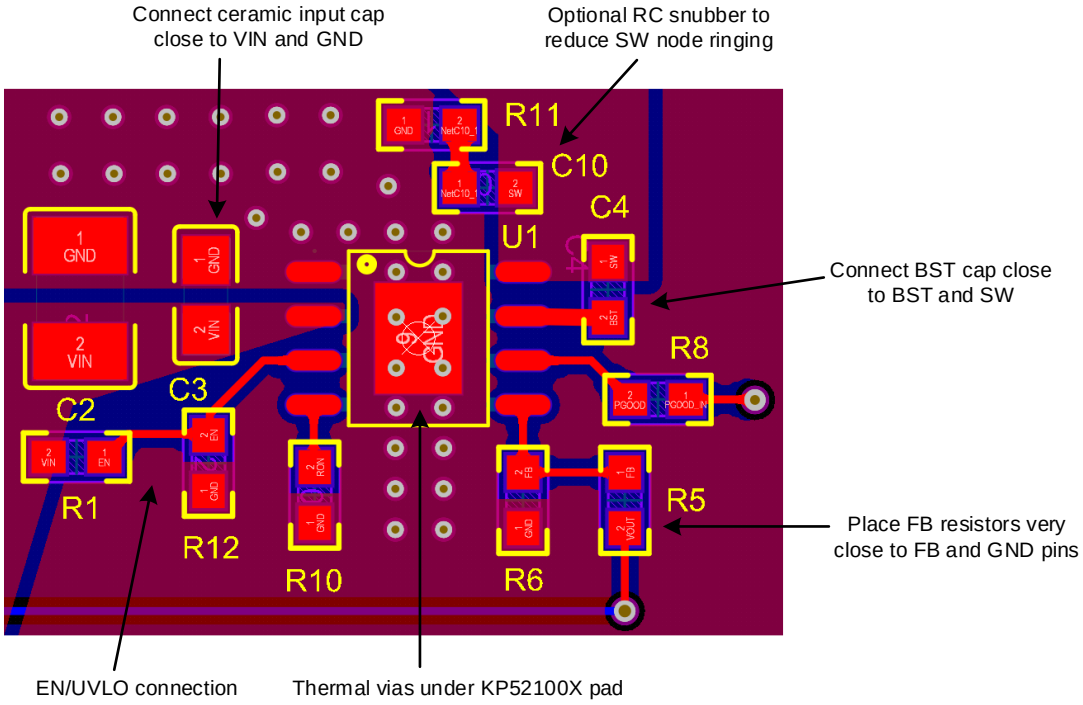


Figure 12 PCB Layout Example

10.9 Application Curves

V_{IN} = 48V, T_A = 25°C, F_{SW} = 400kHz, L_1 = 33µH, DCR = 65mΩ, C_{OUT} = 44µF, unless other noted.

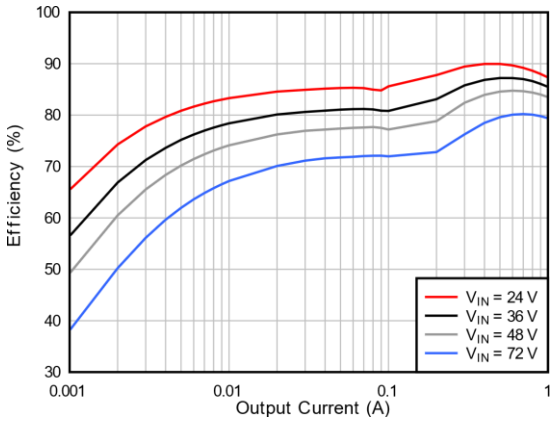


Figure 13 KP521001 Efficiency
(V_{OUT} = 5V, L_1 = 33µH, DCR = 65mΩ)

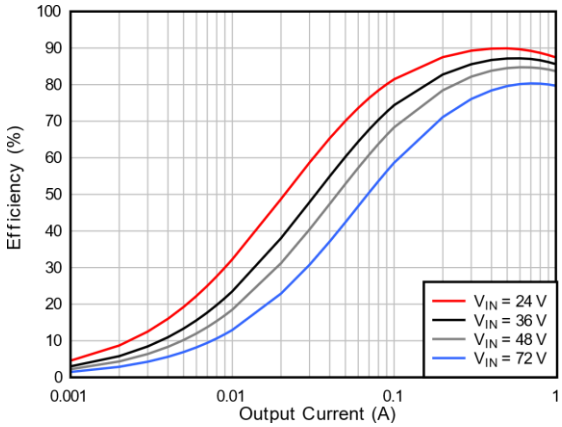


Figure 14 KP521009 Efficiency
(V_{OUT} = 5V, L_1 = 33µH, DCR = 65mΩ)

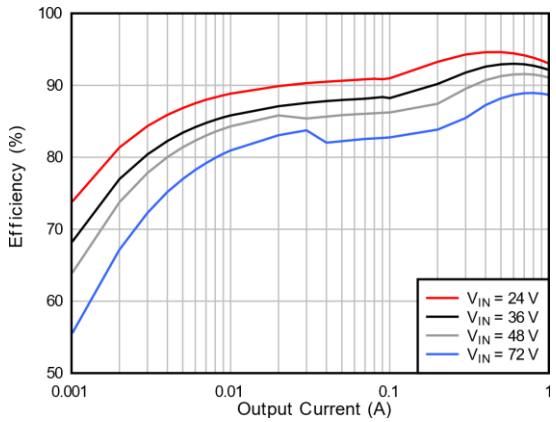


Figure 15 KP521001 Efficiency
(V_{OUT} = 12V, L_1 = 56µH, DCR = 110mΩ)

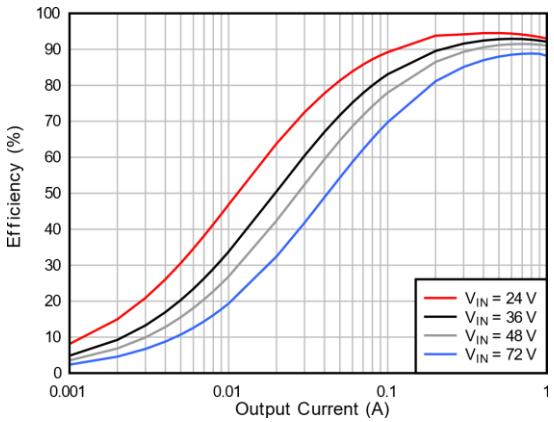


Figure 16 KP521009 Efficiency
(V_{OUT} = 12V, L_1 = 56µH, DCR = 110mΩ)

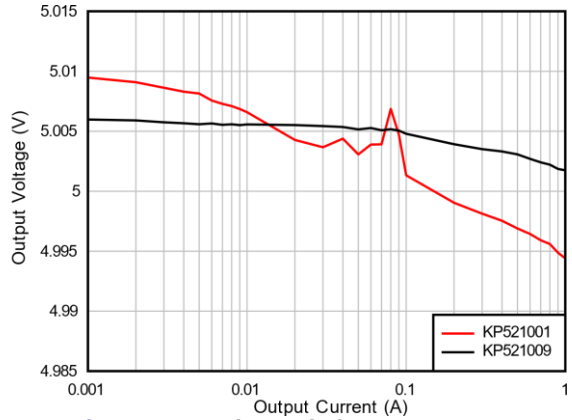


Figure 17 Load Regulation, V_{IN} = 48V

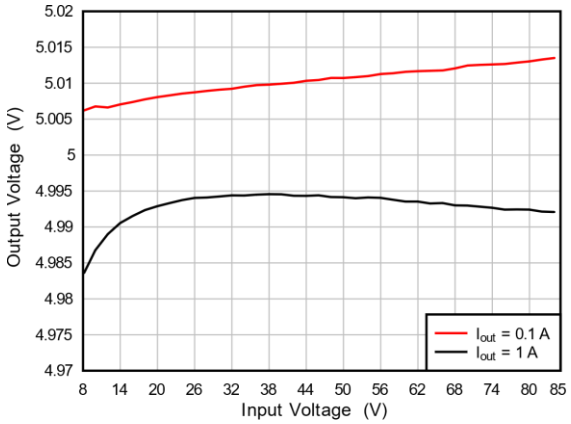


Figure 18 Line Regulation

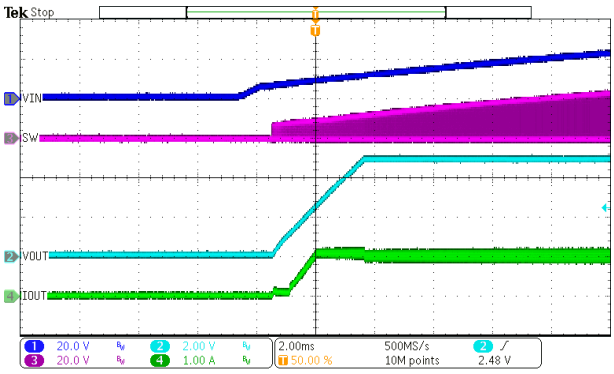


Figure 19 Start-up through VIN

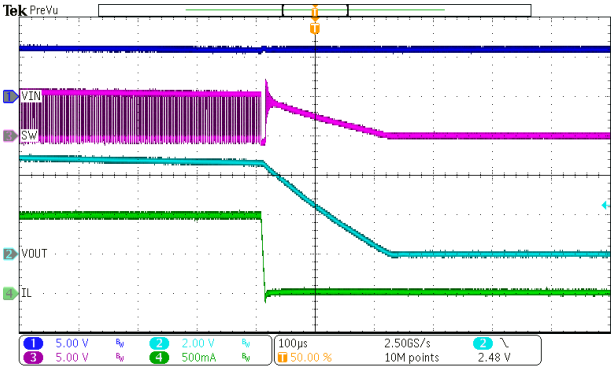


Figure 20 Shutdown through VIN

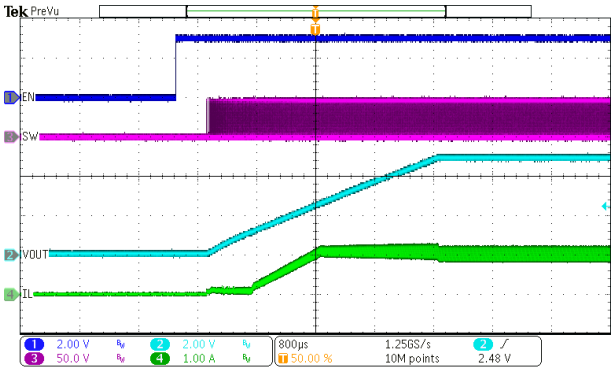


Figure 21 Start-up through EN

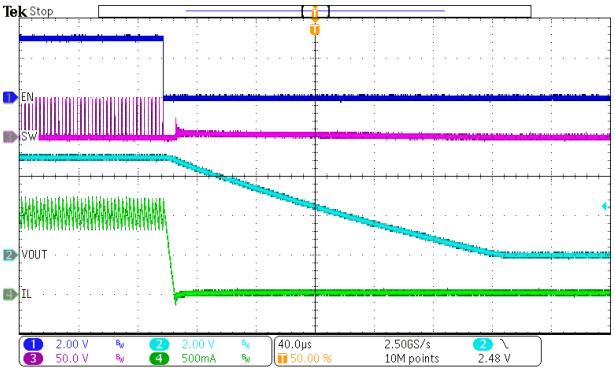


Figure 22 Shutdown through EN

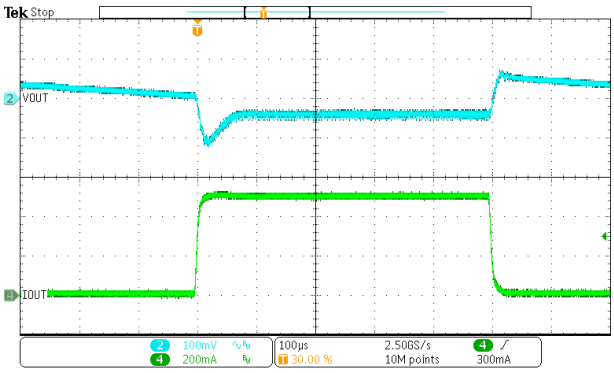


Figure 23 KP521001 Load Transient

(From 0A to 0.5A, 0.16A/µs)

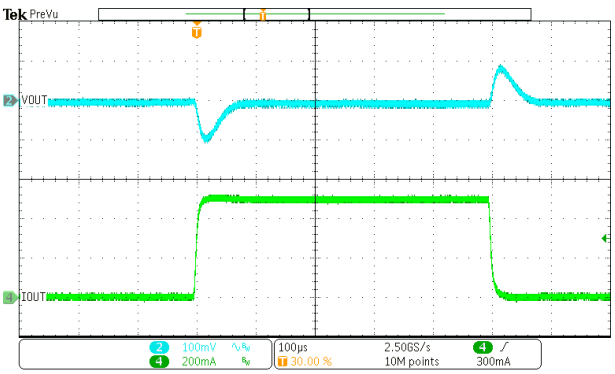


Figure 24 KP521009 Load Transient

(From 0A to 0.5A, 0.16A/µs)

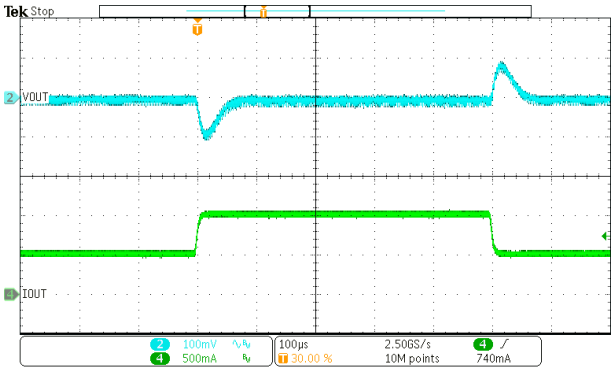


Figure 25 KP521001 Load Transient
(From 0.5A to 1A, 0.16A/µs)

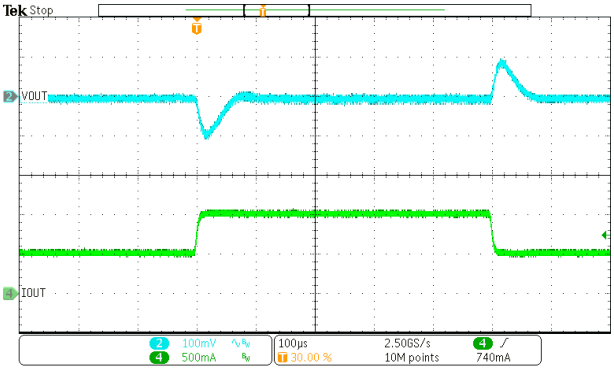


Figure 26 KP521009 Load Transient\
(From 0.5A to 1A, 0.16A/µs)

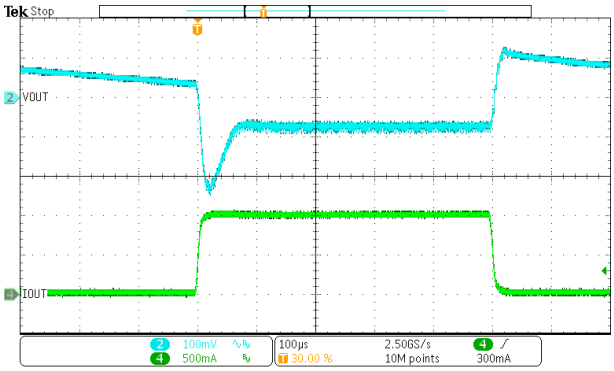


Figure 27 KP521001 Load Transient\
(From 0A to 1A, 0.16A/µs)

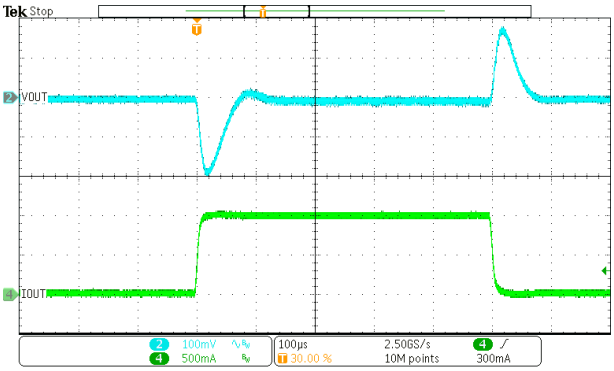


Figure 28 KP521009 Load Transient\
(From 0A to 1A, 0.16A/µs)

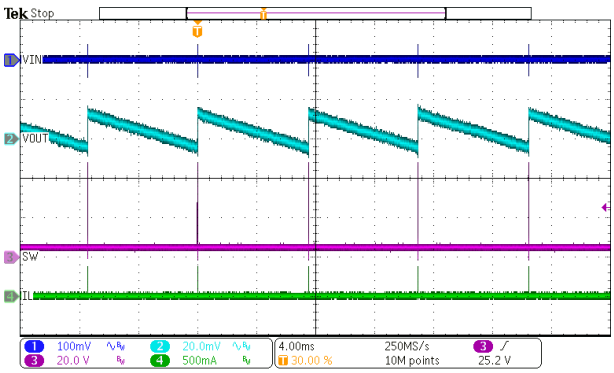


Figure 29 KP521001 SW and Vout Ripple, I_{OUT} = 0A

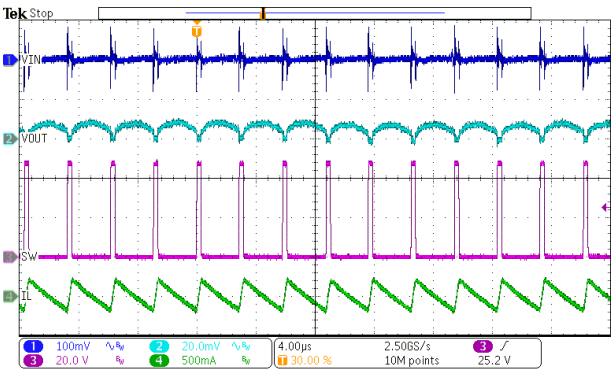


Figure 30 KP521009 SW and Vout Ripple, I_{OUT} = 0A

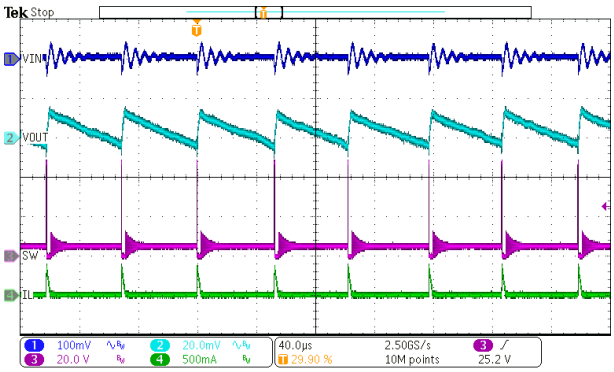


Figure 31 KP521001 SW and Vout Ripple, I_{OUT} = 0.01A

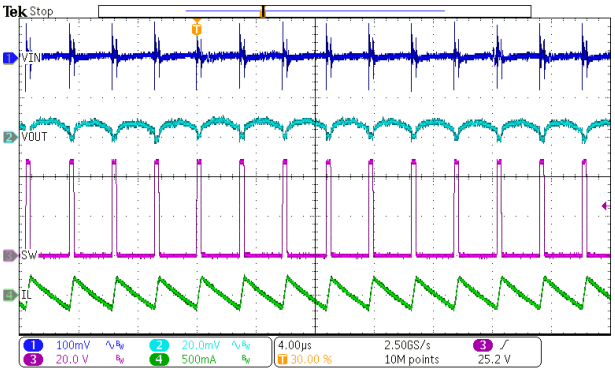


Figure 32 KP521001 SW and Vout Ripple, I_{OUT} = 0.01A

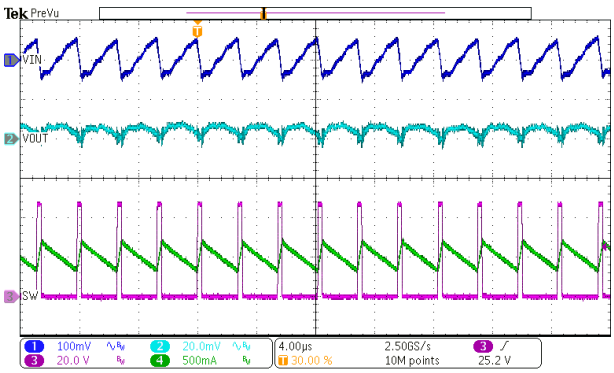


Figure 33 SW and Vout Ripple, I_{OUT} = 0.5A

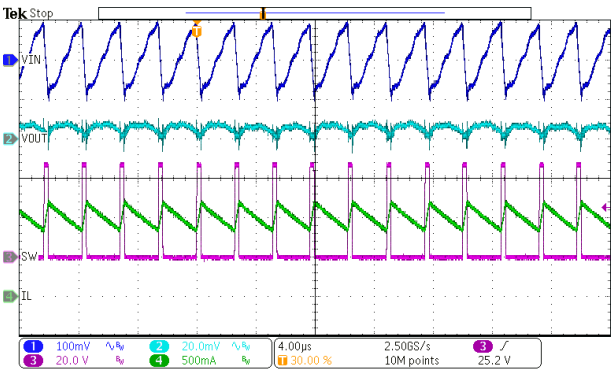


Figure 34 SW and Vout Ripple, I_{OUT} = 1A

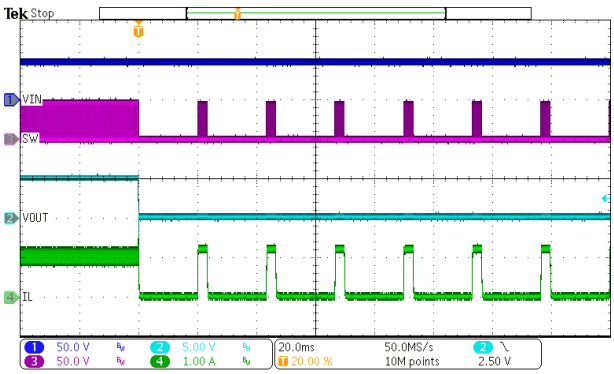


Figure 35 Output Short Entry

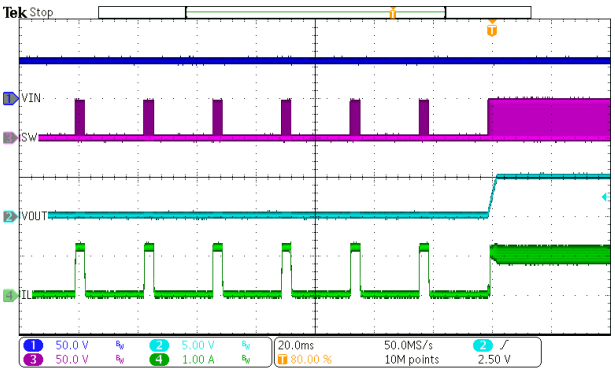


Figure 36 Output Short Recovery

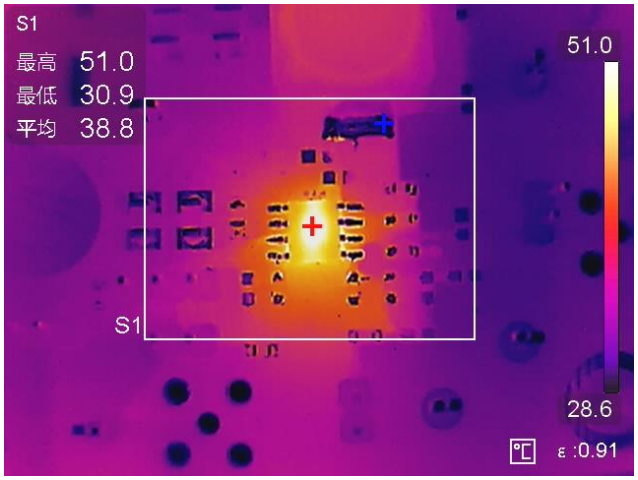


Figure 37 Thermal Performance

V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 1A

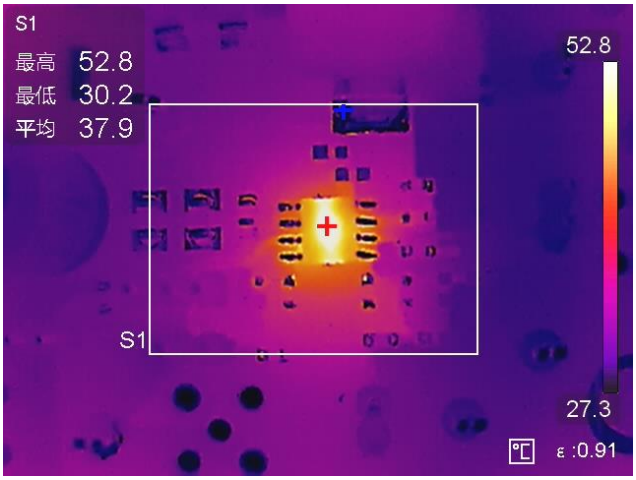


Figure 38 Thermal Performance

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A

11 Typical Application Circuit

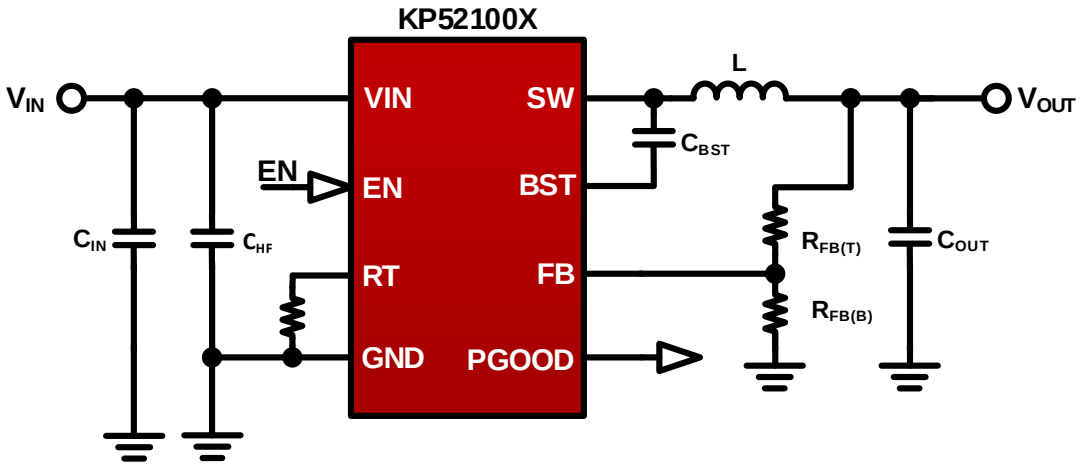


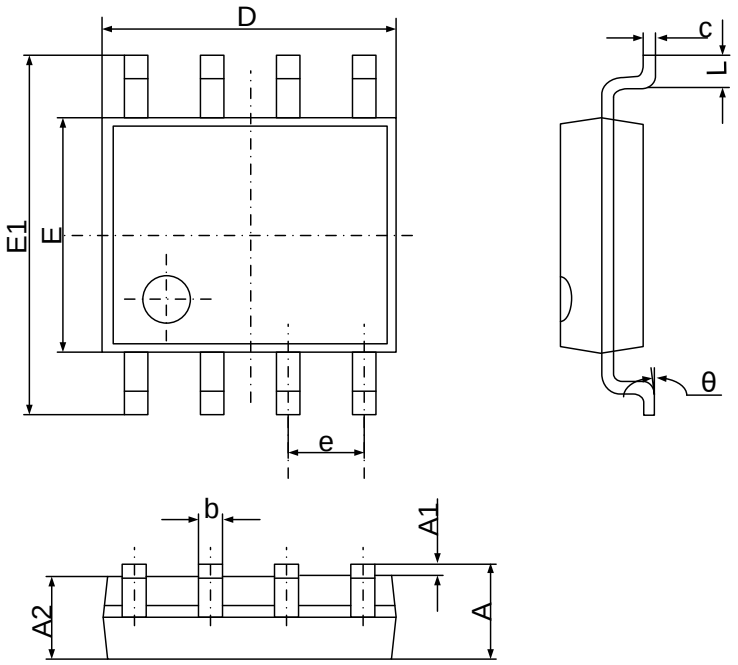
Figure 39 Typical Application Circuit

Table 3 Recommended Components

F_{SW} (kHz)	RT	V_{OUT} (V)	L (µH)	C_{OUT}	$R_{FB(T)}$ (kΩ)	$R_{FB(B)}$ (kΩ)	C_{IN} + C_{HF}	C_{BST}
400	120kΩ or RT Floating	3.3	22	2 x 22µF / 10V	17.6	10	10µF + 100nF	100nF
		5	33	2 x 22µF / 10V	31.6	10	10µF + 100nF	100nF
		12	56	2 x 22µF / 25V	90	10	10µF + 100nF	100nF
		24	100	100µF / 50V, E-cap + 1µF / 50V	190	10	10µF + 100nF	100nF
800	60kΩ or RT tie to GND	3.3	10	2 x 22µF / 10V	17.6	10	10µF + 100nF	100nF
		5	15	2 x 22µF / 10V	31.6	10	10µF + 100nF	100nF
		12	33	2 x 22µF / 25V	90	10	10µF + 100nF	100nF
		24	47	100µF / 50V, E-cap + 1µF / 50V	190	10	10µF + 100nF	100nF

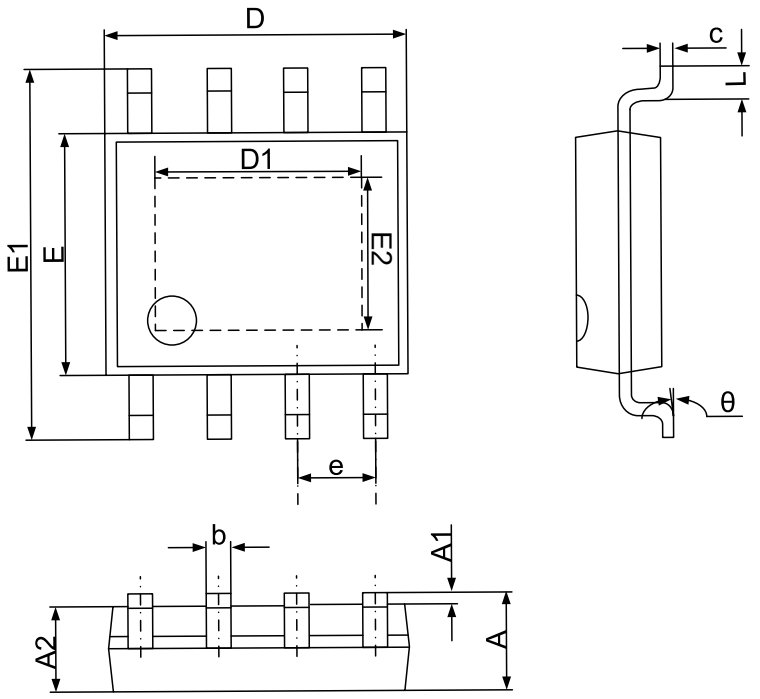
12 Package Dimension

SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

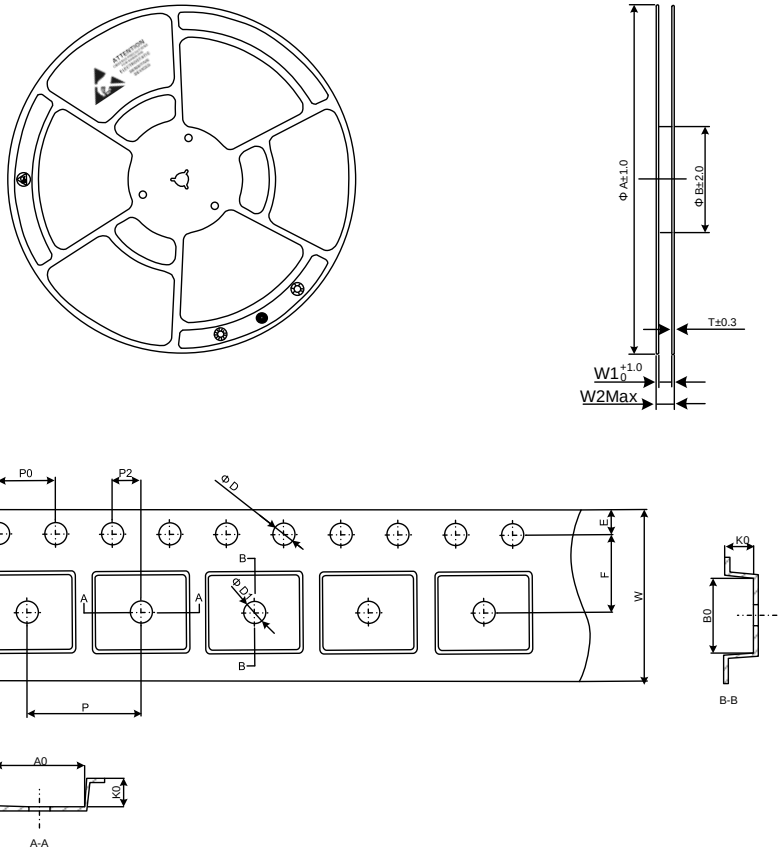
ESOP-8



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.650	-	-	0.065
A1	0.000	-	0.150	0.000	-	0.006
A2	1.300	-	1.500	0.051	-	0.059
b	0.330	-	0.470	0.013	-	0.019
c	0.200	-	0.240	0.008	-	0.009
D	4.800	-	5.000	0.189	-	0.197
D1	3.100 (REF)			0.122 (REF)		
E	3.800	-	4.000	0.150	-	0.157
E1	5.800	6.100	6.200	0.228	0.240	0.244
E2	2.210 (REF)			0.087 (REF)		
e	1.270 (BSC)			0.050 (BSC)		
L	0.500	-	0.800	0.020	-	0.031
θ	0°	-	8°	0°	-	8°

13 Tape and Reel Information

SOP-8



Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2 Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		

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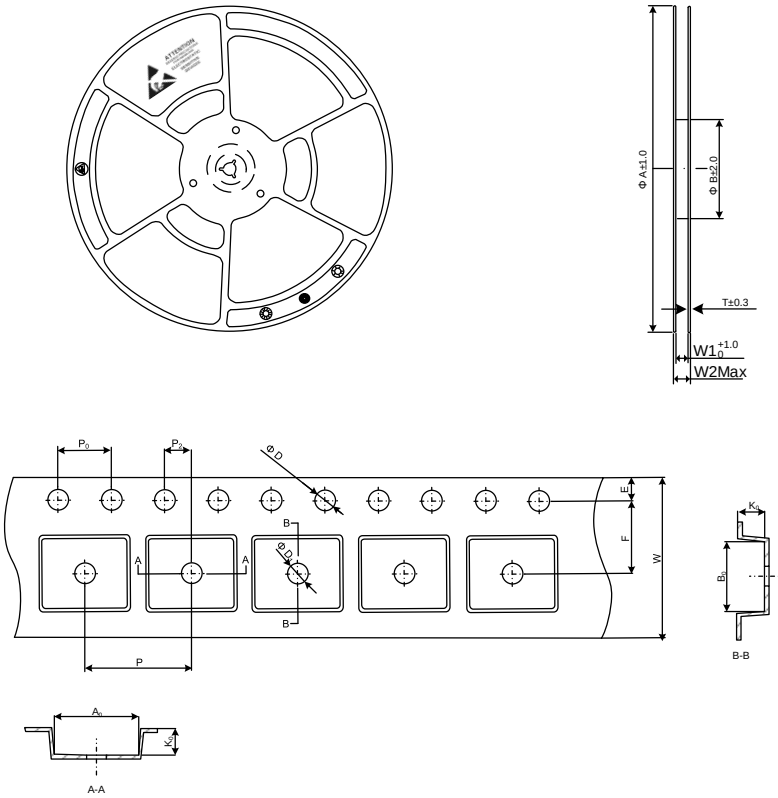

Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2 Max**	**T**
330	100	12.4	18.4	2.1

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P_2	2.00±0.10	A_0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B_0	5.30±0.10
D_1	1.55±0.05	K_0	1.90±0.10
P_0	4.00±0.10		

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