


# B650E AORUS PRO X USB4

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54	U32G2_REDRIIVER

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COVER SHEET			
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**Model Name: B650E AORUS PRO X USB4**

## Component value change history


**Version: 1.0**

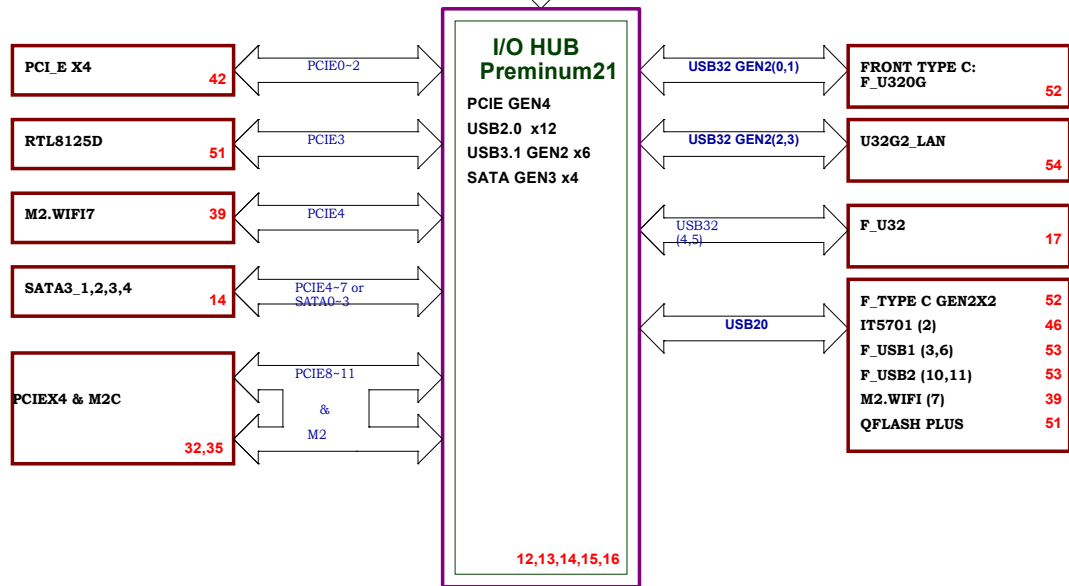
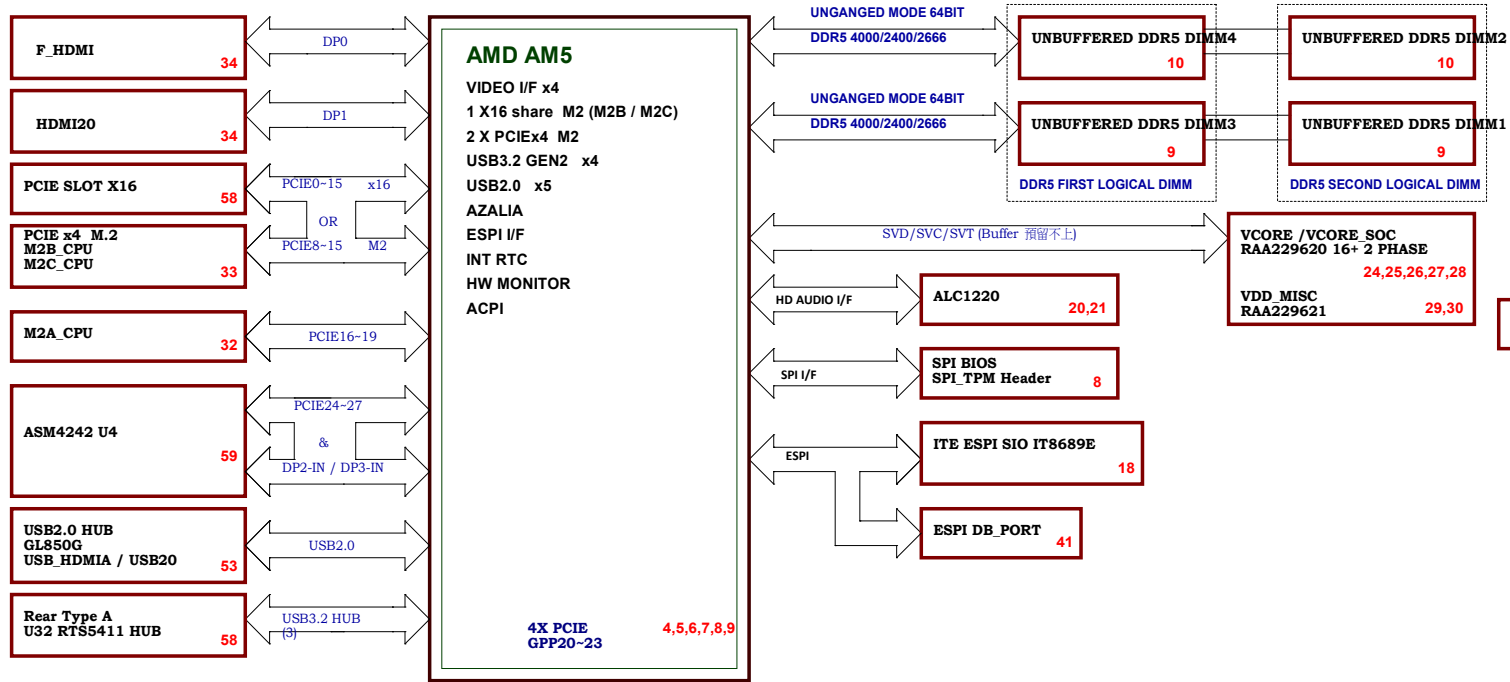
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Date	Change Item	Reason
2022.08.25	F--BOM Release . PCB: 1.0	1. BOM : 10D 2. Location : WIFI_COVER "11KWP-000001-31R"
2022.08.25	F--BOM Release . PCB: 1.0	1. BOM : 10E 2. Location : RAR2 上件 3. Location : RQ2 NA (DATA BUFFER 單向,會有問題)
2022.09.15	F--BOM Release . PCB: 1.0	1. BOM : 10F 2. Location : UAU3D1,UAU3D2,UAU3D4,UAU3D5 修改用料為 "10DE2-353124-10R" 3. Location : AR26 上件pw_sw ac第一次開機"42"燈會滅問題
2022.10.14	F--BOM Release . PCB: 1.0	1. BOM : 10F 2. ECN , 移除10HP4-112516-40R用料 CHIP LAN I225V B3 INTEL 搭配10HP4-112516-40R有LAN ID無法燒錄問題,移除10HP4-112516-40R,修改為10HP4-112516-50R用料
2023.01.04	A-BOM Release . PCB: 1.0	BOM : 10G PCB1.0 (ABOM) 1. Location : MAC11 100p to 470p (for CHOKE noise issue) 2. Location : MCUR100 / MCUR119 NA 3. Location : MCUR155 / MCUR157 change to 300/6/1 4. PWM 料號 10TA1-629620-02R -> 10TA1-629620-04R (delay 1ms)
2023.03.27	F-BOM Release . PCB: 1.0 9MB65EMSR-00-10H	BOM : 10H PCB1.0 (FBOM) 1. Location : DA1_DR3/DA2_DR3/DB1_DR3/DB2_DR3/DC1_DR3/DC2_DR3/DD2_DR3/DD1_DR3/DE1_DR3/DE2_DR3/DF1_DR3/DF2_DR3/DG1_DR3/DG2_DR3/DH1_DR3/DH2_DR3 2.2ohm to 4.7ohm 2.MCUR155,MCUR157 300ohm change to 200ohm
2023.03.28	A-BOM Release . PCB: 1.01 9MB65EMSR-00-10K	1. SPS PIN 3 add 0.1u by on top layer & gen to pin2 2. SPS BOOT PIN 4.7ohm TO 2.2ohm
2023.05.11	P-BOM Release . PCB: 1.01 9MB65EMSR-00-10K	1. 轉P-BOM,試產50PCS
2023.05.29	ECN Release . PCB: 1.01 9MB65EMSR-00-10K	1. 0201 0.1u/X6S 新增替料(10CM9-3K1003-76R)
2023.07.14	A-BOM Release . PCB: 1.01 9MB65EMSR-00-10L	1. RTS5411T -> RTS5411S(FW更新) 2. JYS13008 -10R to -11R RQ1 NA, RAR1 0 ohm上件 3. DB_PORT Add 11DL1-020070-73R(耐高溫)
2023.09.21	F-BOM Release . PCB: 1.01 9MB65EMSR-00-10M	AM5 model PHX CPU hang with Hardware Reset issue 1. FFR9 REMOVE 2. Mother board ID : OR14 change to OR26 3. FAN NCT3947-->NCT3948 4. F*R2 & F*C1 NA
2023.12.25	F-BOM Release . PCB: 1.01 9MB65EMSR-00-10N	Location : PEC1 330u to 470u
2023.12.25	E-BOM Release . PCB: 0.2	1. U4_RST- & U4_WAKE 移至CPU端(P.7) 2. M2A 與 ASM4242 位置對調
2024.04.15	P-BOM Release . PCB: 1.0	1. Location : ECDR6 要上件, OFLASH PLUS FUNCTION 2. 8851G_INT 移至gpio11 (AD5) 3. VDDIO_MEM add WBC192 POSCAP 4. DG_U1VIN 改VCC 5. A_Q5 方向 6. LED_B_33 change to 470/8P4R/6 7. MA_L10.22->0.15uH (MA_OR18 : 75K-> 69.8K)

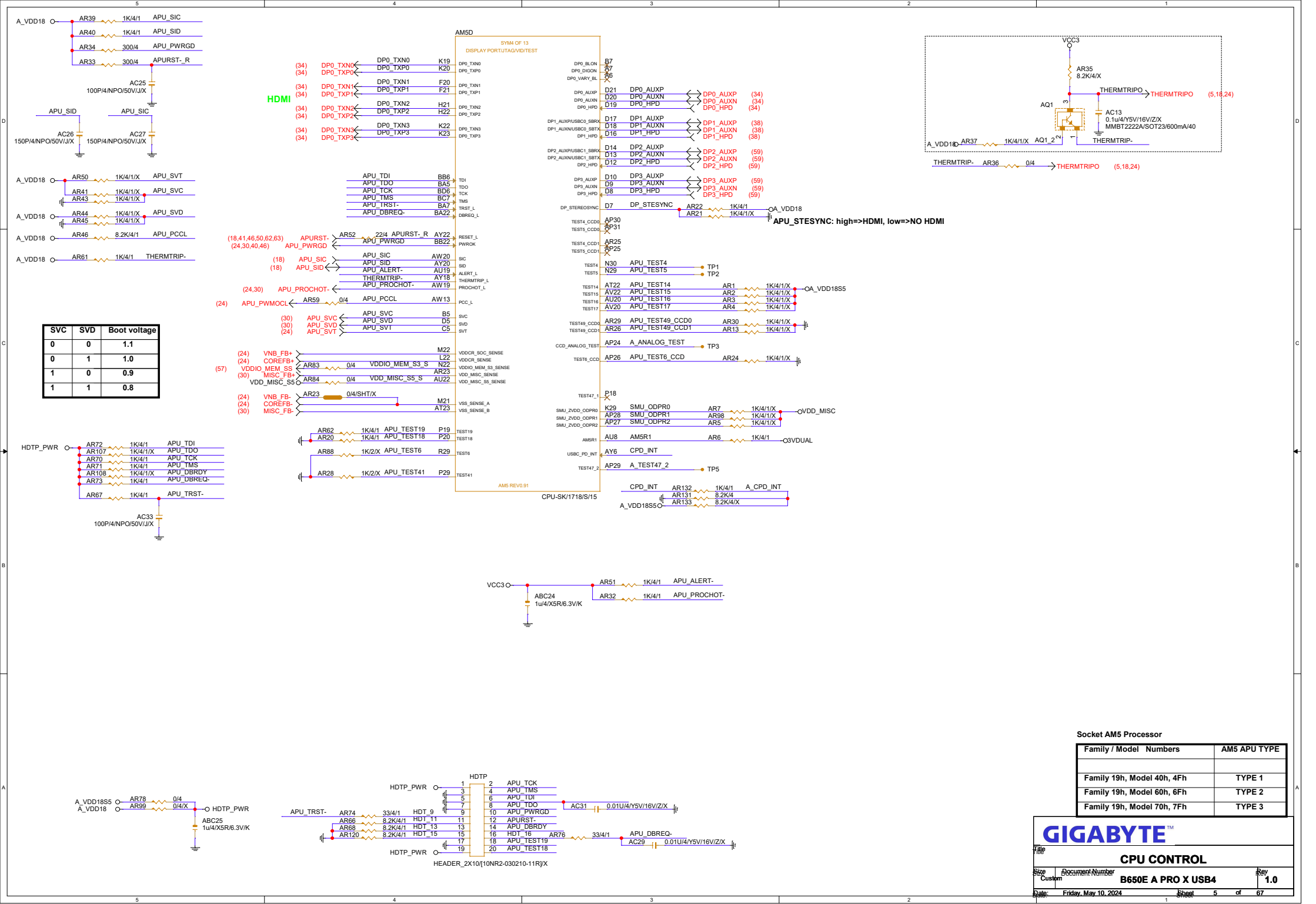
### Circuit or PCB layout change for next version

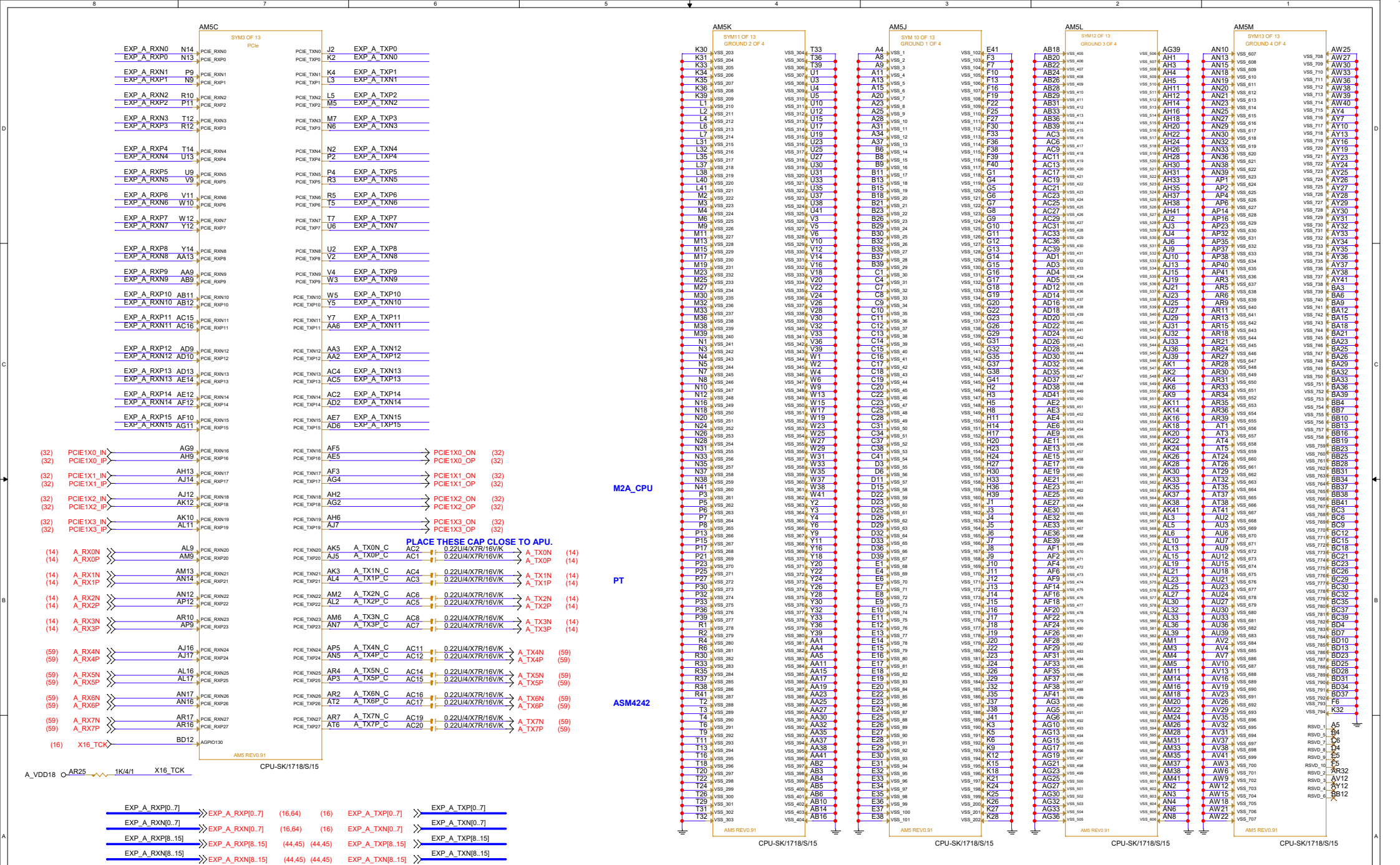
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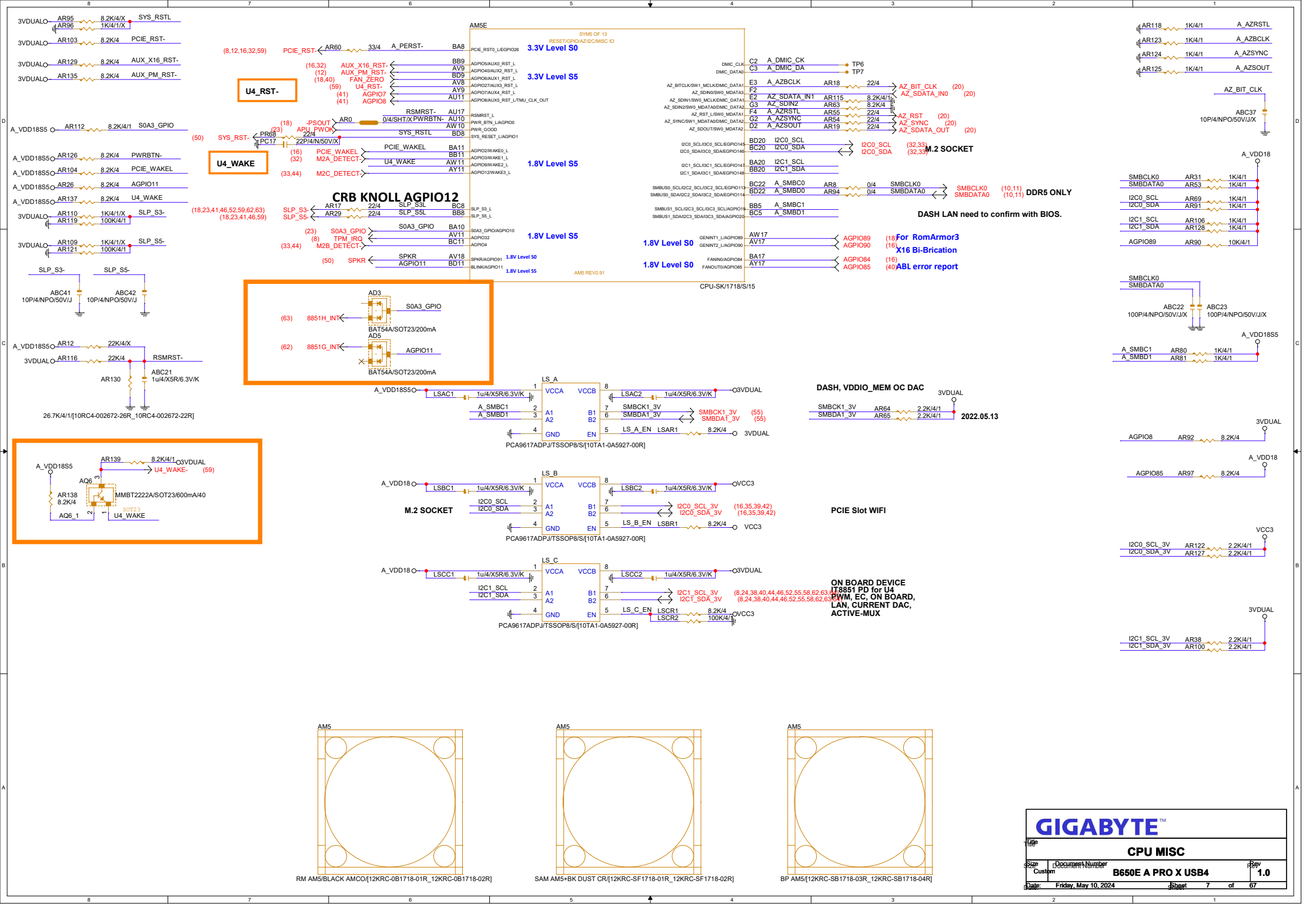
				
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<b>BOM &amp; PCB HISTORY</b>				
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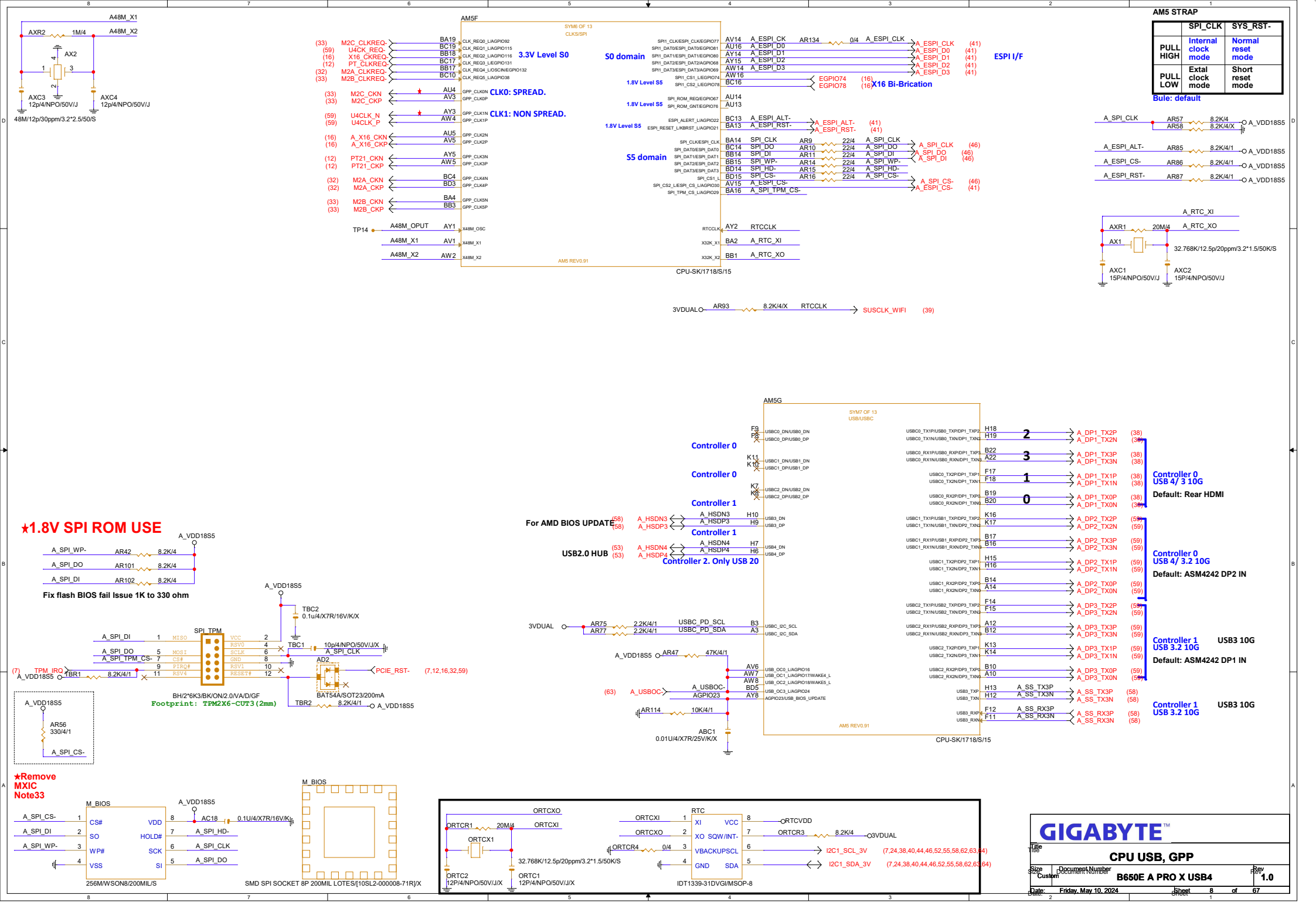


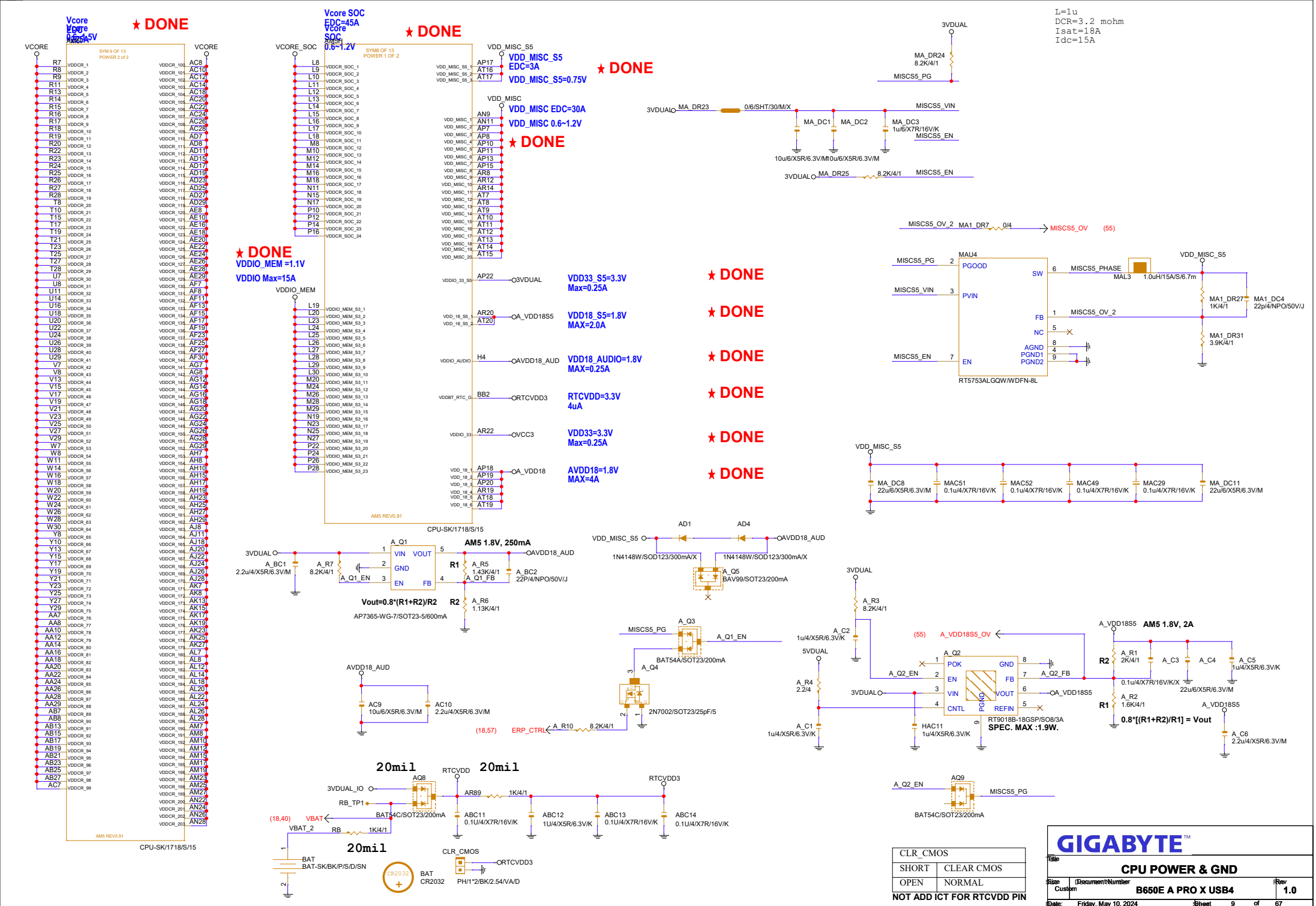




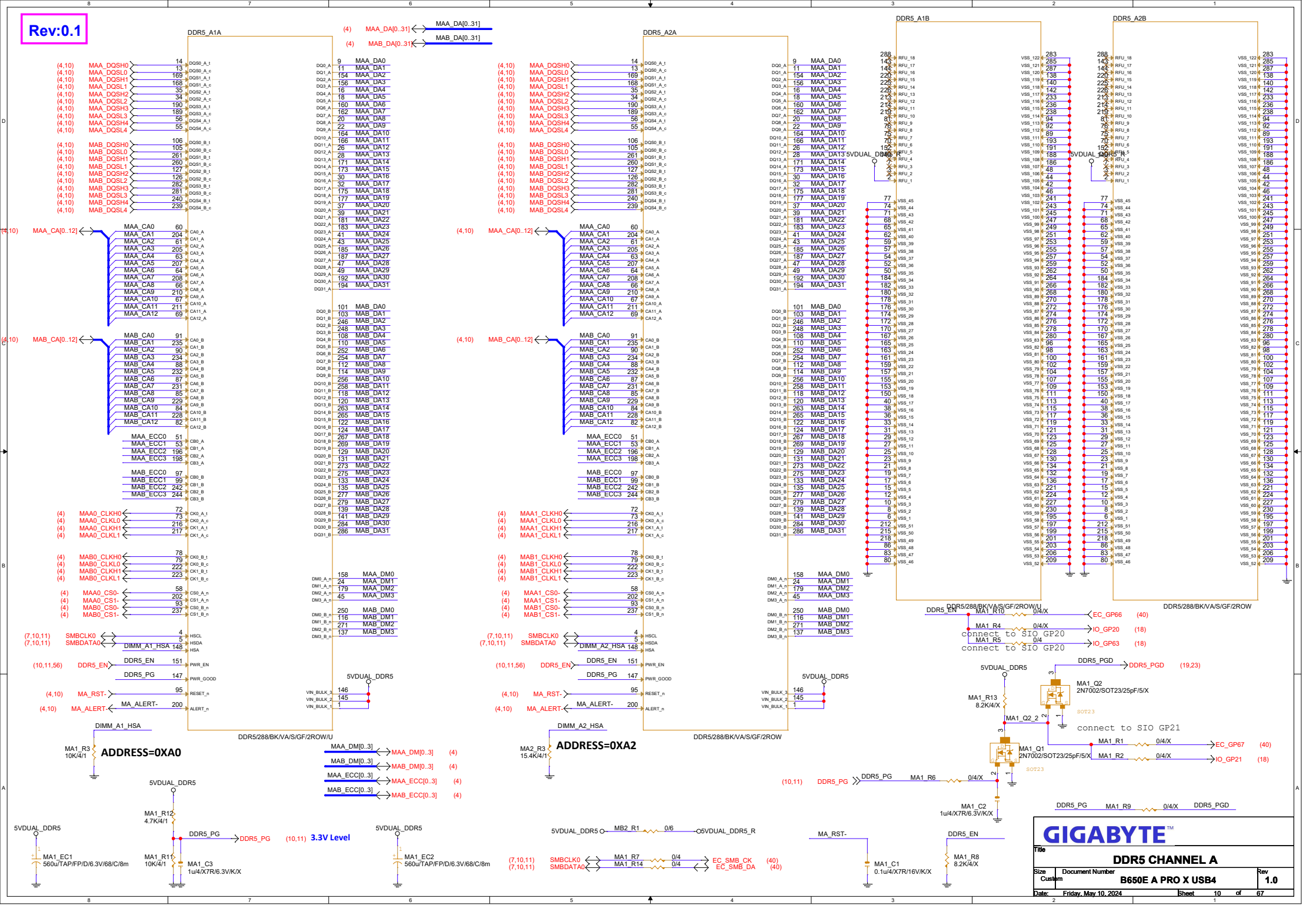


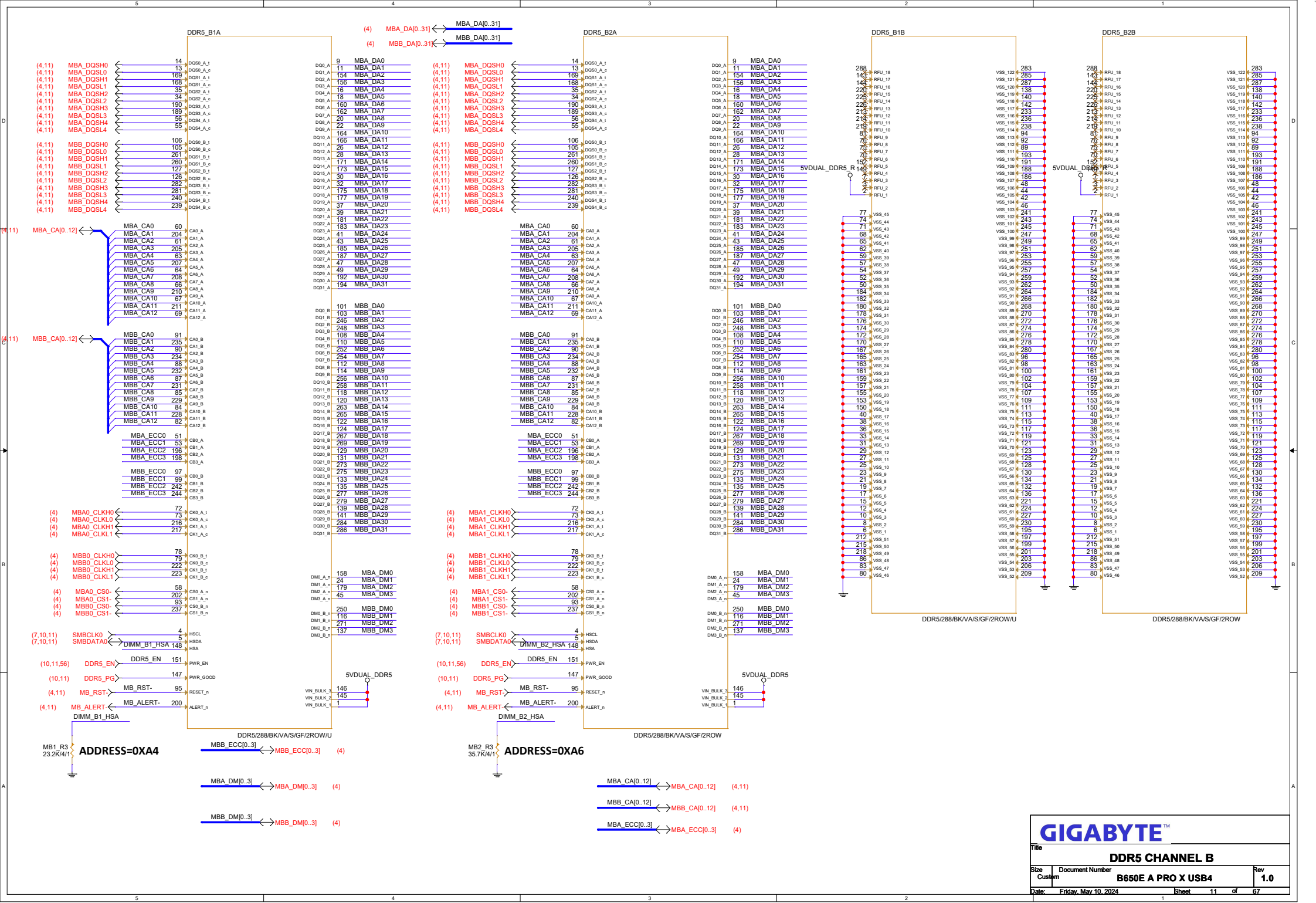




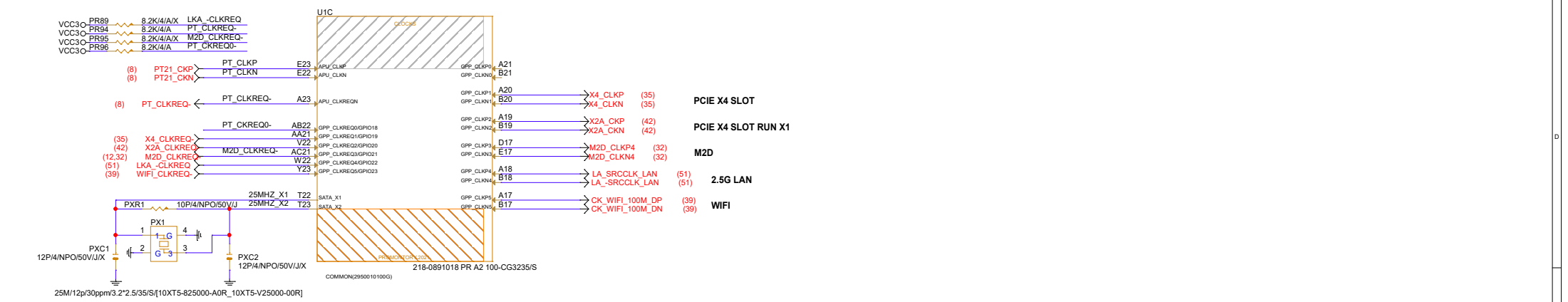


**Rev:0.1**

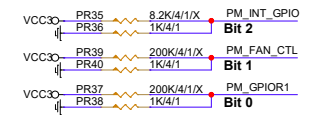




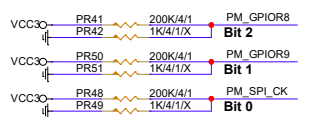
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Bit 2	Bit 1	Bit 0	GPP Group 0 LANE 0 1 2 3
1	1	1	X4
0	1	1	X2 --- X2 ---
0	0	1	X2 --- X1 X1
0	1	0	X1 X1 X2 ---
0	0	0	X1 X1 X1 X1
Others: Reserved			



Bit 2	Bit 1	Bit 0	GPP Group 1 LANE 4 5 6 7
1	1	1	X4
0	1	1	X2 --- X2 ---
0	0	1	X2 --- X1 X1
0	1	0	X1 X1 X2 ---
0	0	0	X1 X1 X1 X1
Others: Reserved			



Bit 2	Bit 1	Bit 0	GPP Group 2 LANE 8 9 10 11
1	1	1	X4
0	1	1	X2 --- X2 ---
0	0	1	X2 --- X1 X1
0	1	0	X1 X1 X2 ---
0	0	0	X1 X1 X1 X1
Others: Reserved			

Bit 1	Bit 0	Function
1	1	Debug signal group 3 output
1	0	Debug signal group 2 output
0	1	Debug signal group 1 output
0	0	Debug signal group 0 output

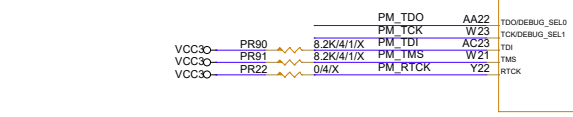
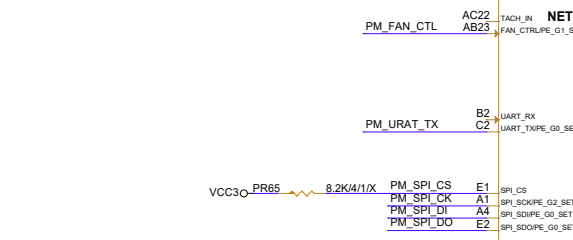
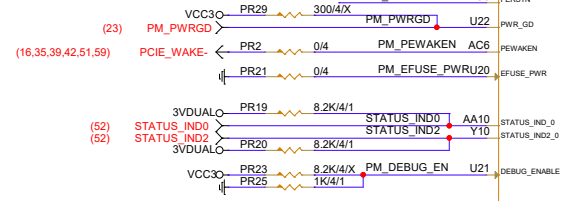
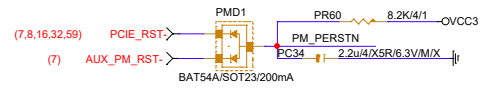
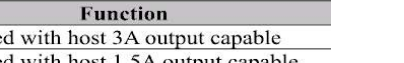
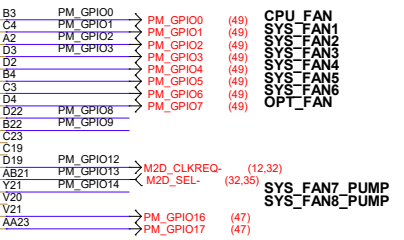
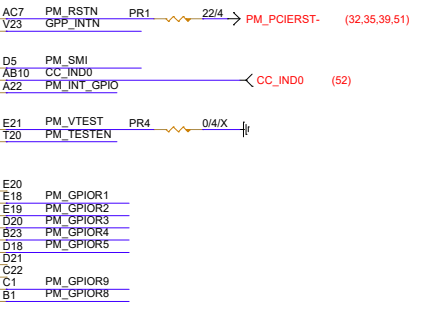
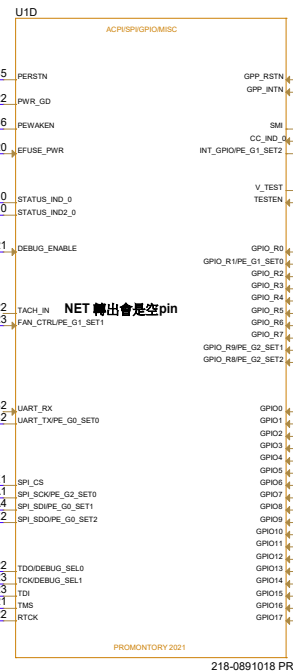


Table 34. Type-C Status Function Table

STATUS_IND_0	STATUS_IND2_0	Function
0	1	Device attached with host 3A output capable
1	0	Device attached with host 1.5A output capable
1	1	Device attached with host 900mA output capable
0	0	Device detached
CC_IND_0	Function	
0	Configuration channel on CC1	
1	Configuration channel on CC2	



ANS 12604179

**PM CLK/SPI/MISC**

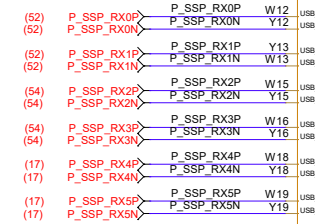
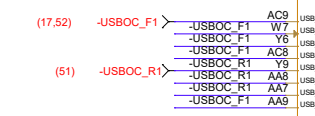
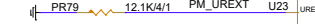
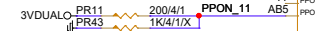
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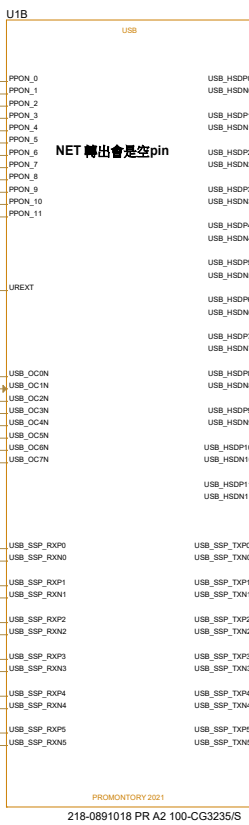
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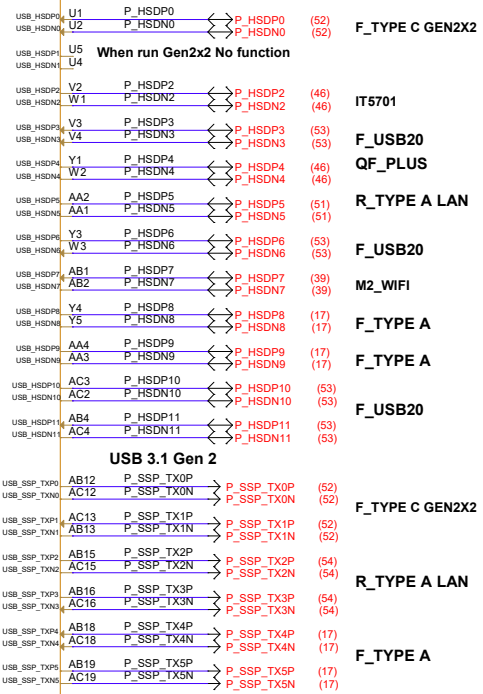
PPON\_11  
1: Type C indicator polarity is default. 0: Type C indicator polarity is inverse.



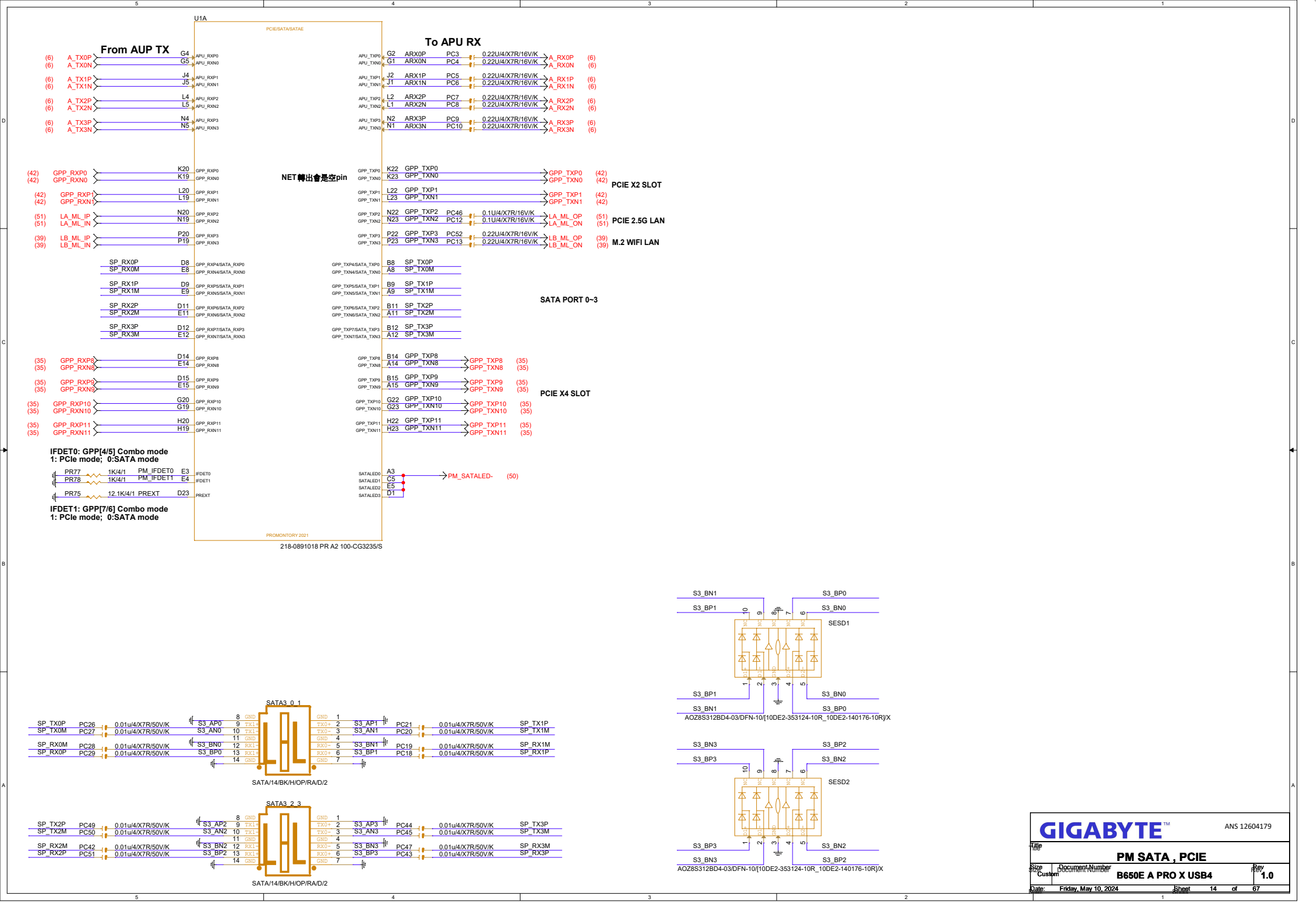
NET 轉出會是空pin

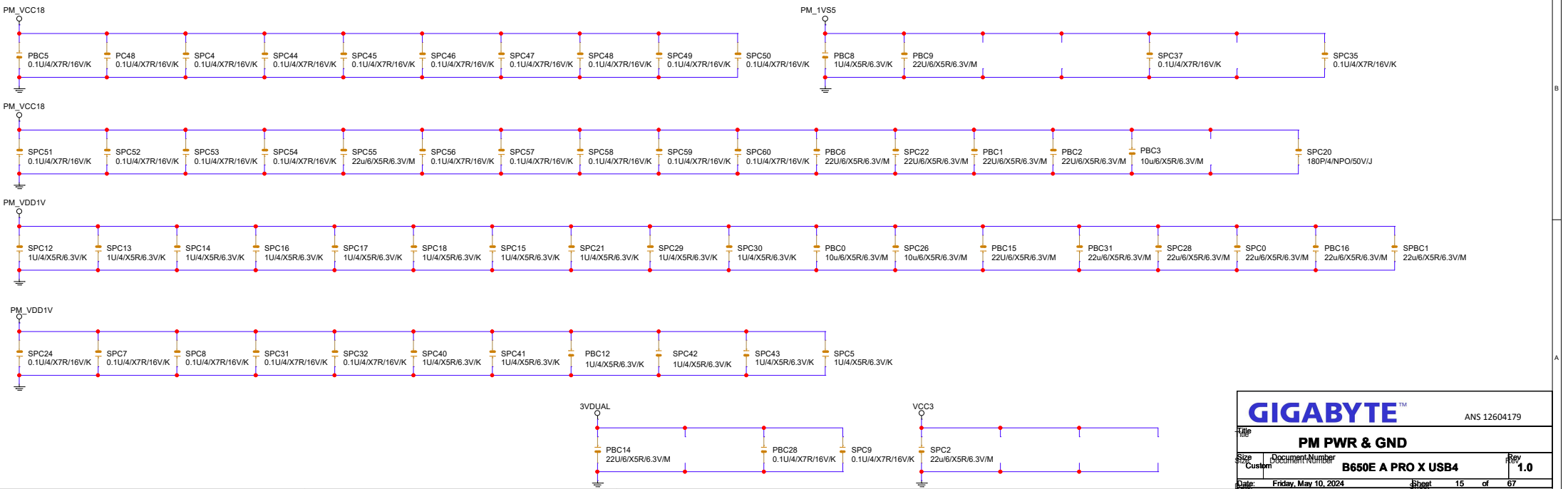
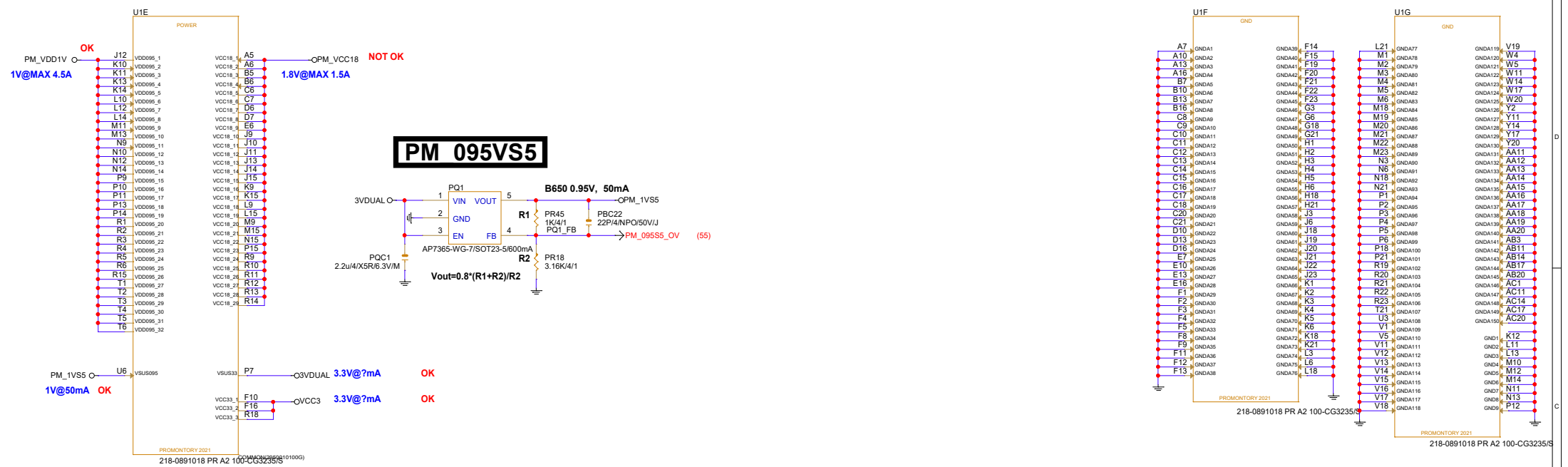


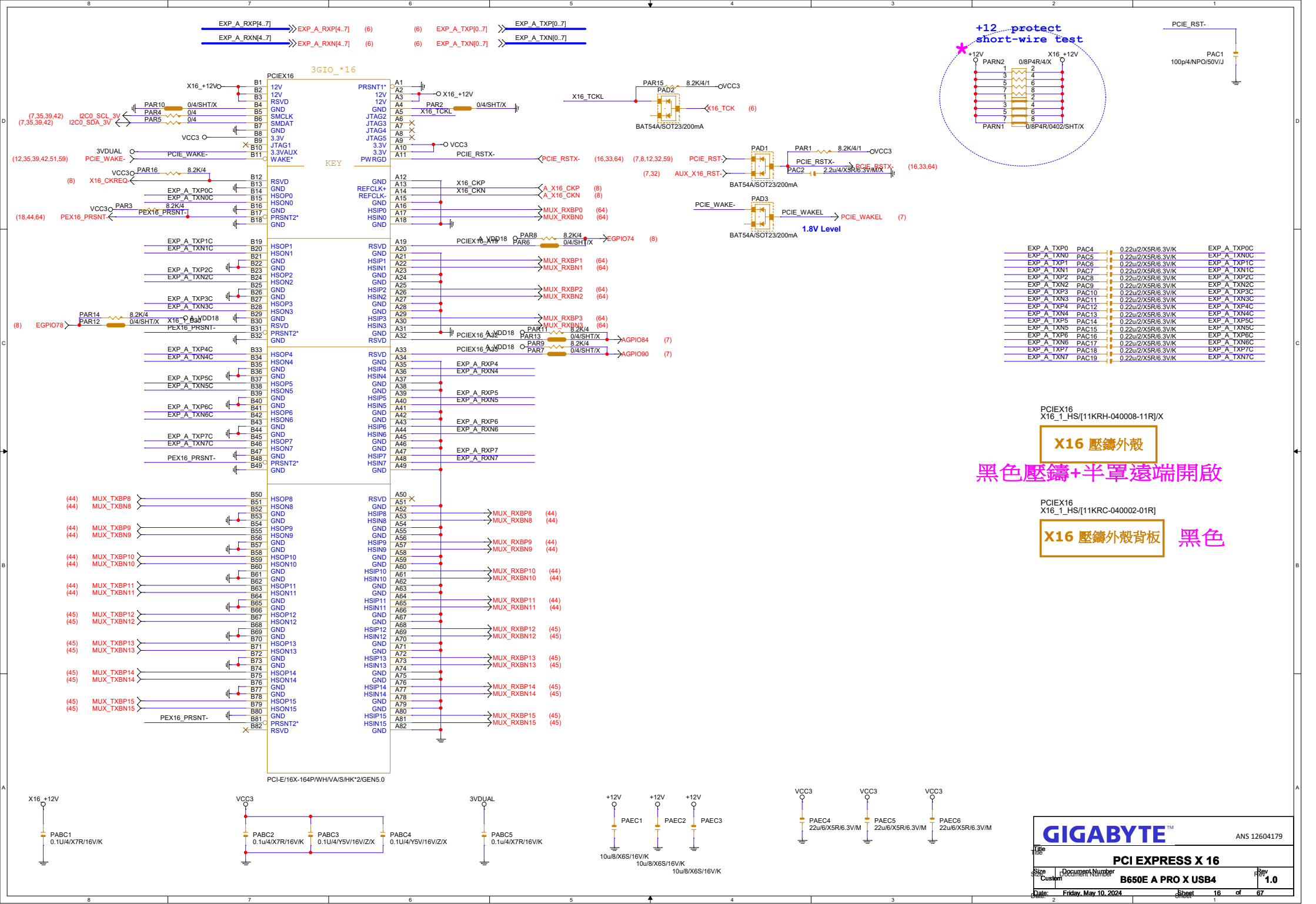
USB30G2	USB20	OC
0	0	OC0N
1	1	OC1N
2	4	OC2N
3	5	OC3N
4	8	OC4N
5	9	OC5N
	2	OC6N
	3	OC7N
	6	OC7N
	7	OC7N
	10	OC7N
	11	OC7N



PROMONTORY 2021  
218-0891018 PR A2 100-CG3235/S





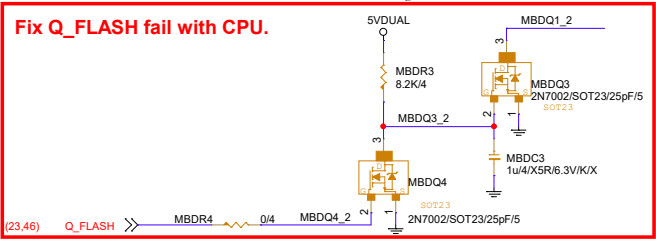
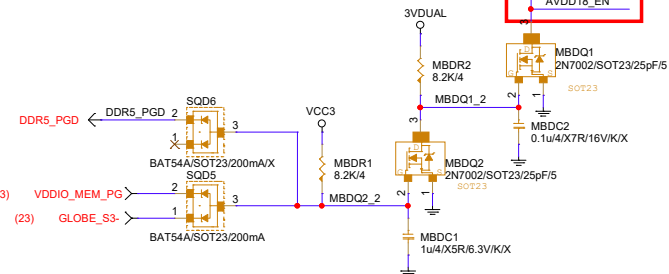






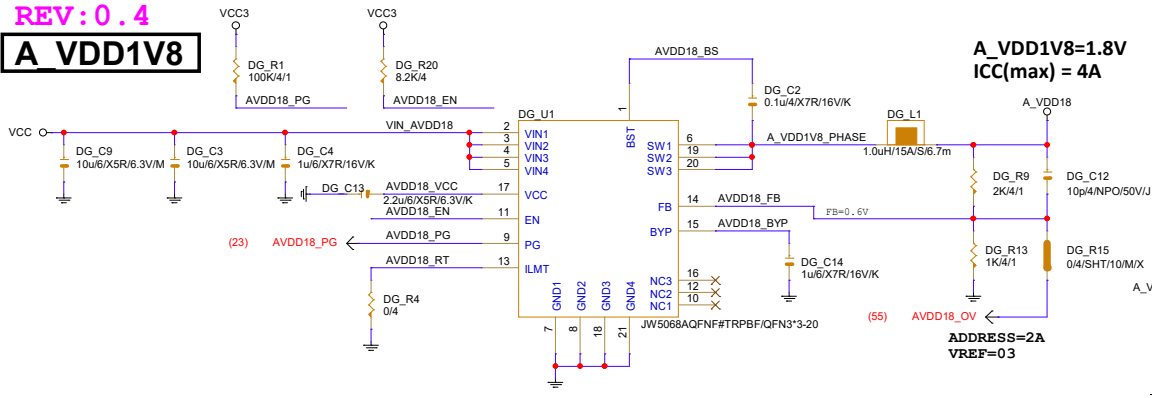
PWR\_SEQ

3VDUAL  
上件  
MB\_DR30  
8.2K/4/X  
AVDD18\_EN

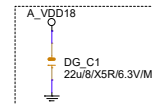


REV:0.4

A\_VDD1V8

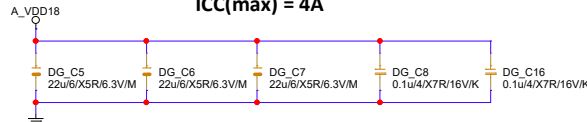


CHOKE與CAP料號可變



請放置CHOKE一出來位置.先預留.  
請自行確認ripple後再決定是否上件

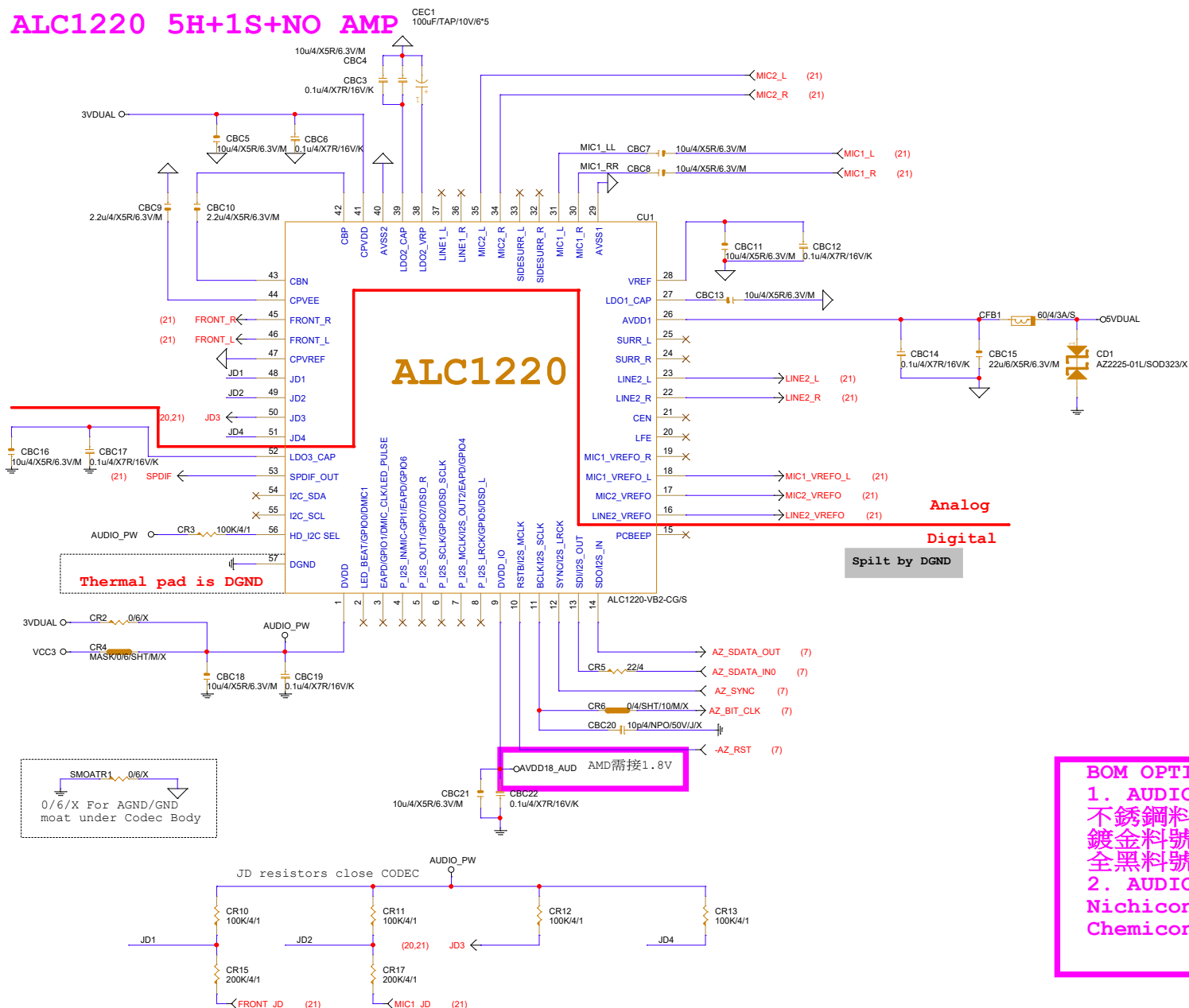
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ICC(max) = 4A



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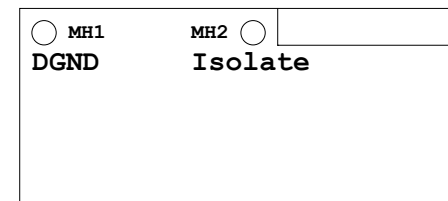
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# ALC1220 5H+1S+NO AMP



LAYOUT注意:螺絲孔下GND方式

1. MH1下DGND
2. MH2一律改為Isolate



LAYOUT注意:是否要加?

AGND切割線

音效區域印刷



BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號:11NR6-403025-A3R

鍍金料號:11NR6-403025-92R

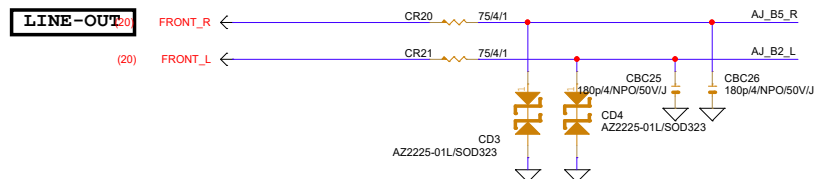
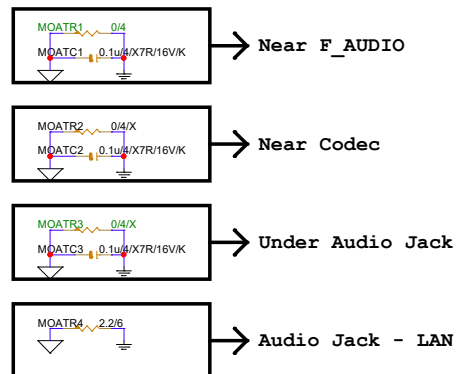
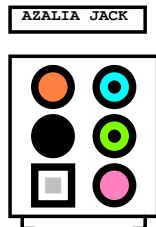
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2. AUDIO CAP

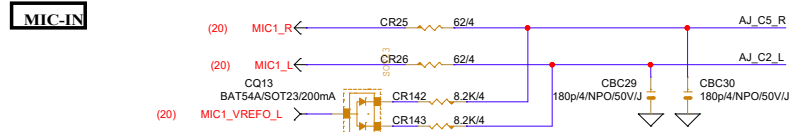
Nichicon MW音效電容 : 100u/TAP/6.3V/65

Chemicon音效電容 : 100uF/TAP/10V/6\*5

Rev 6.0

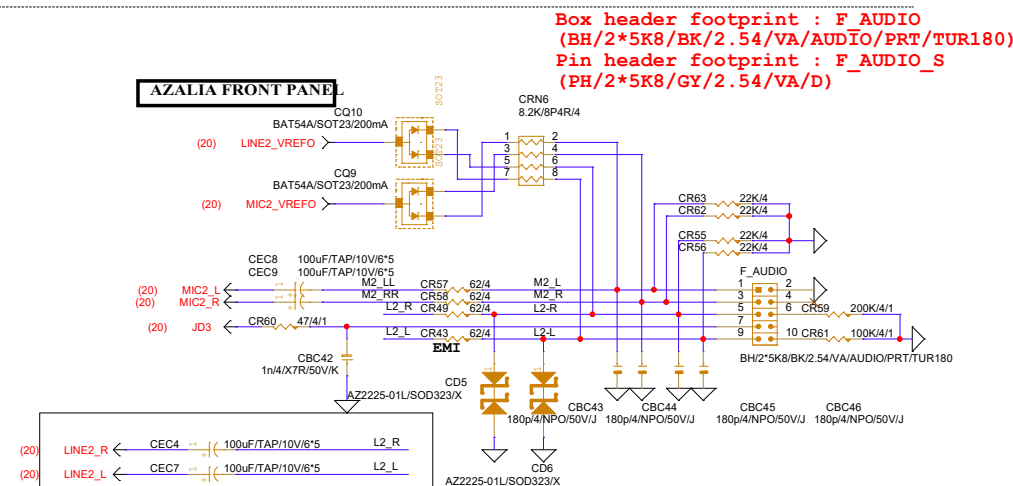
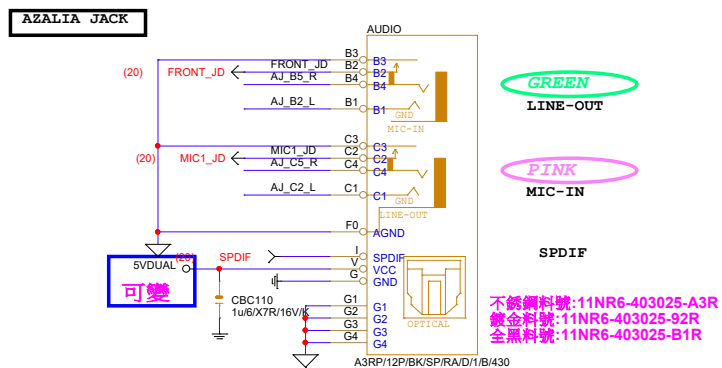


## LINE-IN



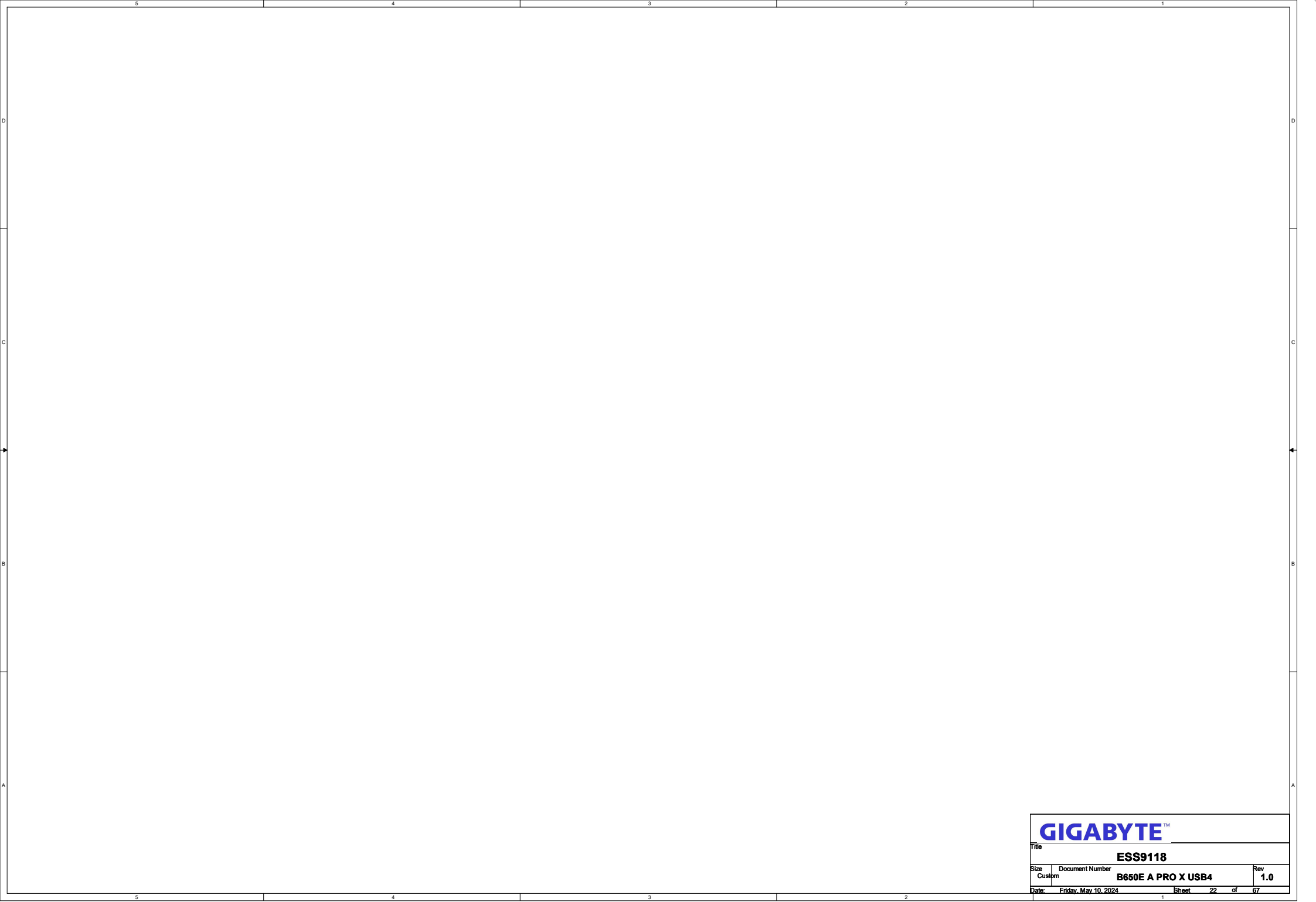
**SURROUND**

CEN/LFE



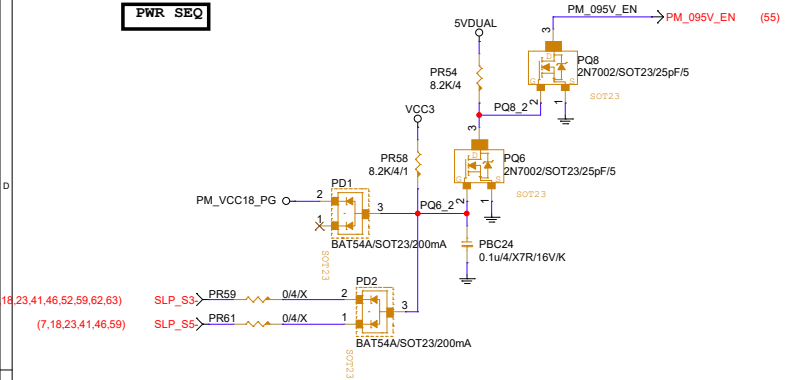
**GIGABYTE™**

Title			
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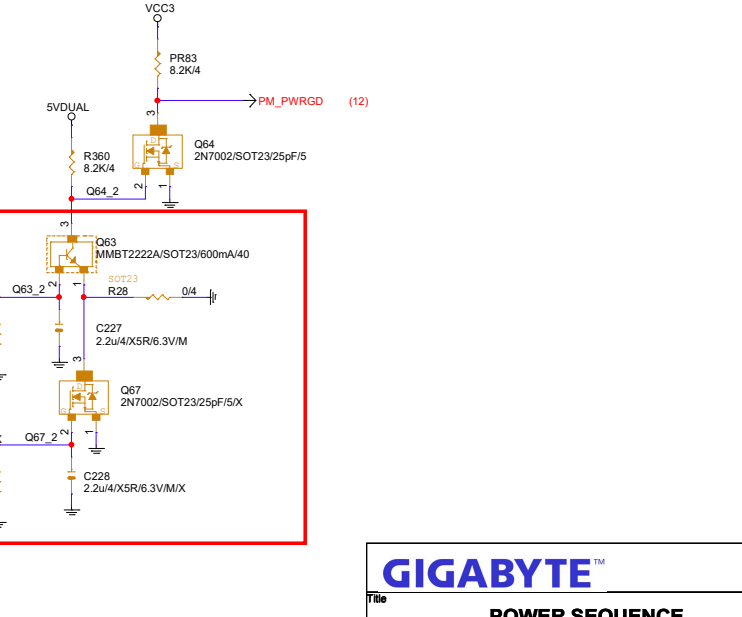
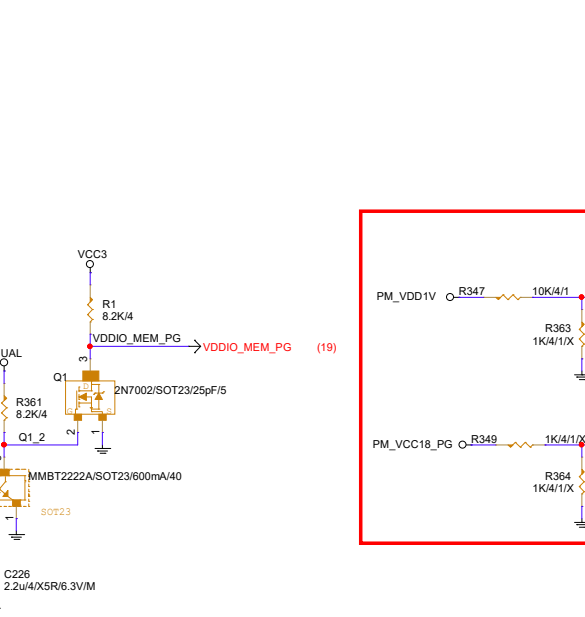
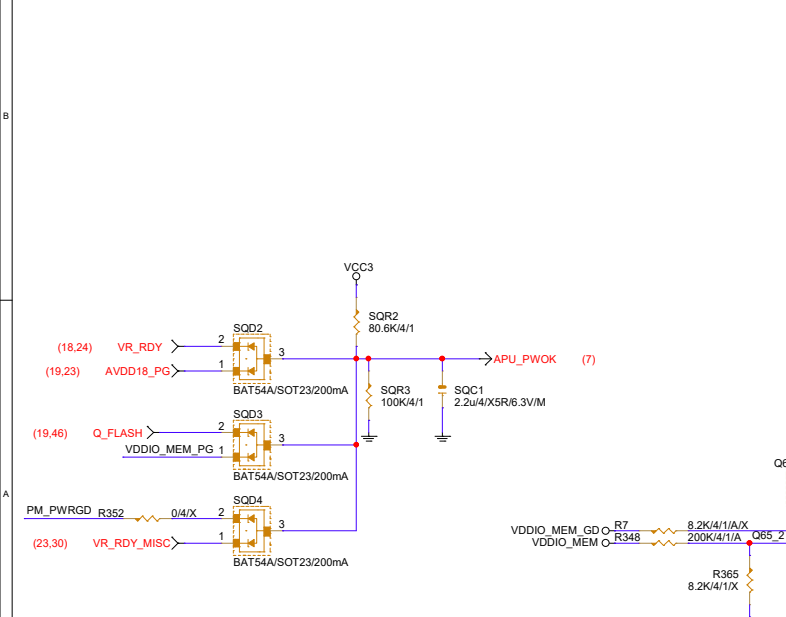
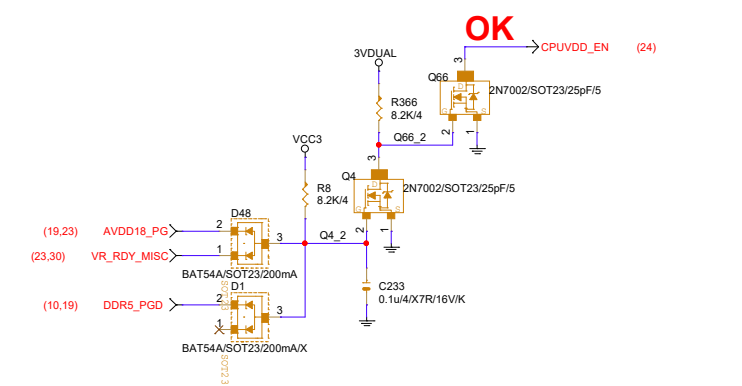
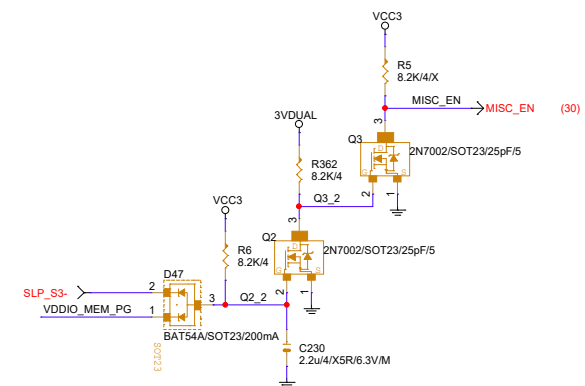
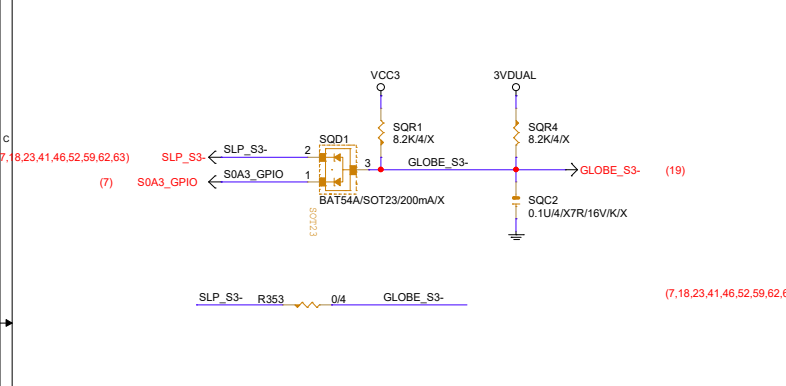
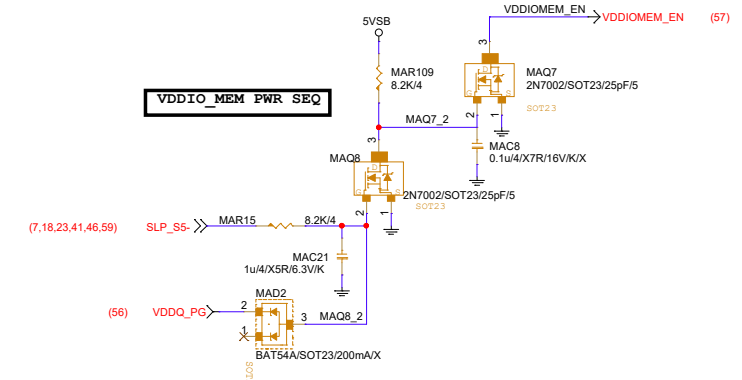


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PWR\_SEQ



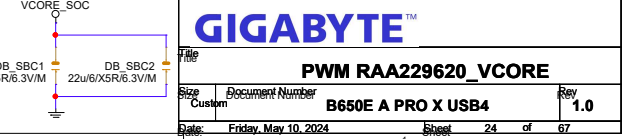
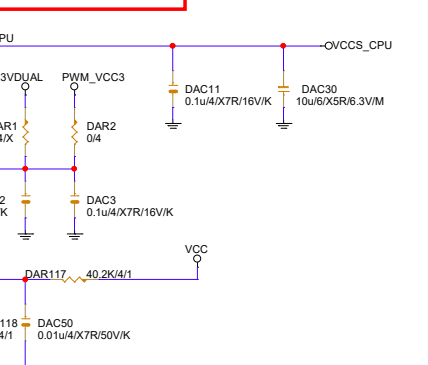
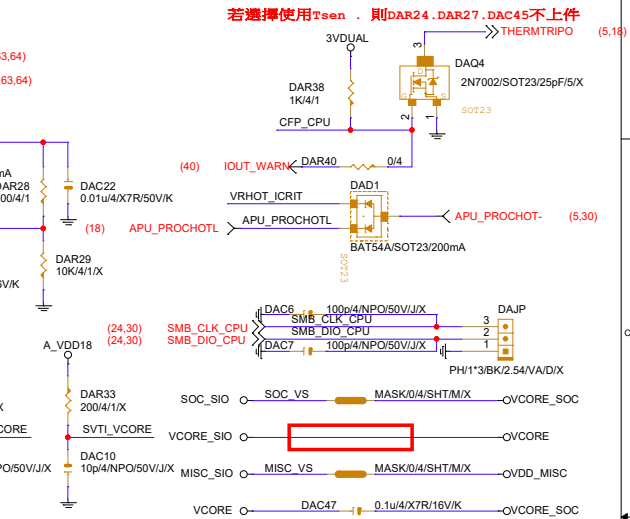
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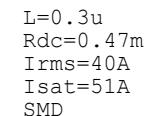
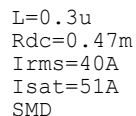
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使用TI and intersil DRMOS不上件

IRTN0\_SOC DAR69 953/4/1/X SOC\_CS0

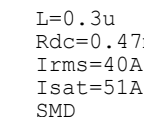
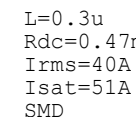
IRTN1\_SOC DAR70 953/4/1/X SOC\_CS1



VCORE PHASE1 1

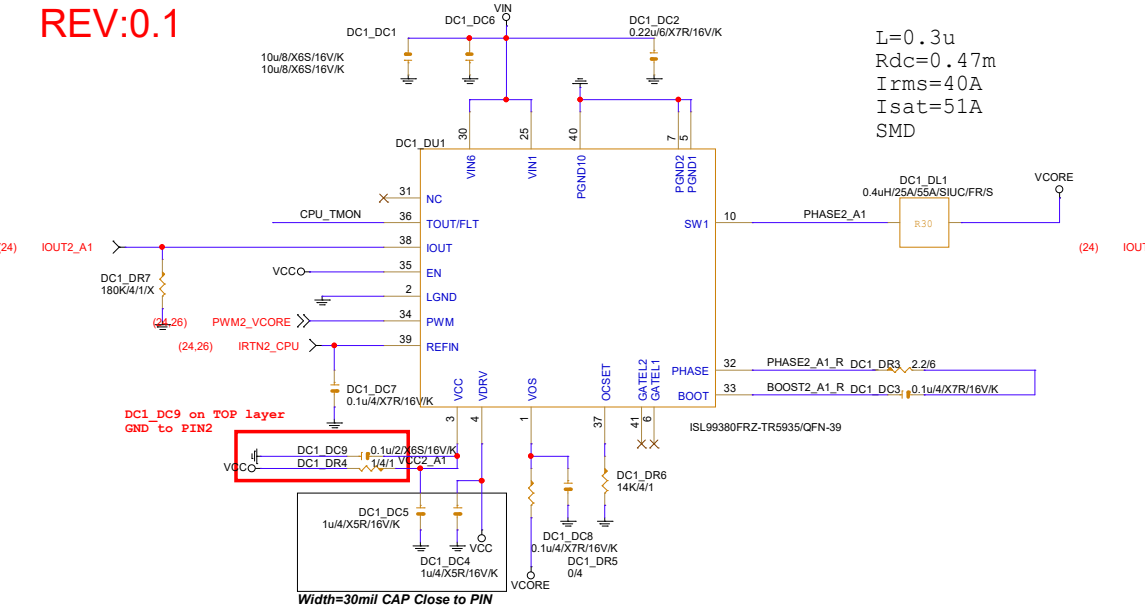


## VCORE PHASE2 1

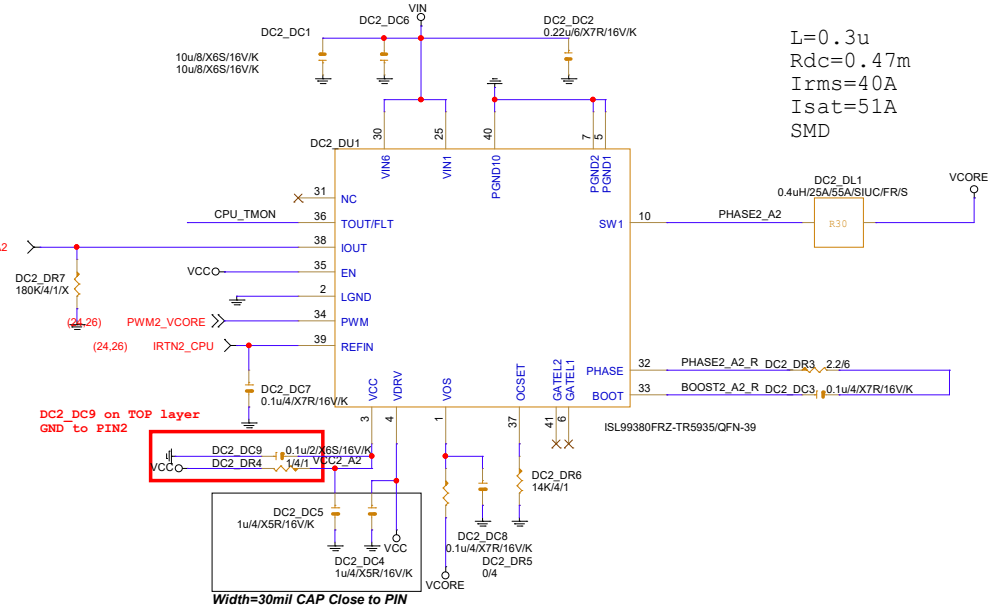


VCORE PHASE3\_1

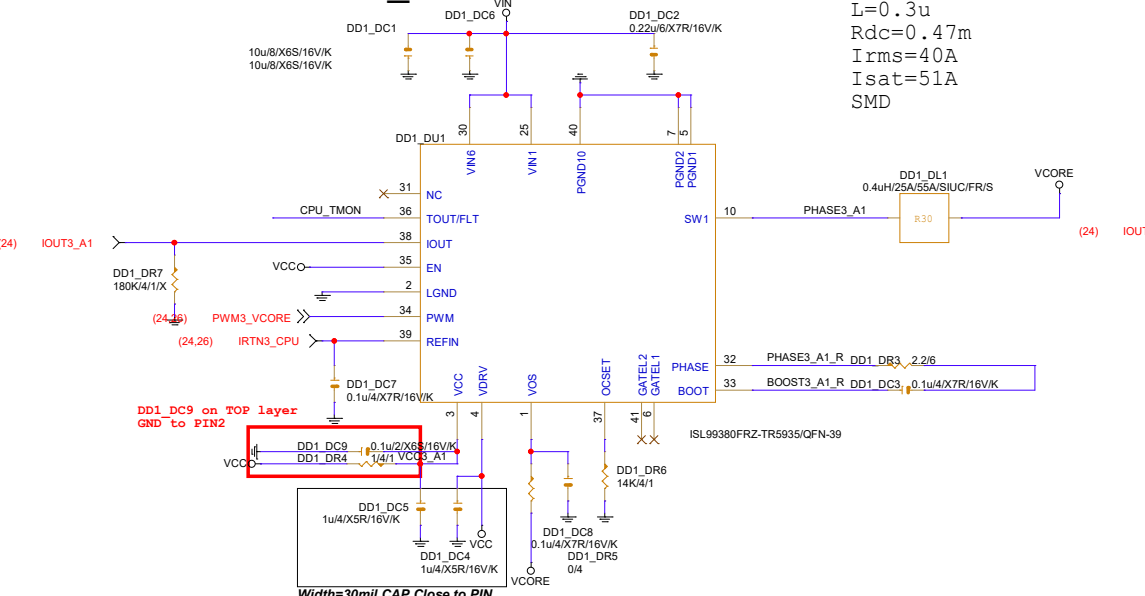
REV:0.1



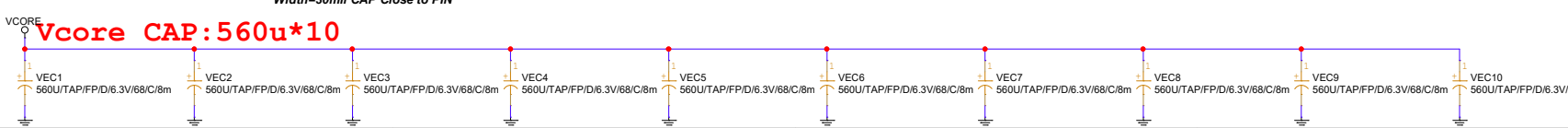
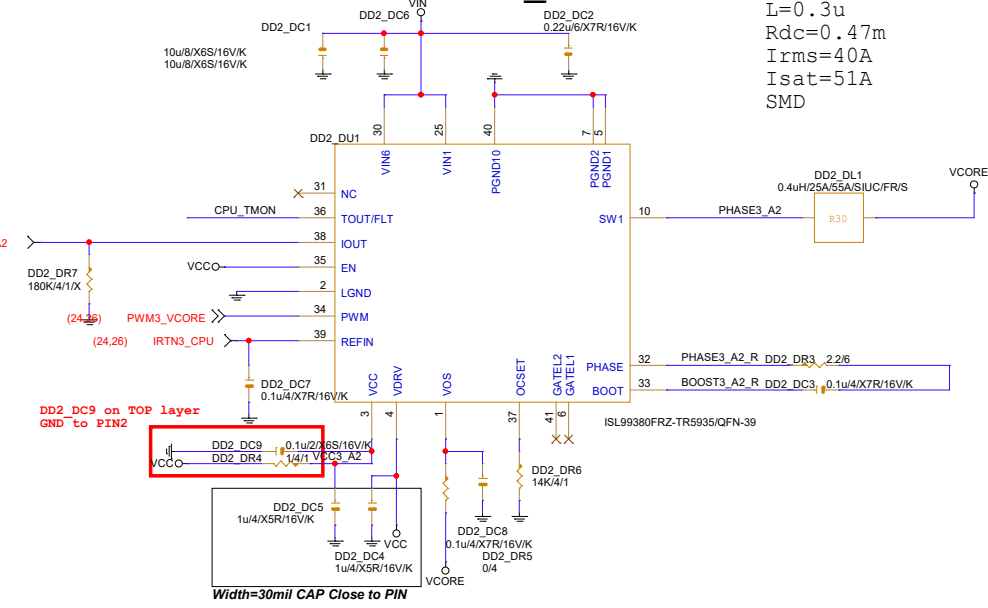
VCORE PHASE3\_2



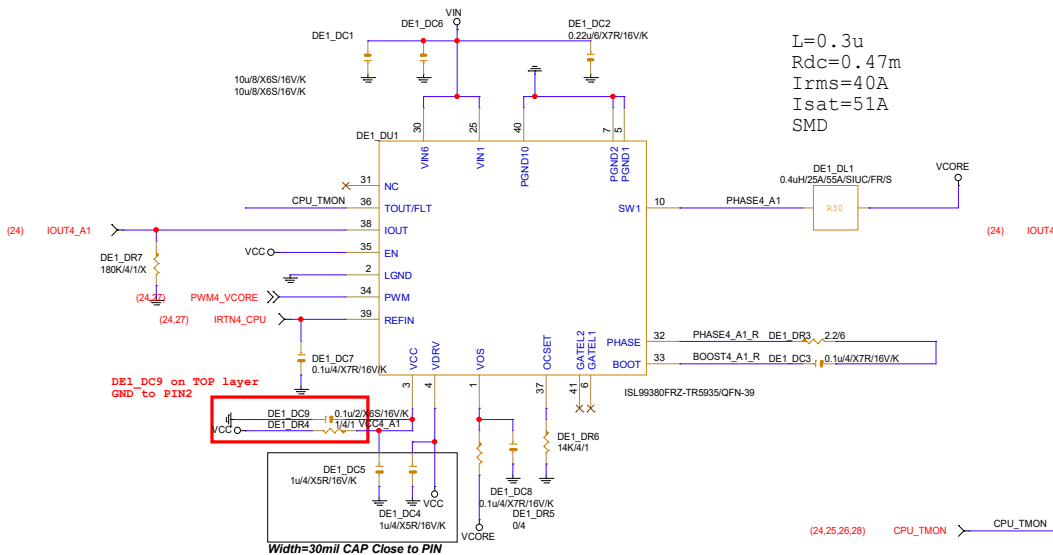
VCORE PHASE4\_1



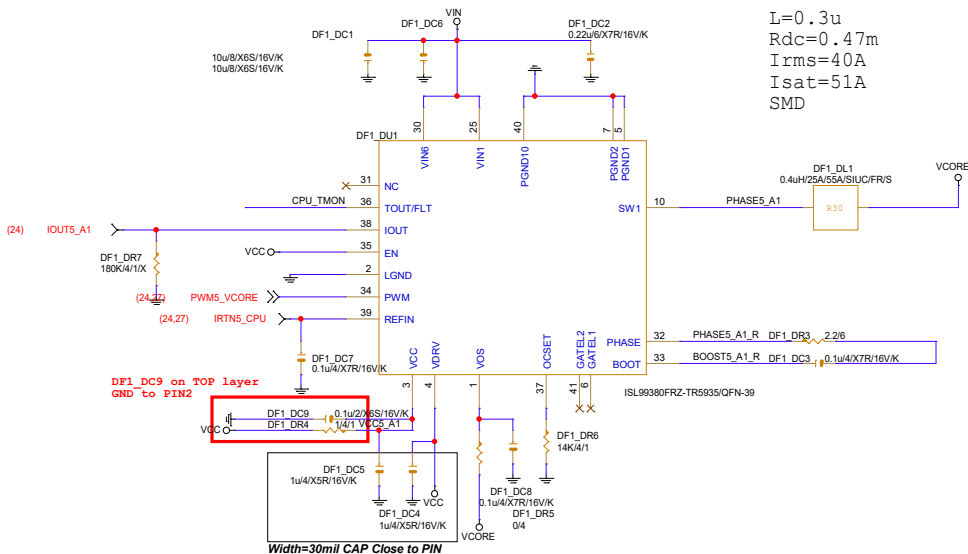
VCORE PHASE4\_2



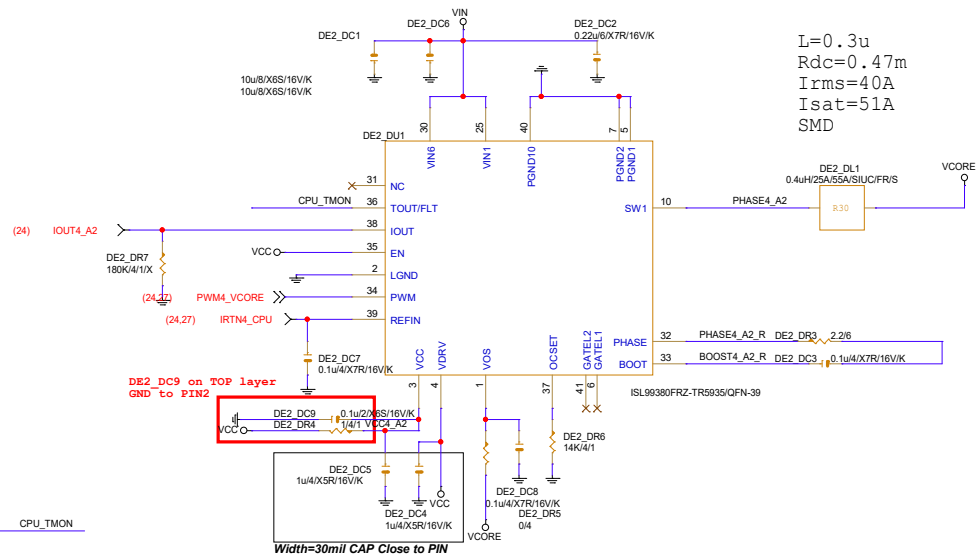
## VCORE PHASE 5\_1



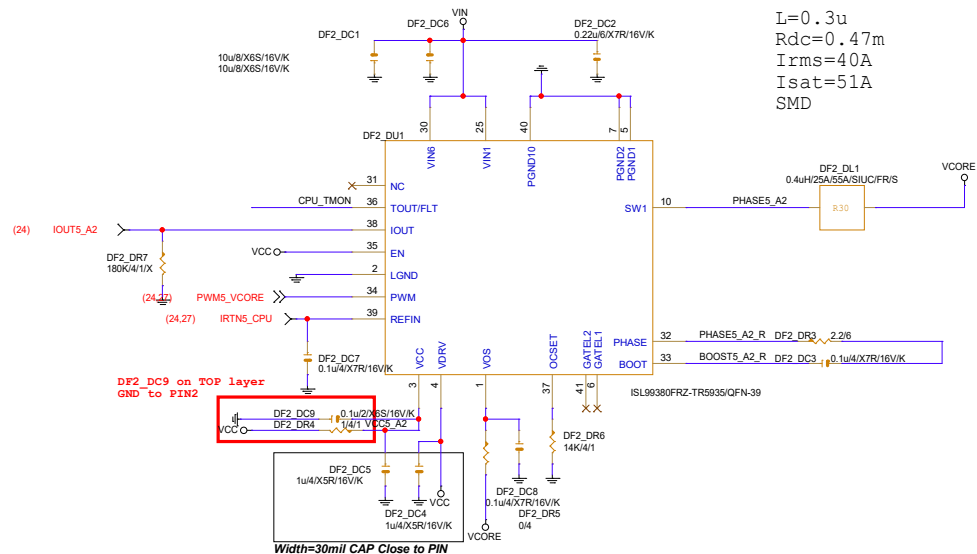
## VCORE PHASE 6\_1



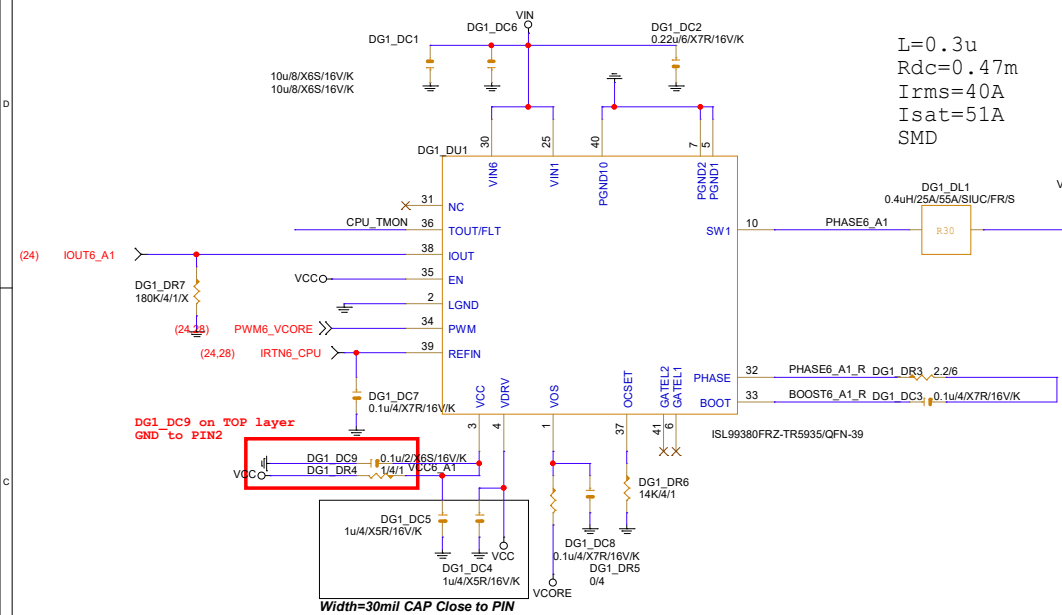
## VCORE PHASE 5\_2



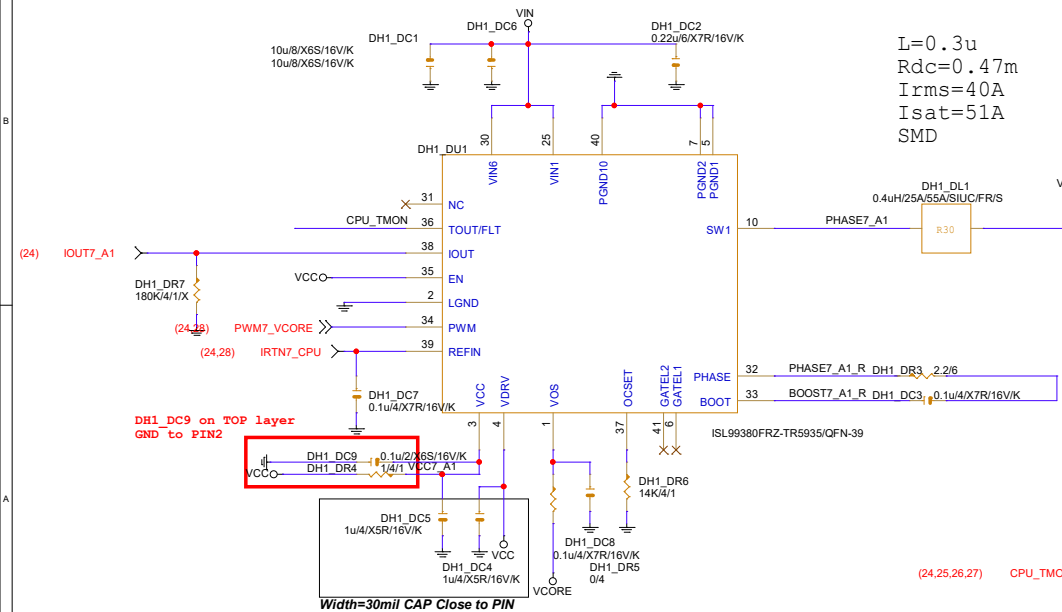
## VCORE PHASE 6\_2



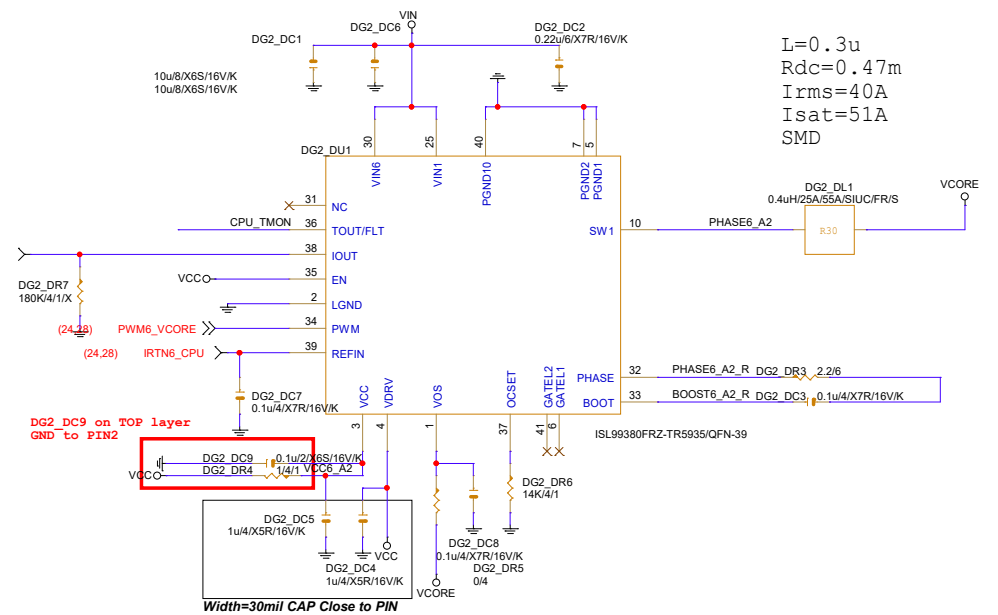
## VCORE PHASE 7\_1



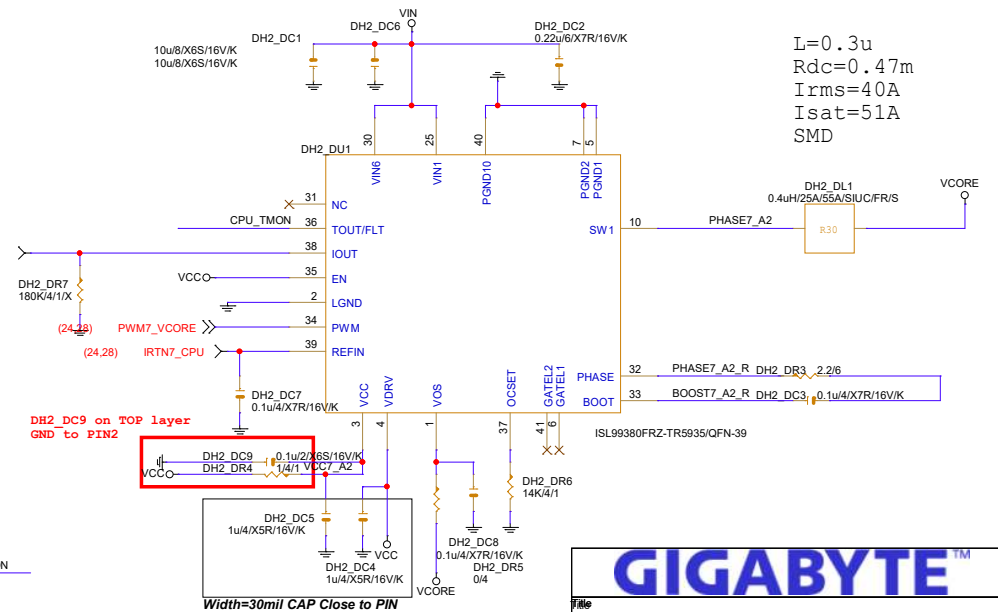
## VCORE PHASE 8\_1



## VCORE PHASE 7\_2



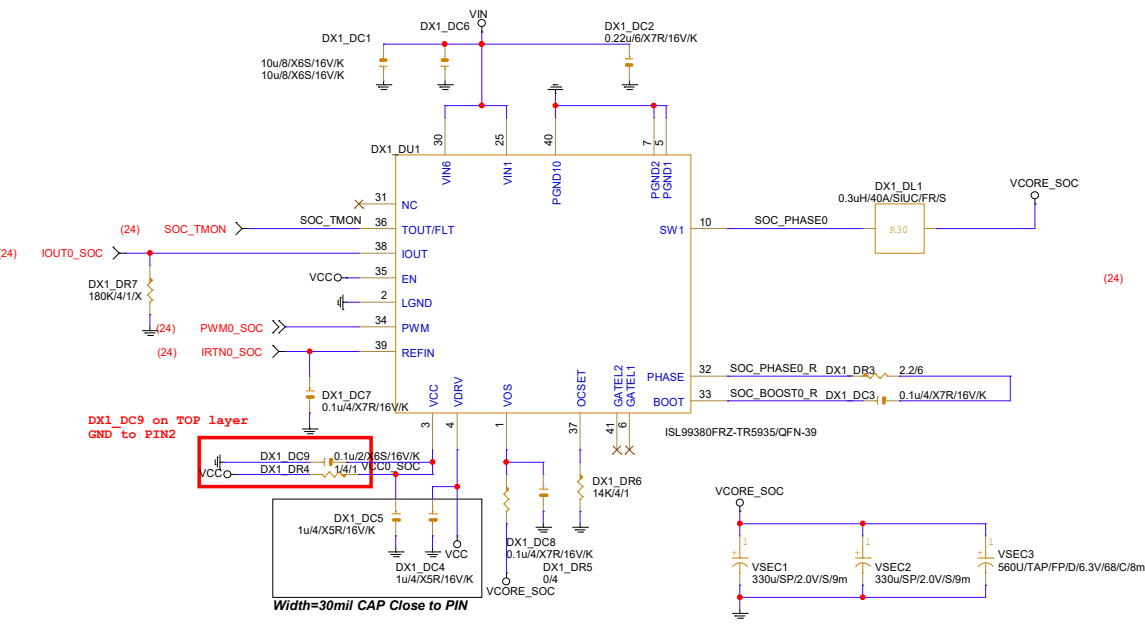
## VCORE PHASE 8\_2

**GIGABYTE™**

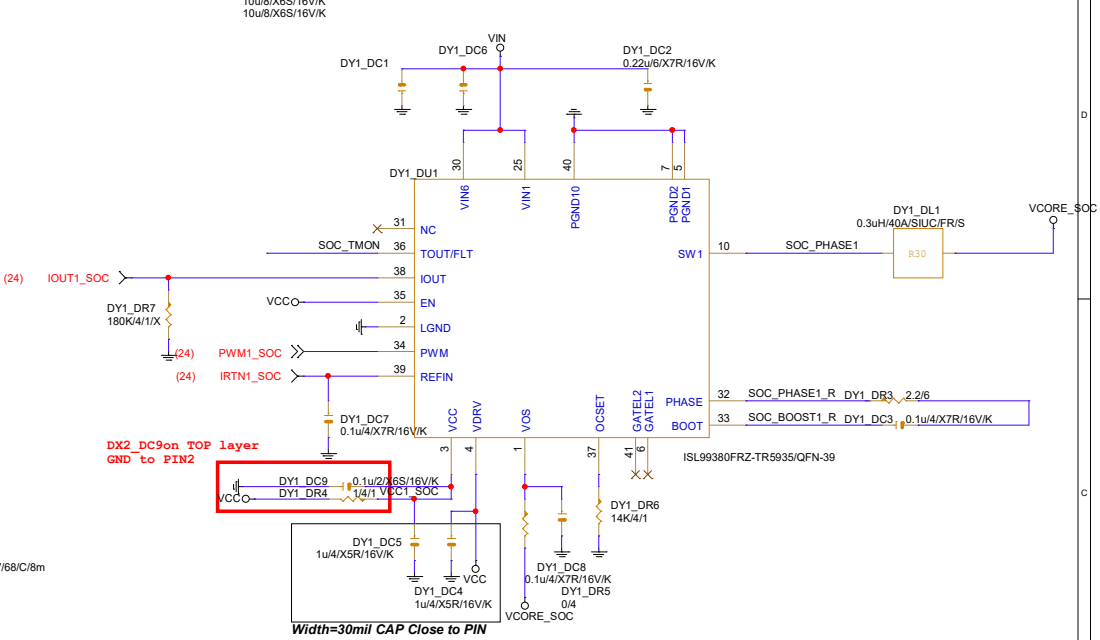
Title	VCORE_PSTAGE-4
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Size	Document Number	Rev
Custom	<b>B650E A PRO X USB4</b>	<b>1.0</b>
Date:	Friday, May 10, 2024	Sheet 28 of 67

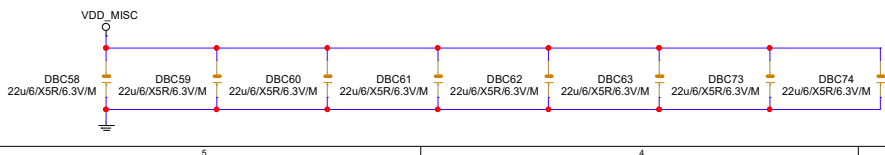
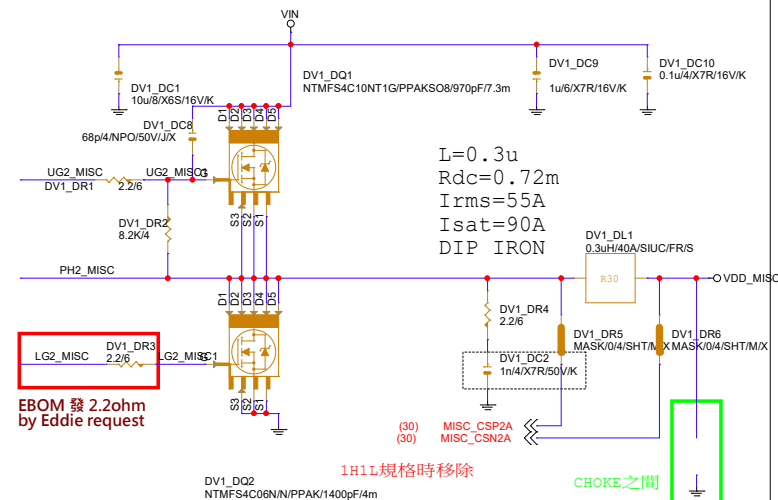
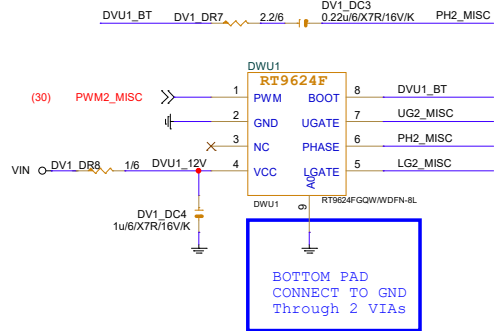
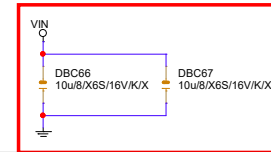
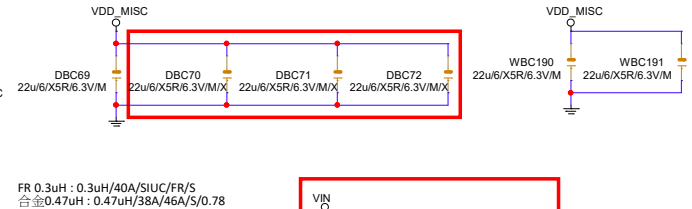
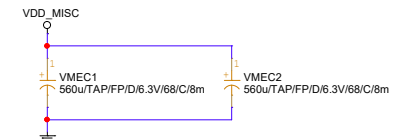
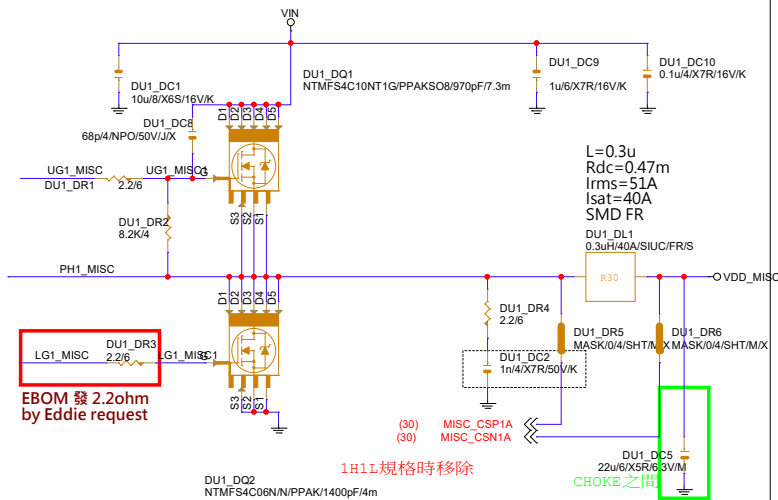
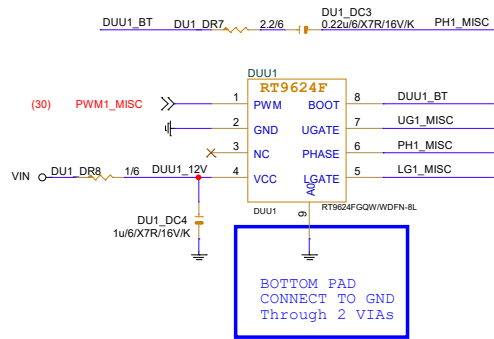
VCORE\_SOC PHASE1



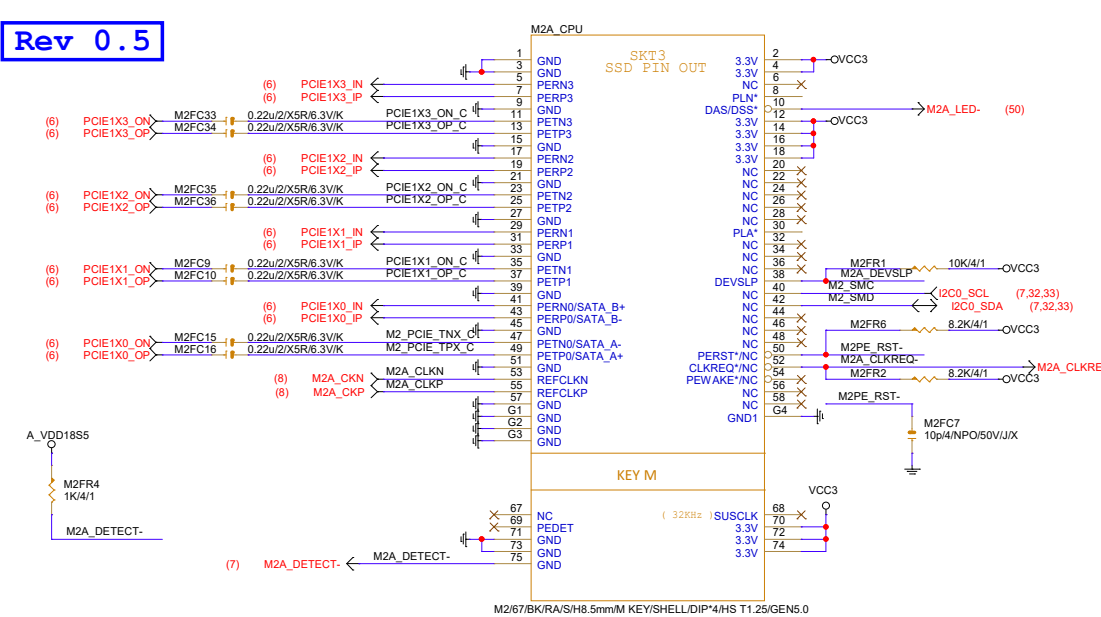
VCORE\_SOC PHASE2



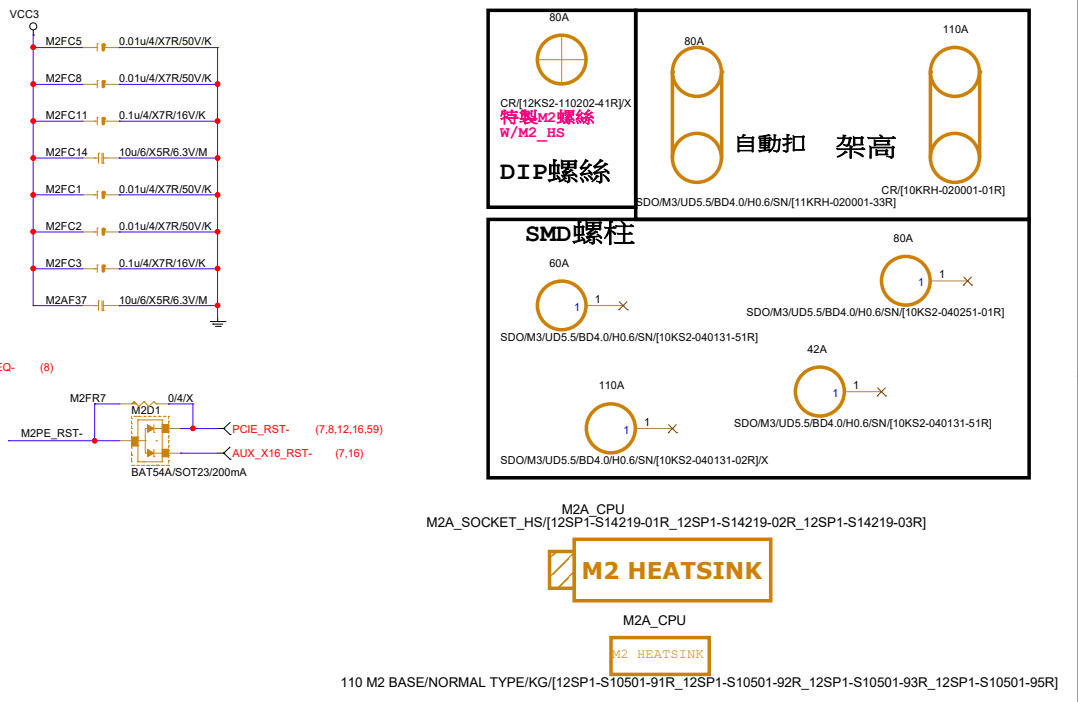




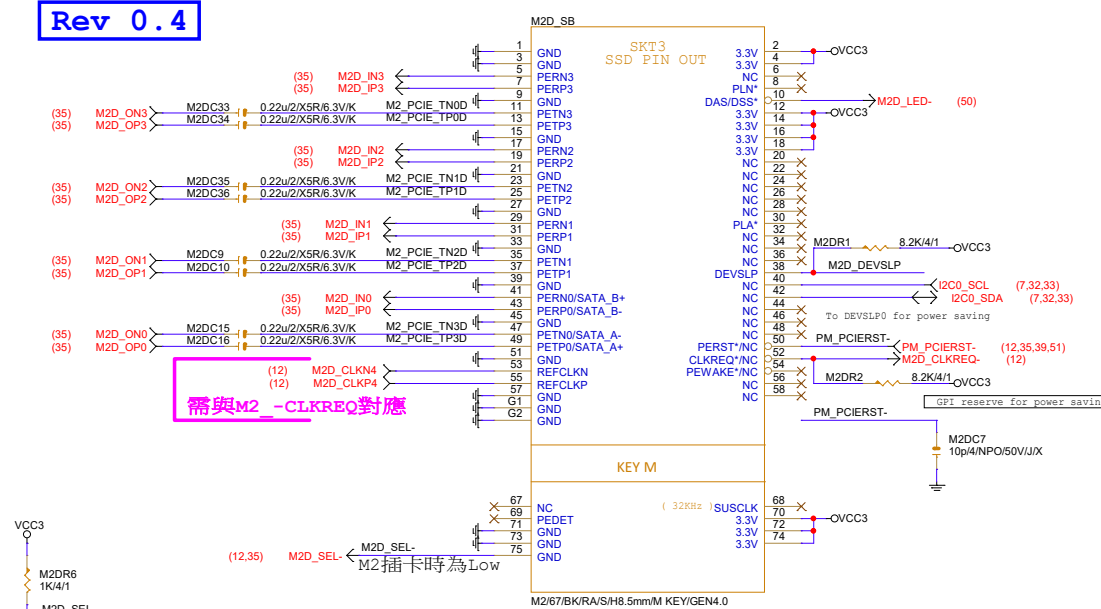
Rev 0.5



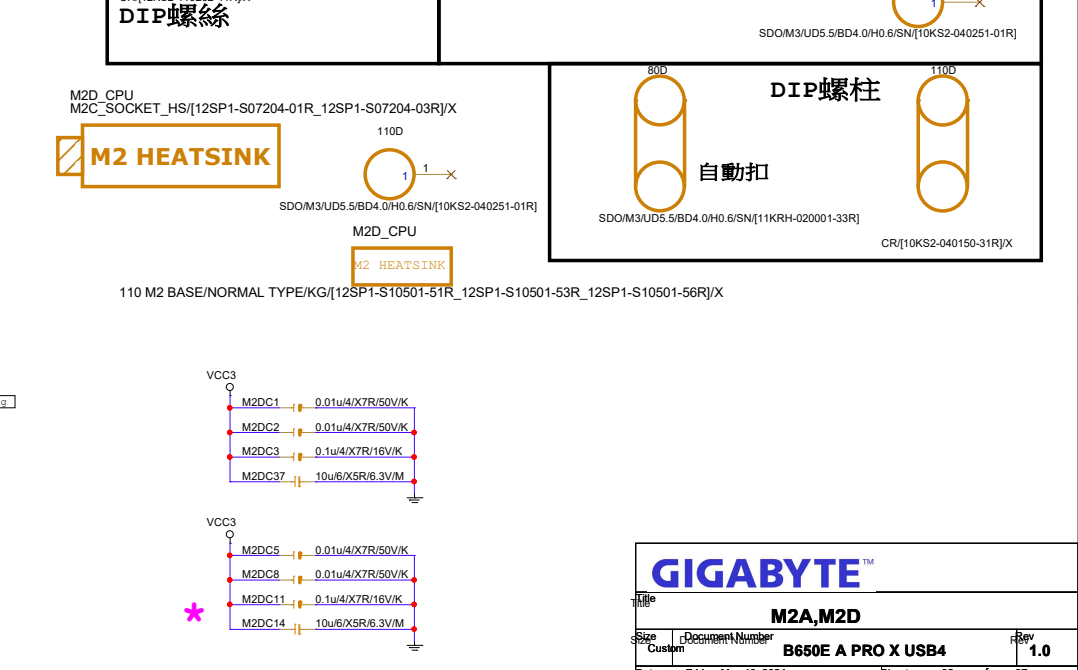
8.5H鐵殼  
Footprint :M2\_110(DIP)

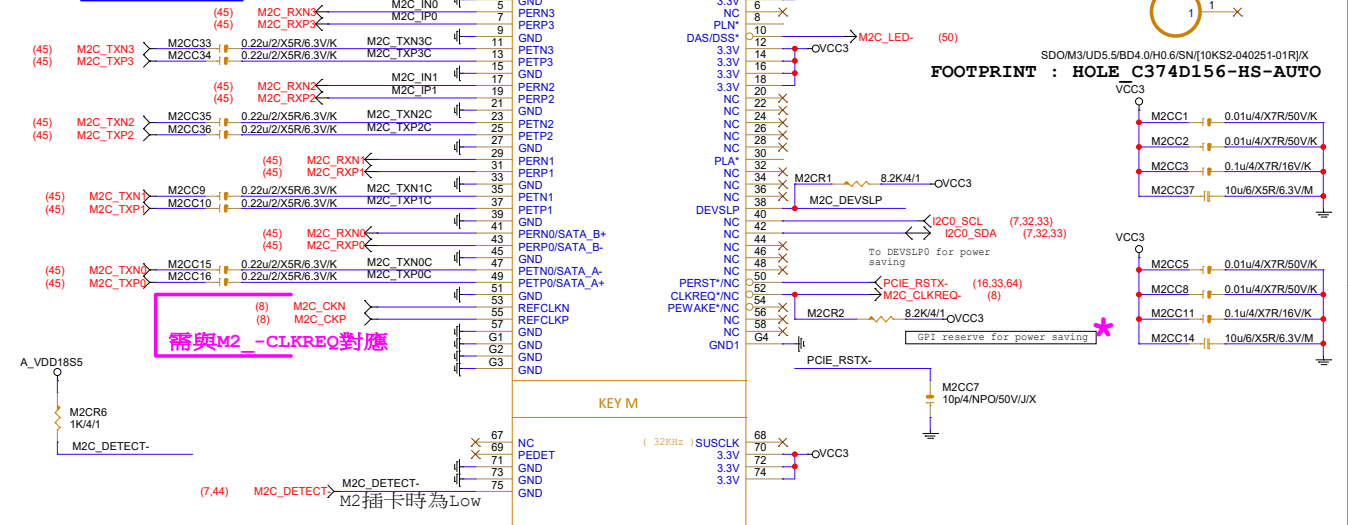
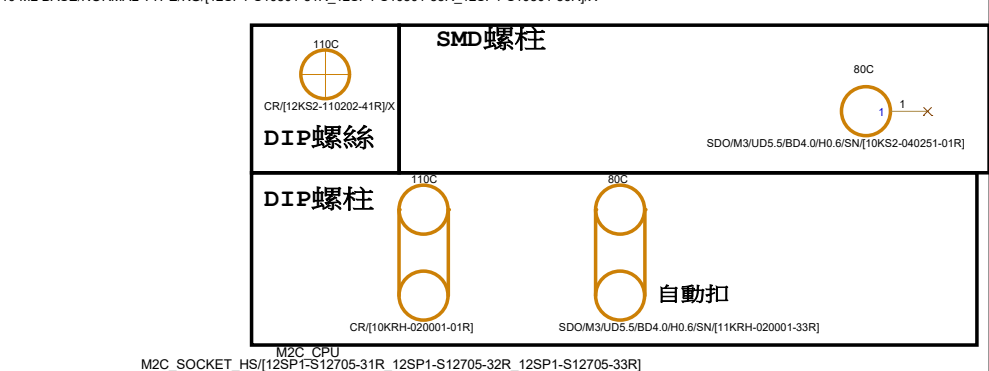
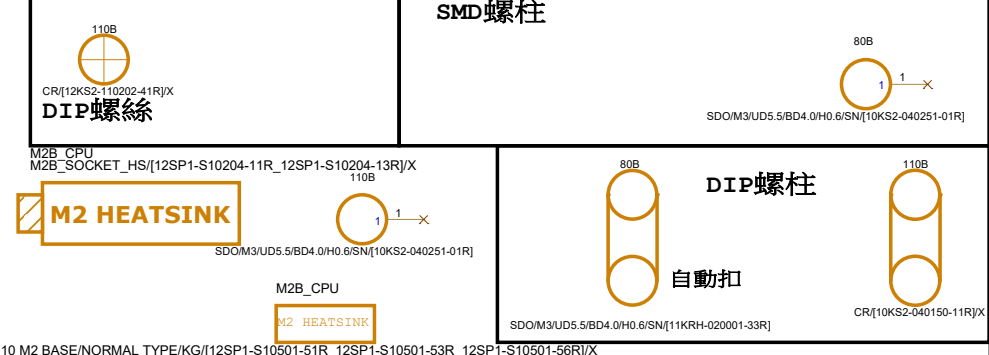
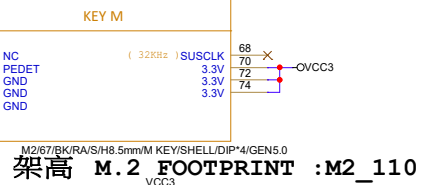
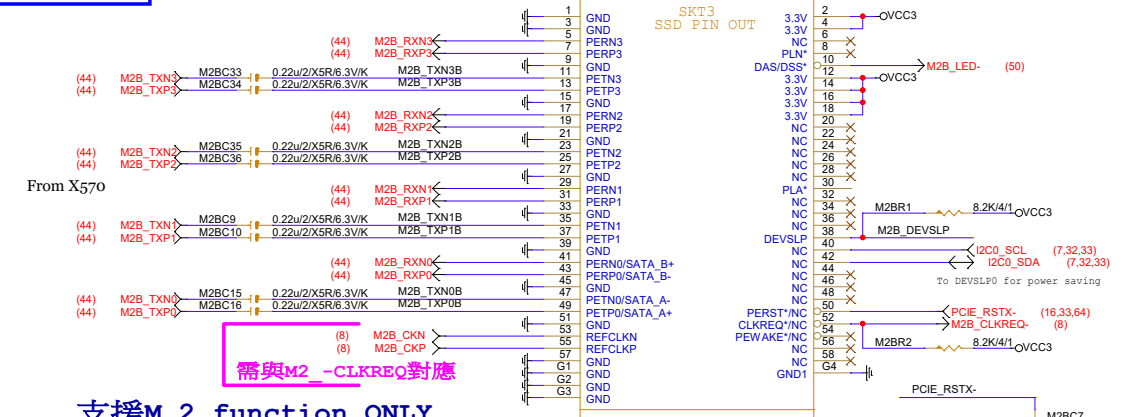


Rev 0.4

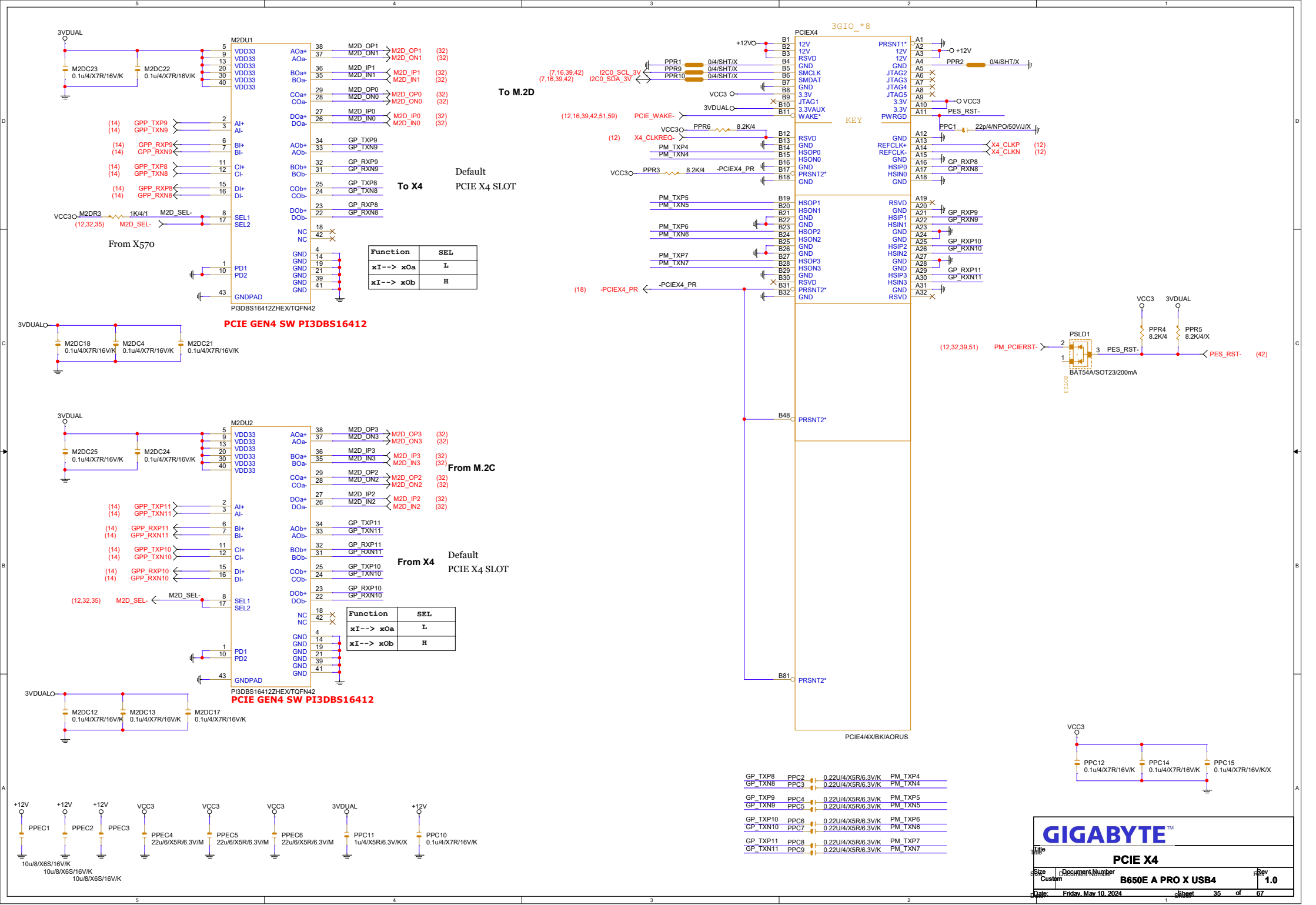


8.5H 架高無鐵殼  
Footprint : NGFF-M-75P-8CM-3A-SMD



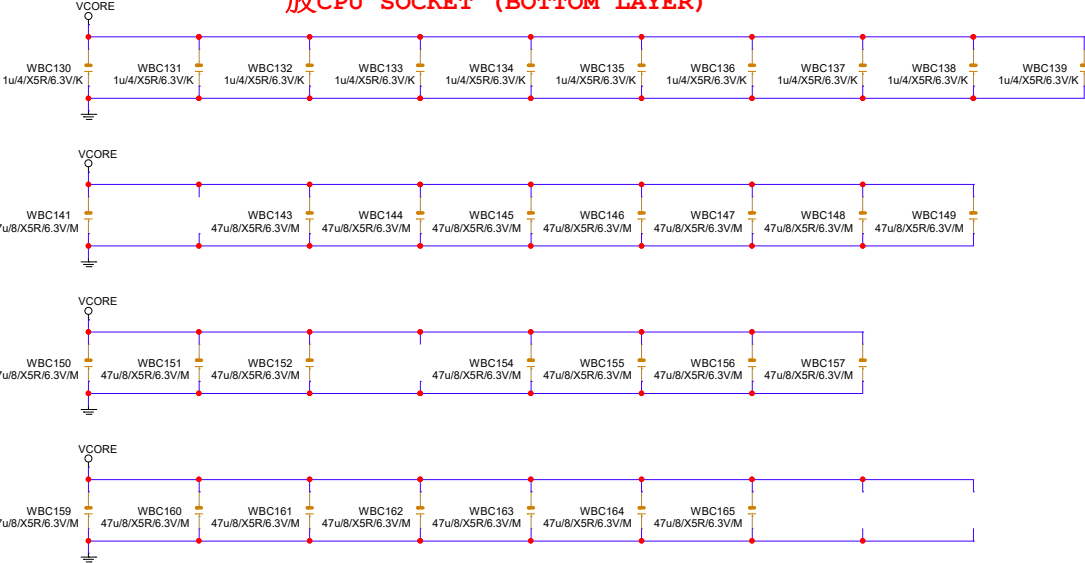




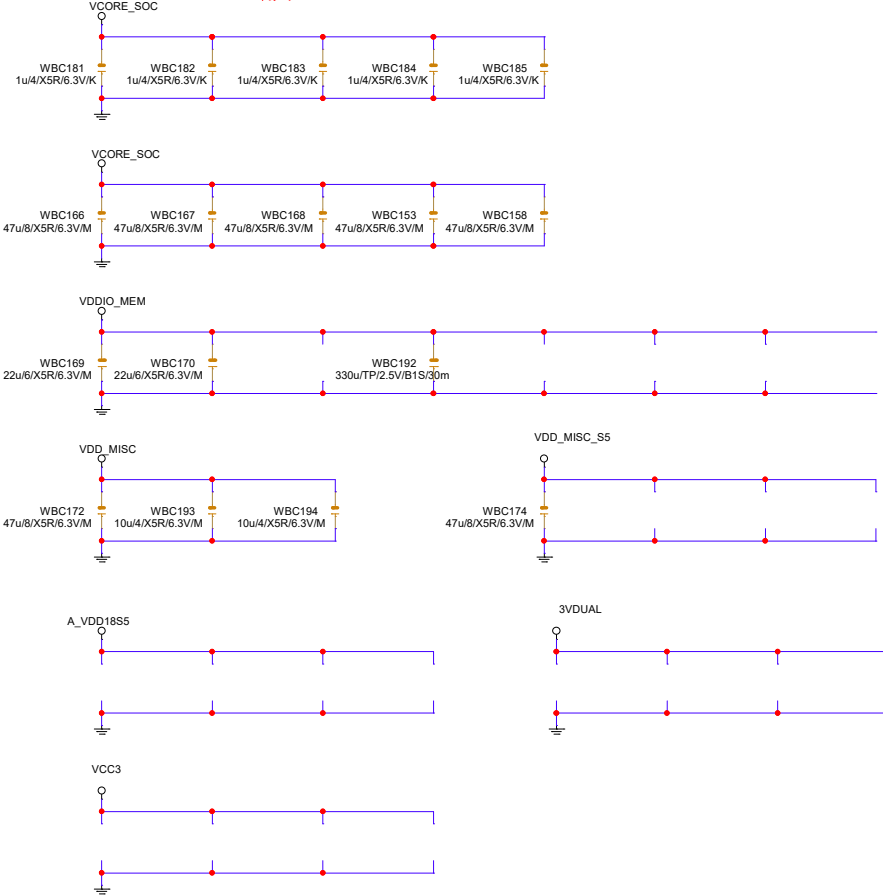




放CPU SOCKET (BOTTOM LAYER)

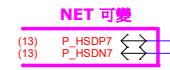


放CPU SOCKET (BOTTOM LAYER)





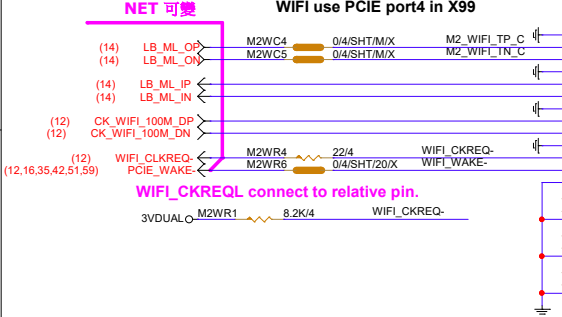
請選擇適用的USBport :  
SOC/UD7/UD5/G1/G7 : USB4  
;UD3/G5:USB6



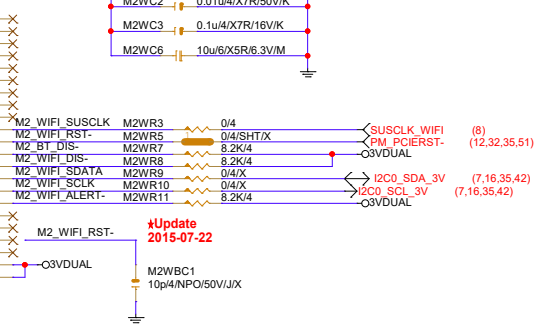
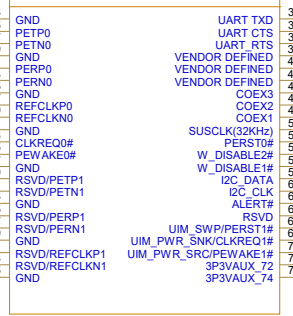
PCIe:15/4/4/4/15(breakout min 8/4/4/4/8)  
外層Impedance=85 +- 17.5%

PCIe:15/4/4/4/15(breakout min 8/4/4/4/8)  
內層 Impedance=85 +- 12%

WIFI use PCIe port4 in X99



Module Key E



Footprint Notice.

\*Update  
2015-07-22  
\*Footprint  
for 直立式  
SMD:  
WIFI-EKEY

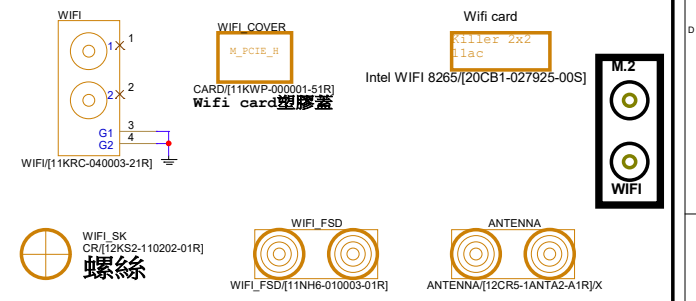
Footprint Notice.

\*Update  
2015-07-22  
\*Footprint for  
橫躺式SMD: NGFF-E-75P-2

FOR M.2 WIFI MODULE @ REAR PANEL

\*Update  
2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線





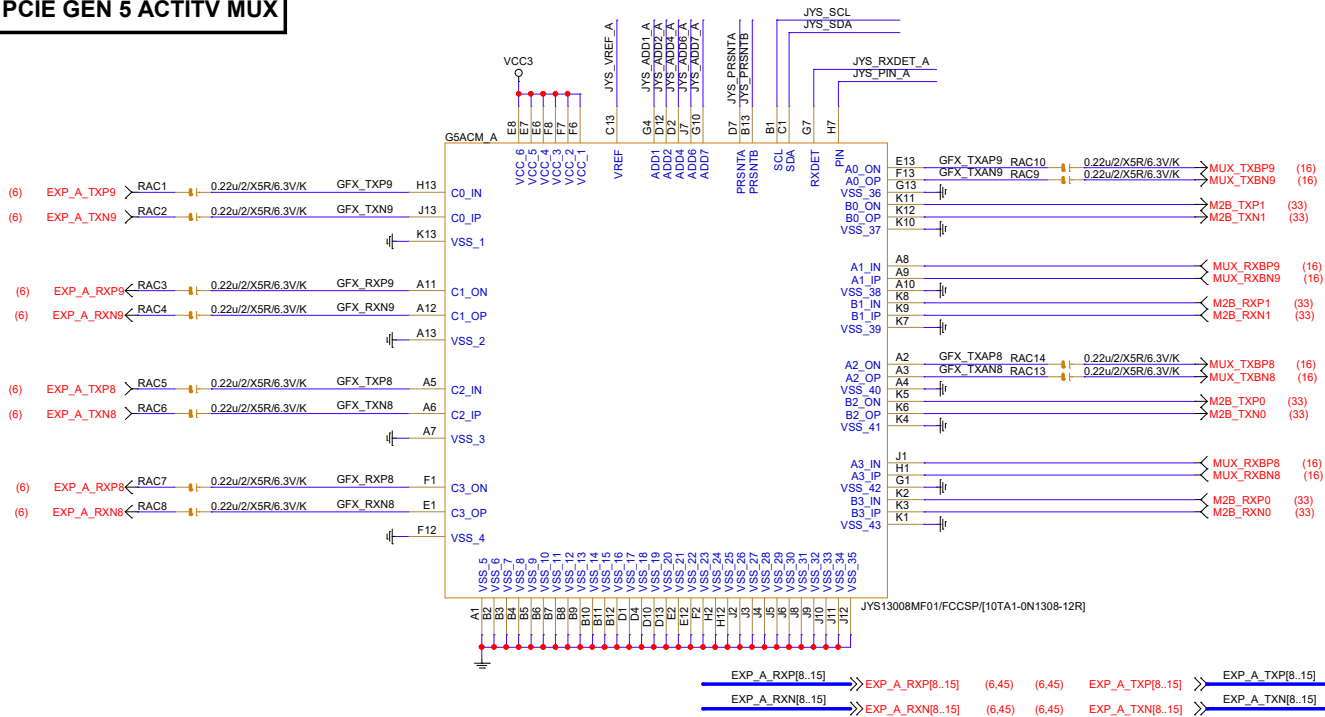




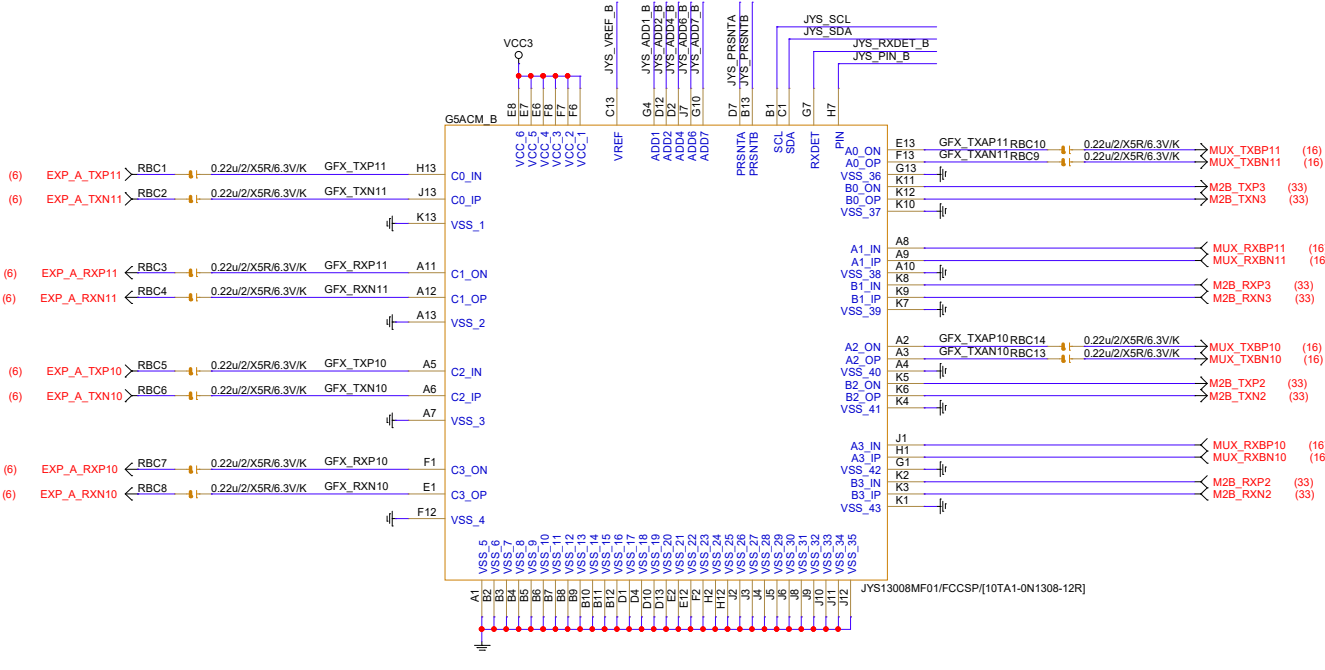
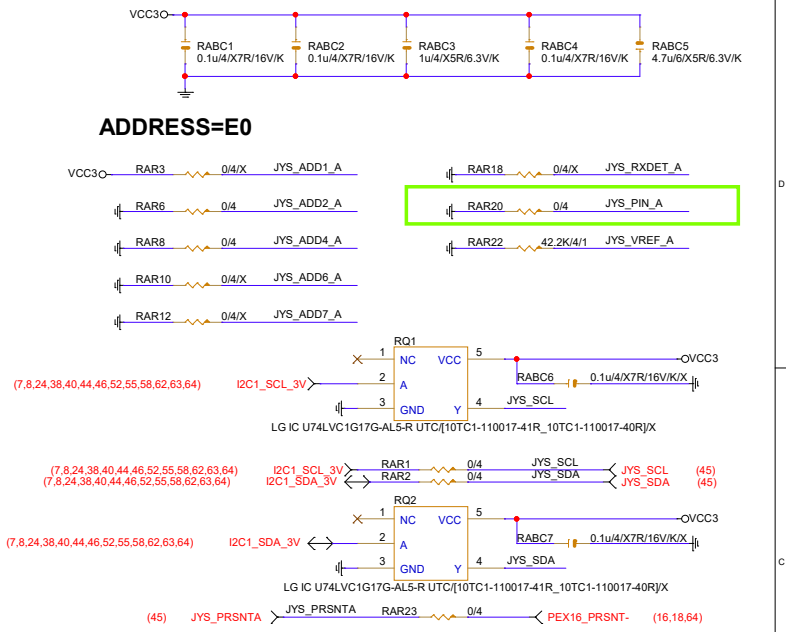


<div><div></div><div>GIGABYTE™</div></div>			
TitleCKG, HWM, TPM, THB			
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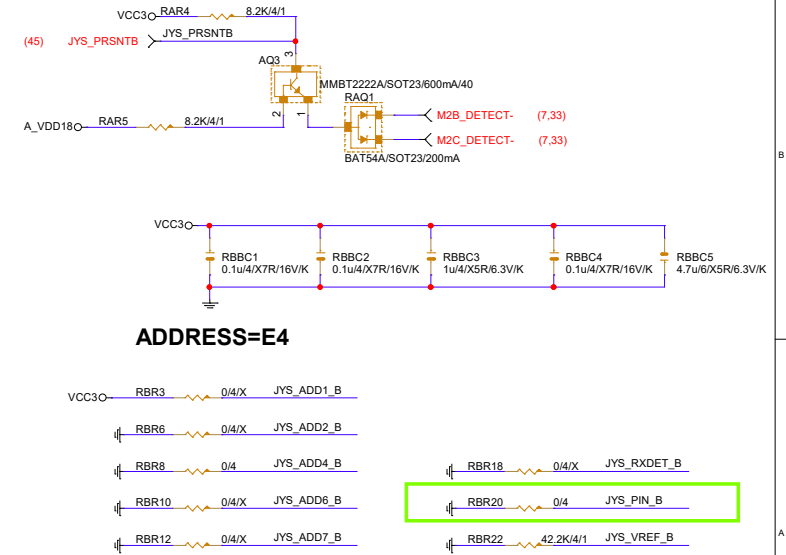
PCIE GEN 5 ACTIV MUX



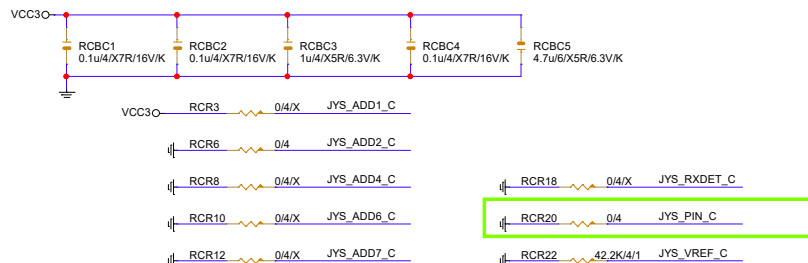
ADDRESS=E0



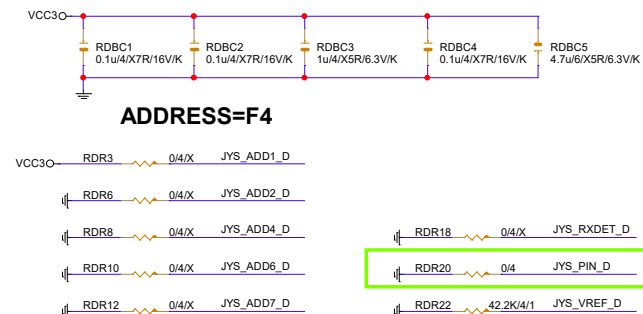
ADDRESS=E4



## PCIE GEN 5 ACTITV MUX



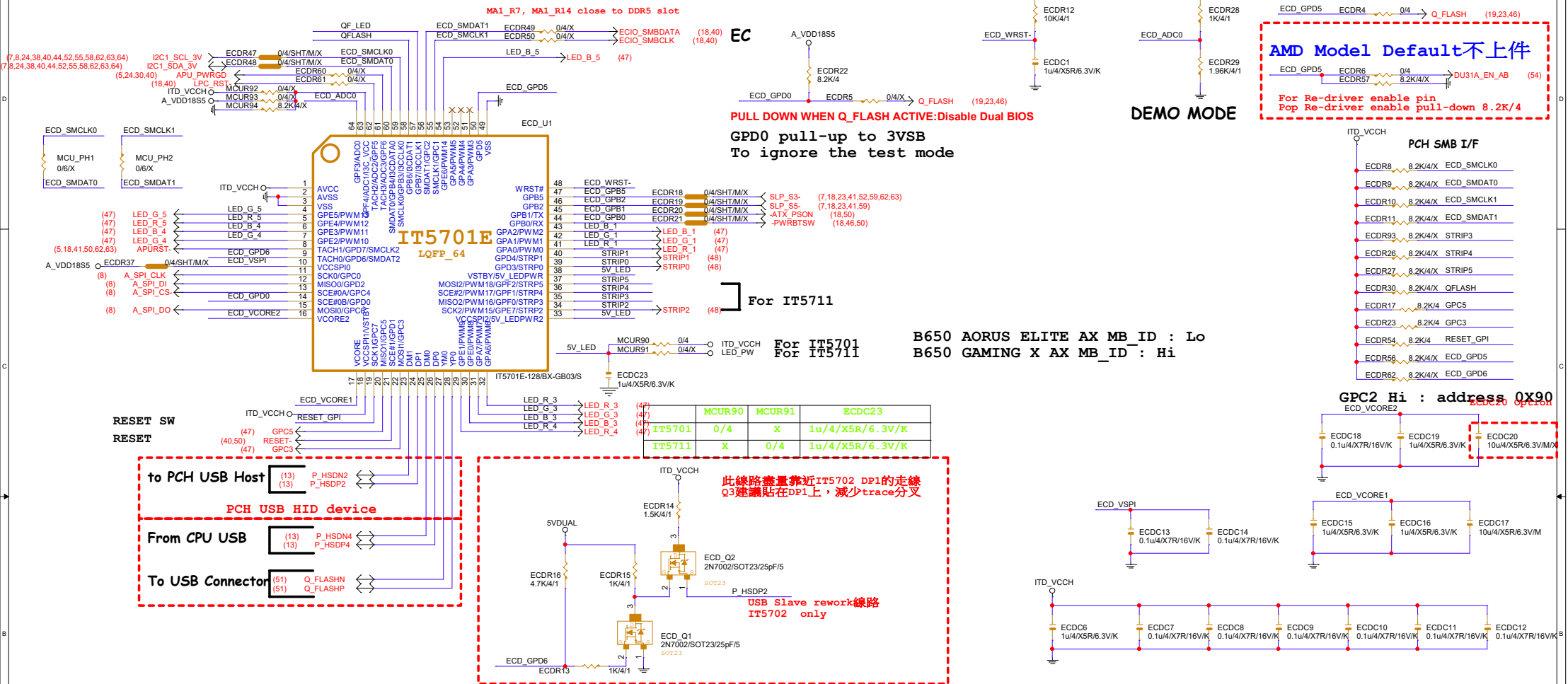
EXP_A_RXP[8..15]	>>	EXP_A_RXP[8..15]	(6,44)	(6,44)	EXP_A_TXP[8..15]	>>	EXP_A_TXP[8..15]
EXP_A_RXN[8..15]	>>	EXP_A_RXN[8..15]	(6,44)	(6,44)	EXP_A_TXN[8..15]	>>	EXP_A_TXN[8..15]



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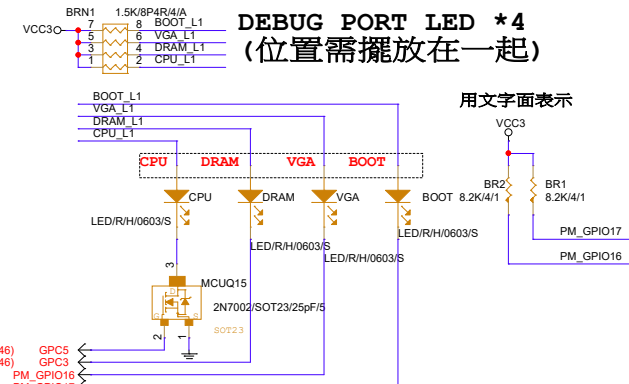
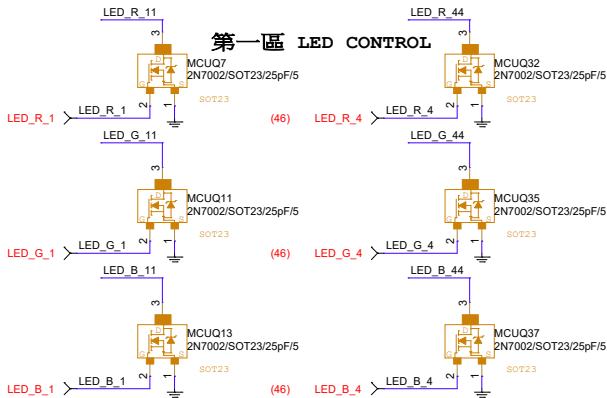
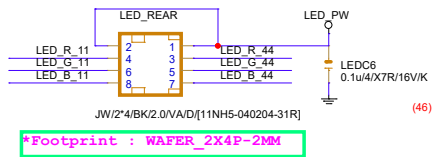
Title				<b>PCIE GEN5 AMC-2</b>			
Size	Custom	Document Number	<b>B650E A PRO X USB4</b>				Rev
							<b>1.0</b>
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## ECD\_U1 請放在PCH到BIOS路徑上. 避免線過長



## 第一區 LED

FOR 後窗裝甲 led connect  
(LED\_COVER放在後窗裝甲內)

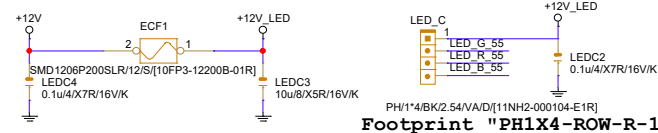
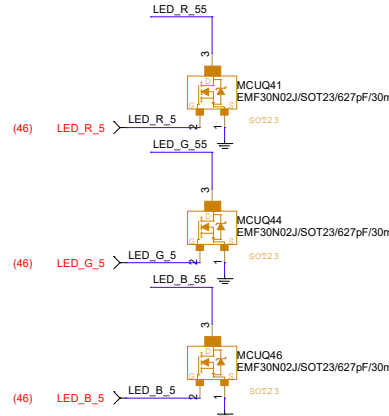


## 第三區 LED

## 第五區 LED

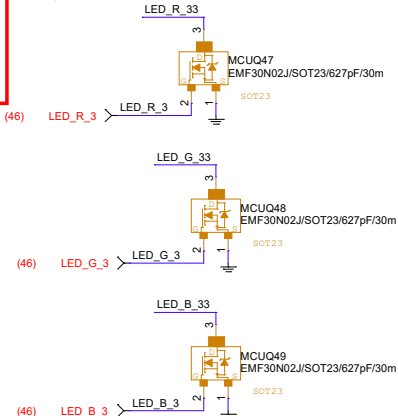
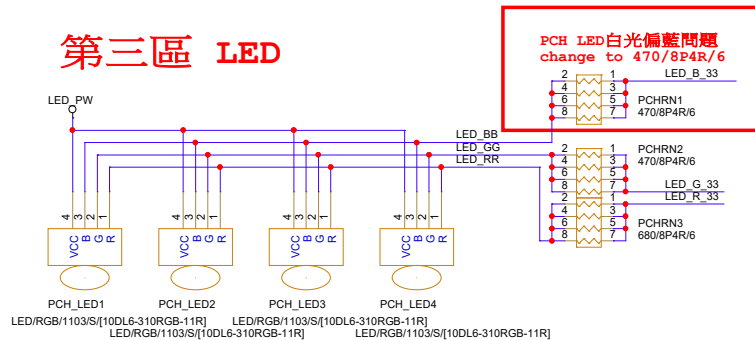
第五區 LED CONTROL

燈條 LED (LED\_C放在PCB左邊板邊位置)



## 第三區 LED

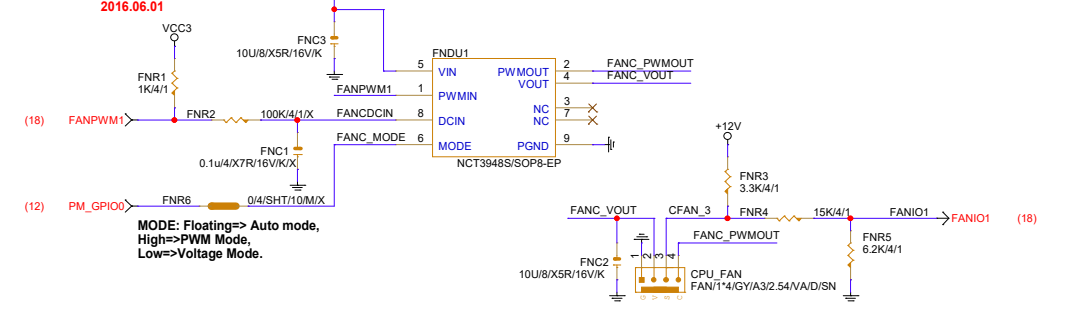
第三區 LED CONTROL



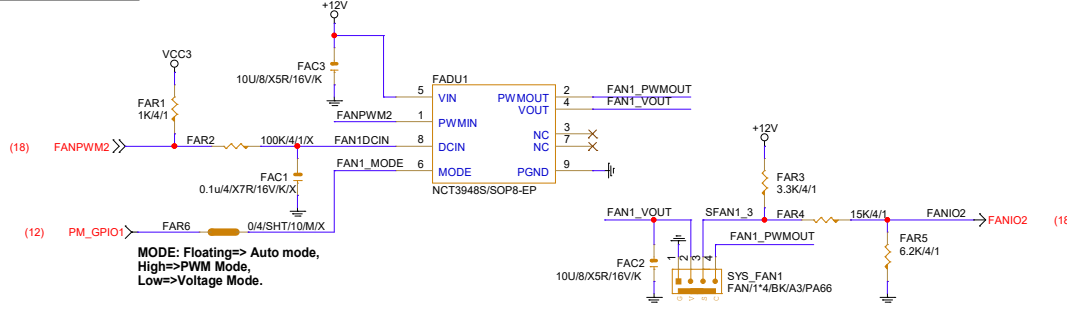
FOOTPRINT : LED-4P-RGB-SIDE-1



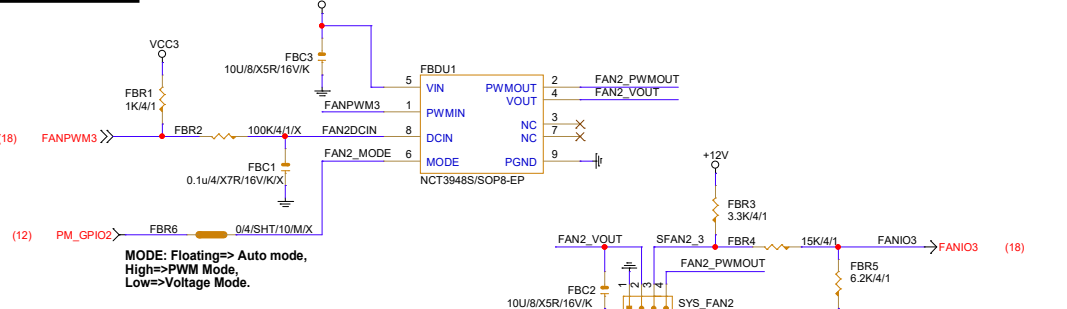
Rev: 0.8



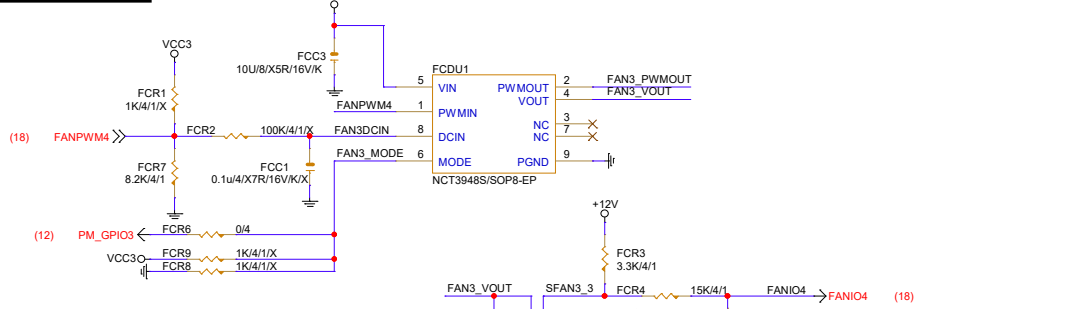
SYSTEM FAN1



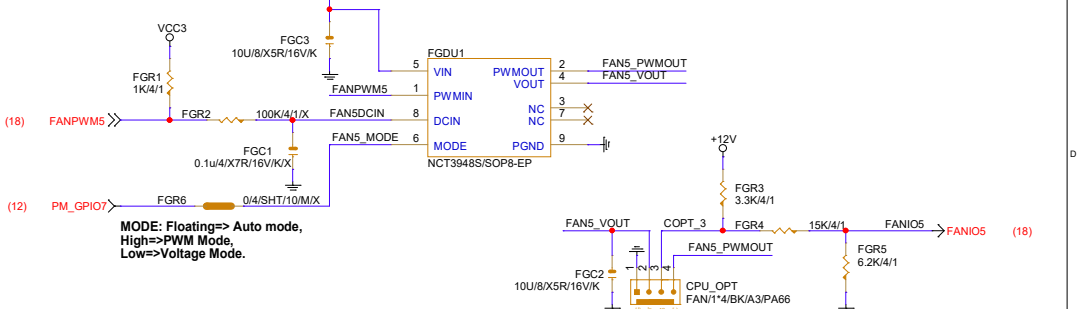
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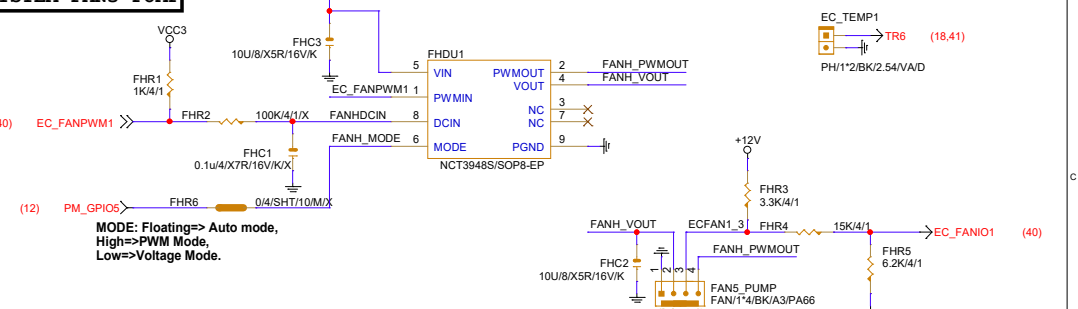
SYSTEM FAN3



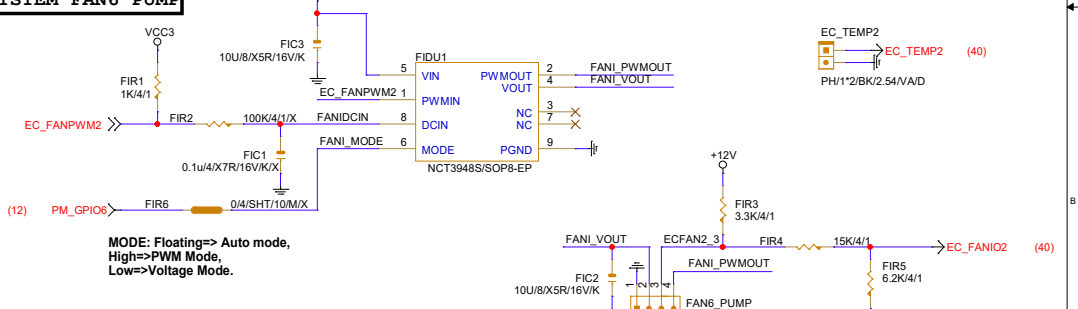
CPU\_OPT



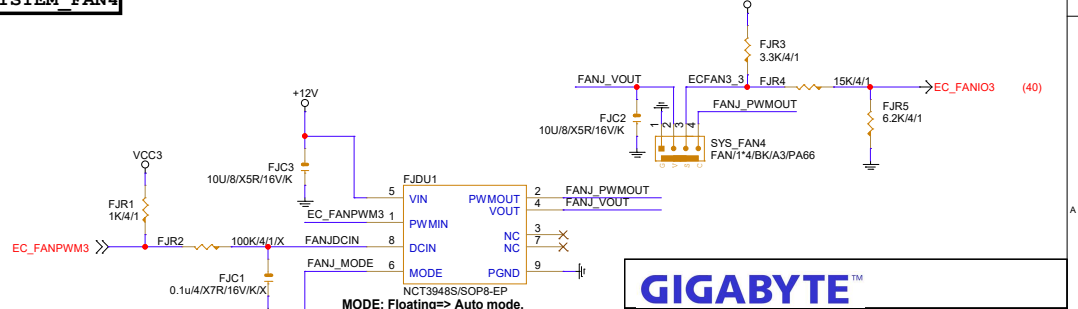
SYSTEM FAN5 PUMP



SYSTEM FAN6 PUMP



SYSTEM\_FAN4

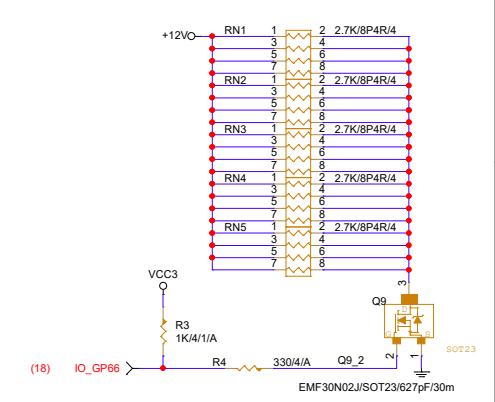
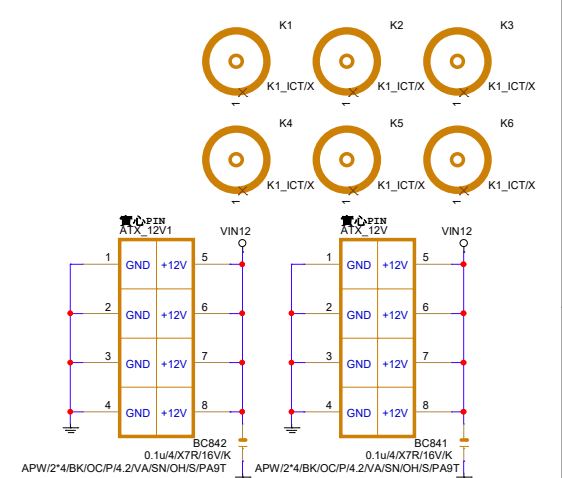
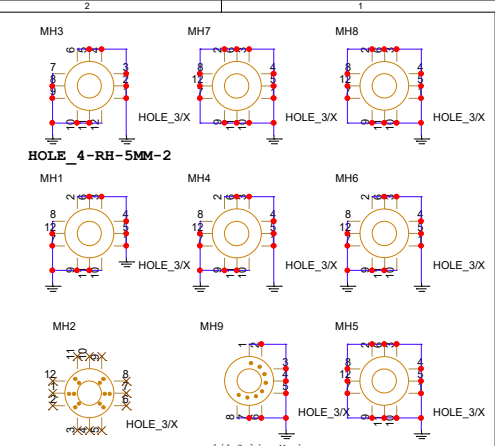


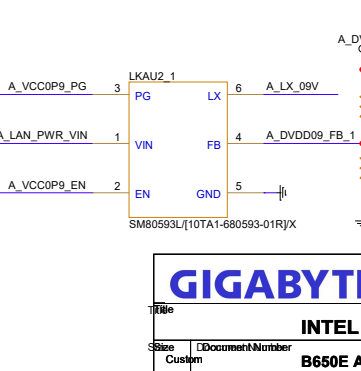
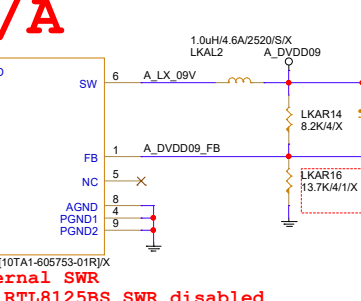
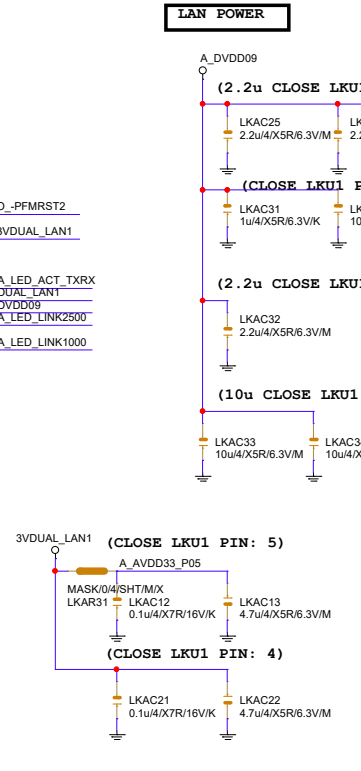
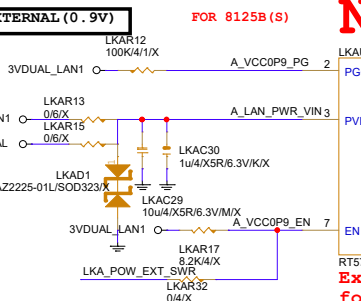
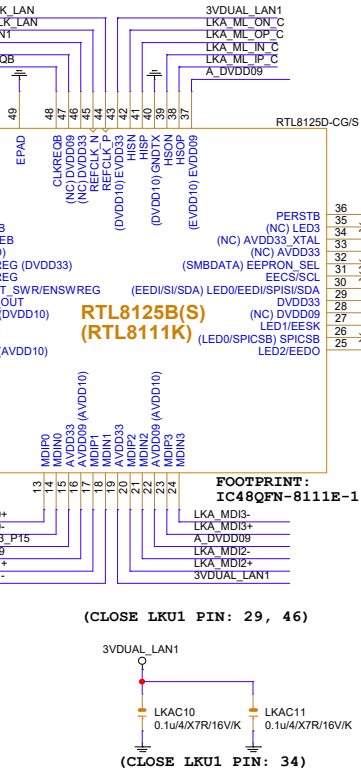
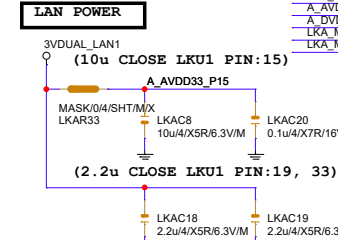
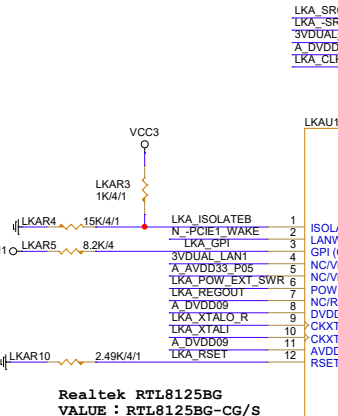
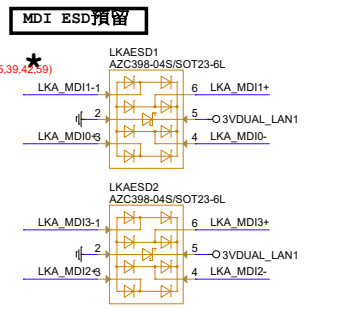
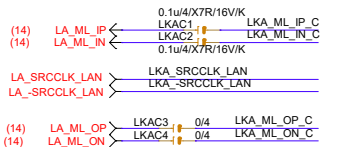
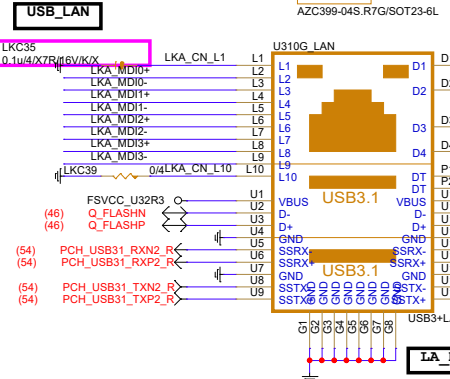
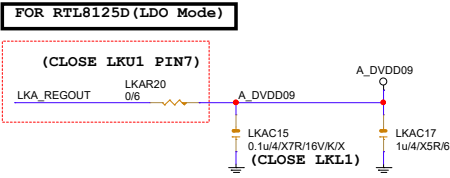
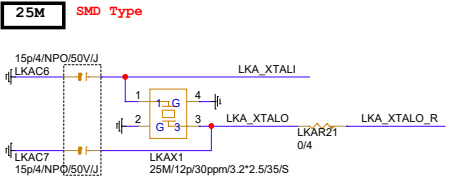
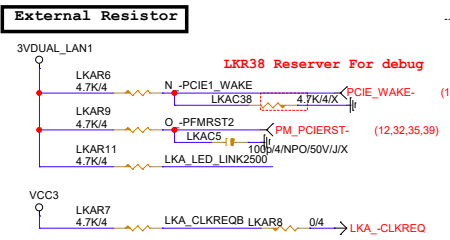
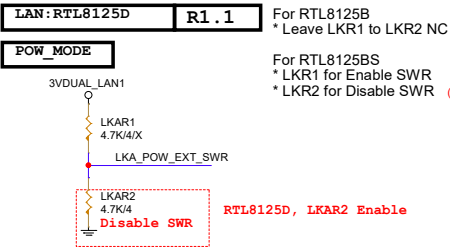
KBL FAN LOCATION MAP REFER TO PAGE.27

**GIGABYTE**

**FAN**

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**INTEL I225V LAN**

**B650E A PRO X USB4**

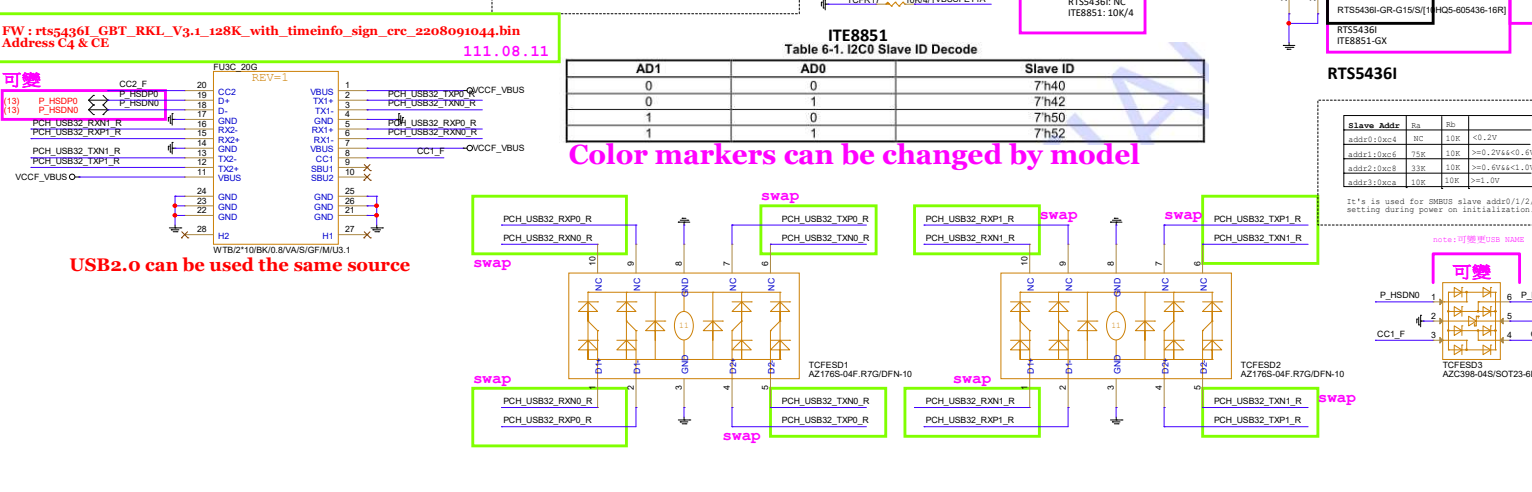
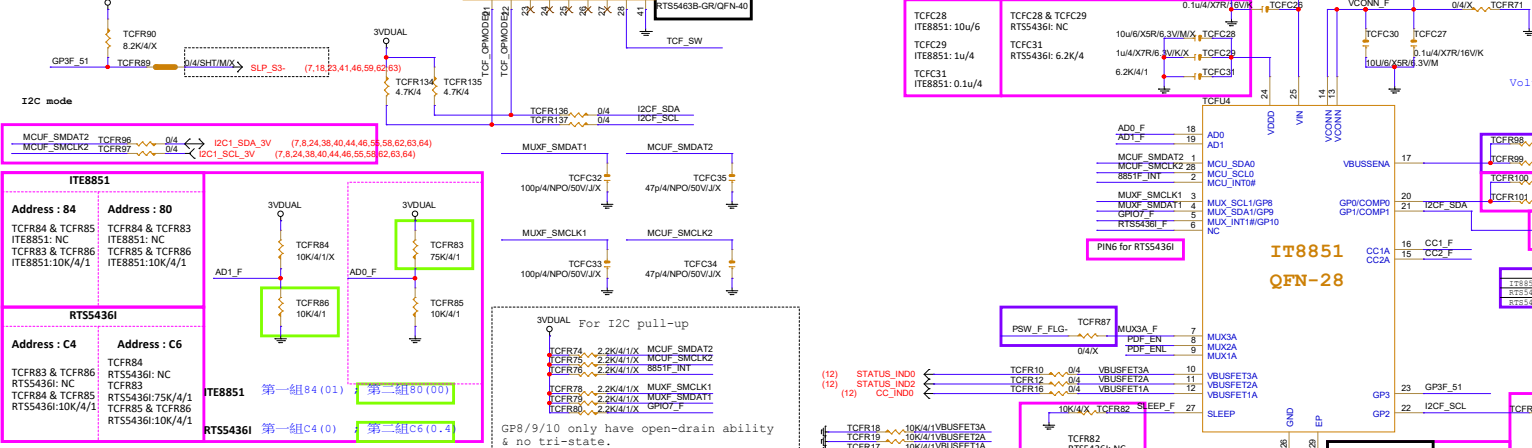
Size: Custom

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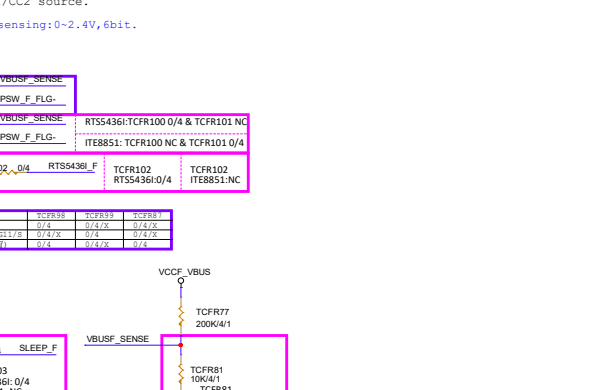
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GROUP F Front TypeC

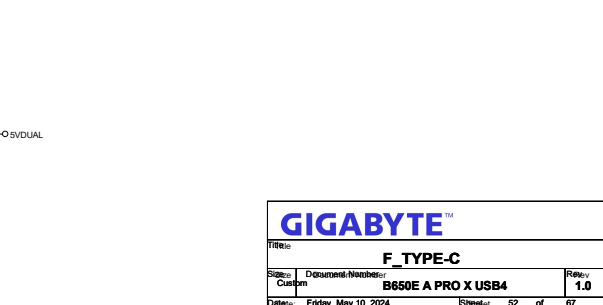


TCFU2	TCFU3	TCFU4	TCFU5	TCFU6	TCFU7	TCFU14	TCFU11	TCFU5	TCFU11
SY6863B3	SY6863B3	NC	2.2K/4.7K	NC	100k/8	4.7k/5k	0/4.7k	0/4.7k	1.2k/4.7k
RT9742A1	RT9742A1	NC	NC	NC	100k/8	100k/8	0/4.7k	0/4.7k	1.2k/4.7k
RT9742A2	RT9742A2	NC	NC	NC	100k/8	100k/8	0/4.7k	0/4.7k	1.2k/4.7k

NN is a power  
out for switch to  
(C22) power



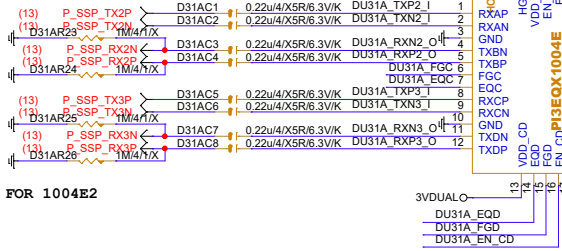
RTSS436i: 10K/4/1  
ITE8851: 20K/4/1





**GROUP A**

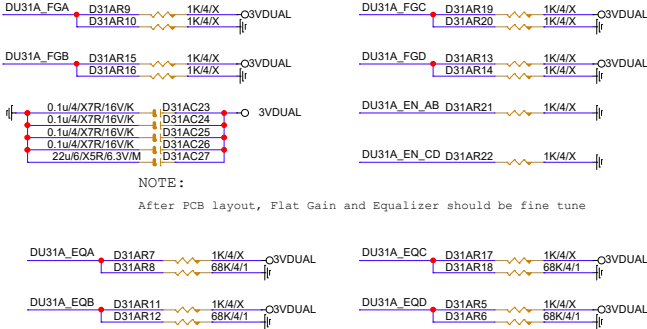
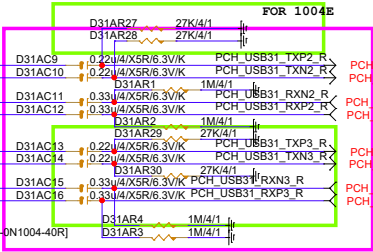
## PCH Site



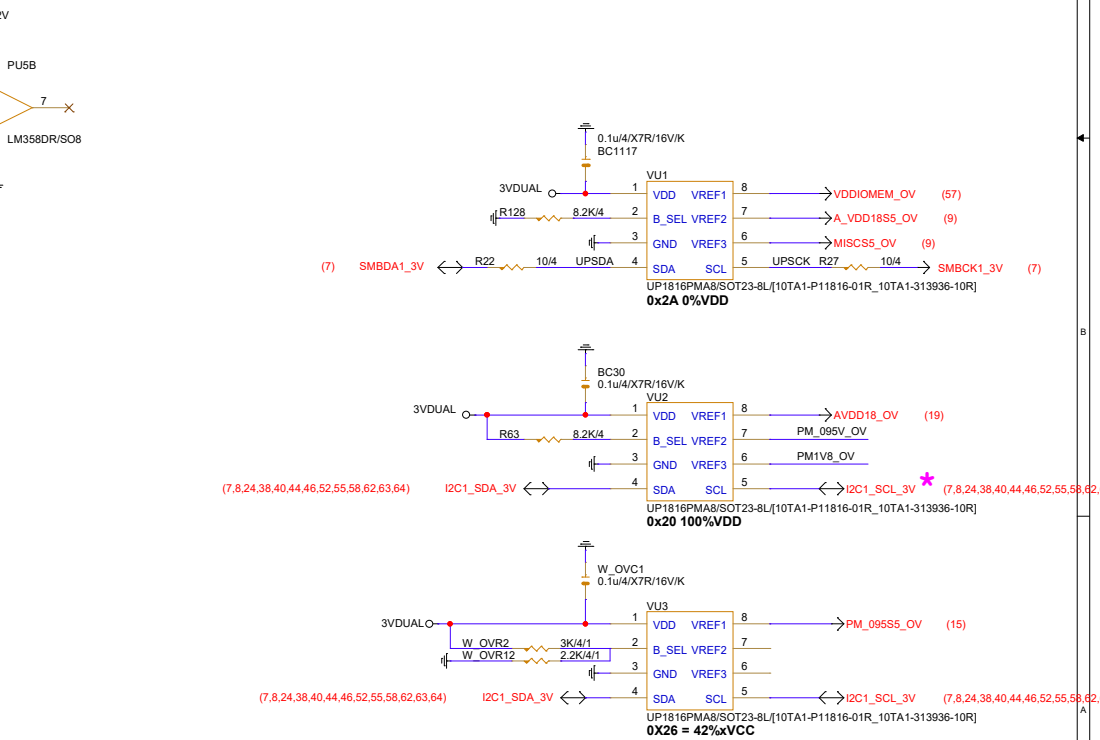
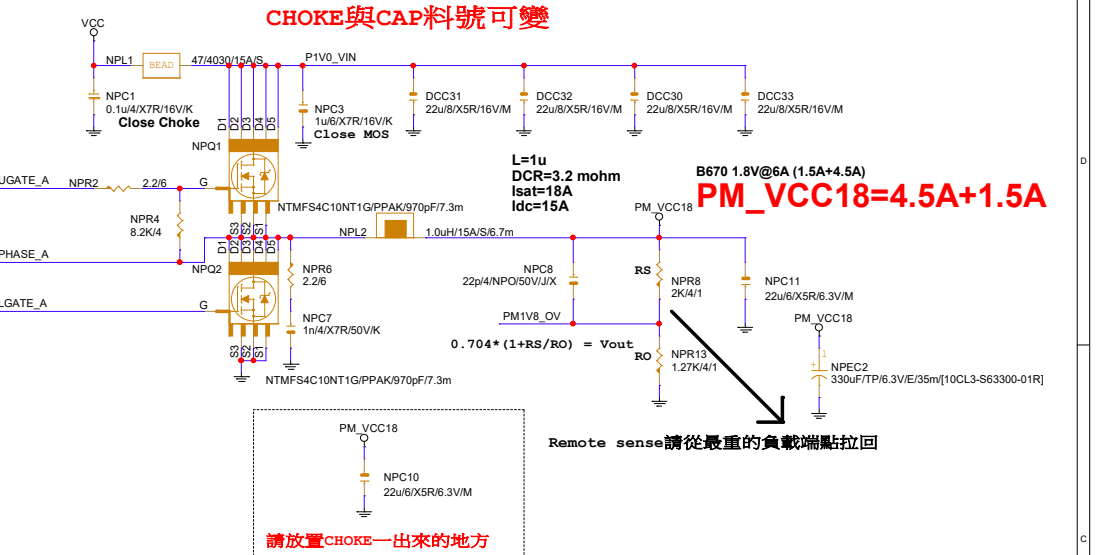
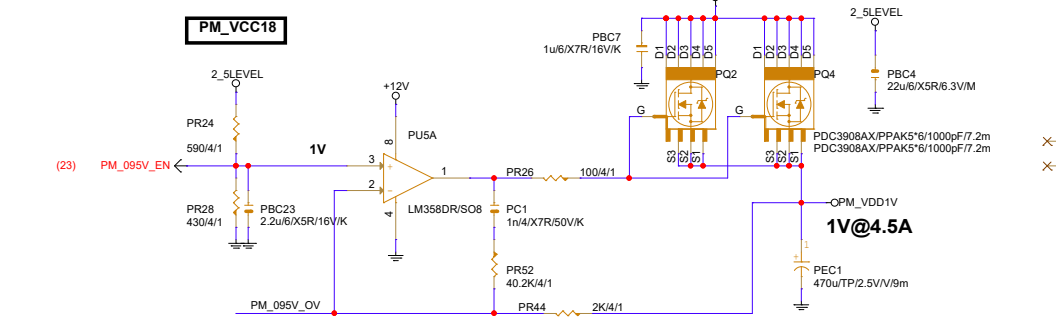
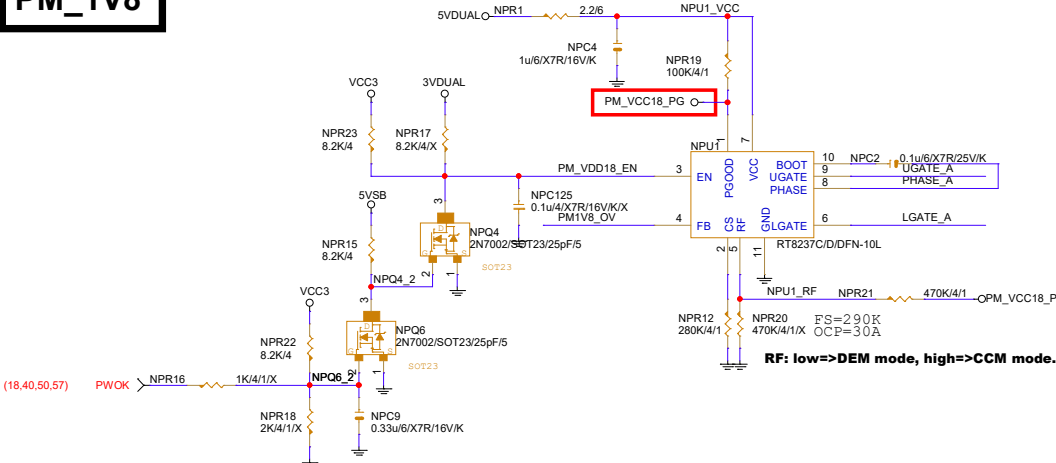
Layout Rule:

1. Differential Pair can't be swapped
2. Redriver to Connector Length min. 1 inch
3. PCH to Redriver Length min. 6 inch

## USB Type A Connector Site



PM\_1V8



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

GIGABYTE™

File

PM\_OWR\_OC\_DAC

Size

Custom

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1.0

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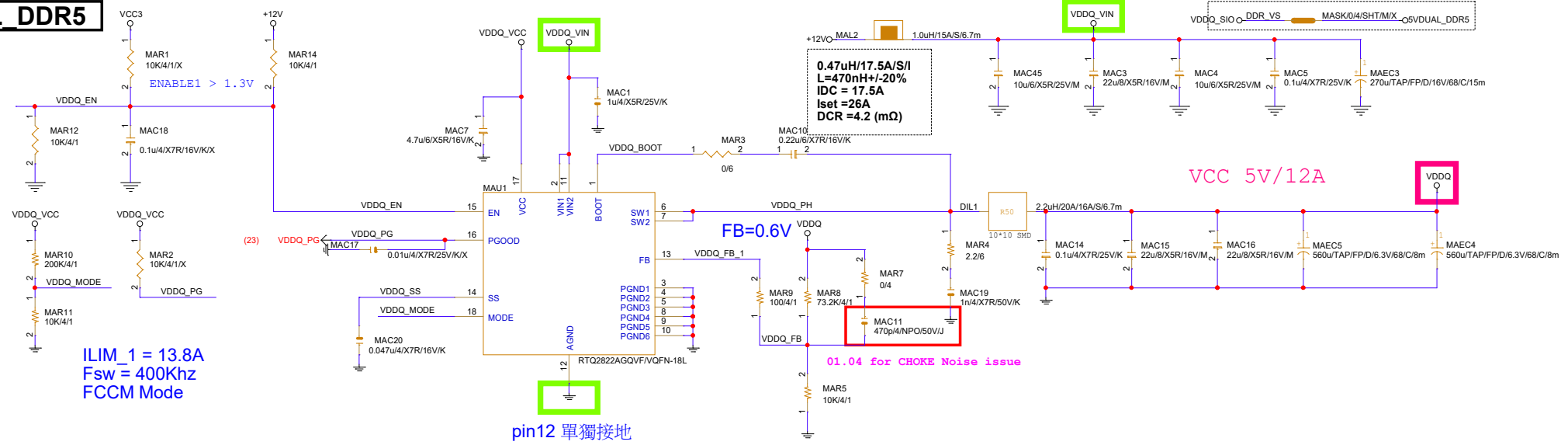
67

PM\_OWR\_OC\_DAC

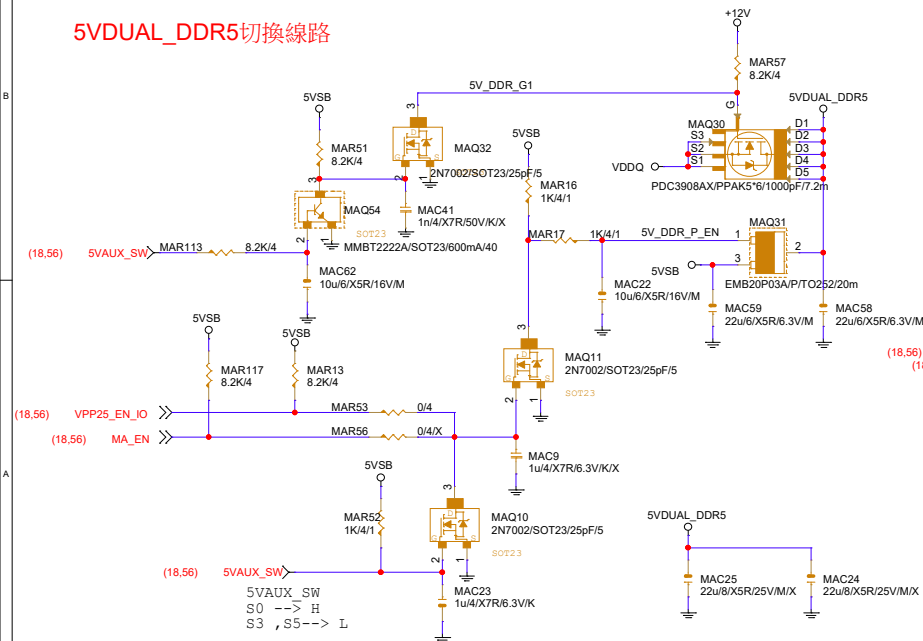
B650E A PRO X USB4

Rev 1.0

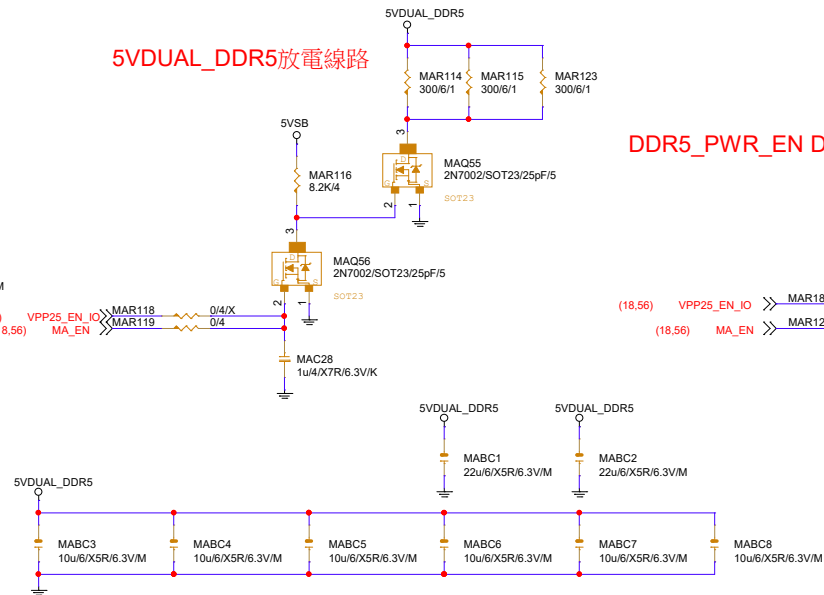
REV: 0.13



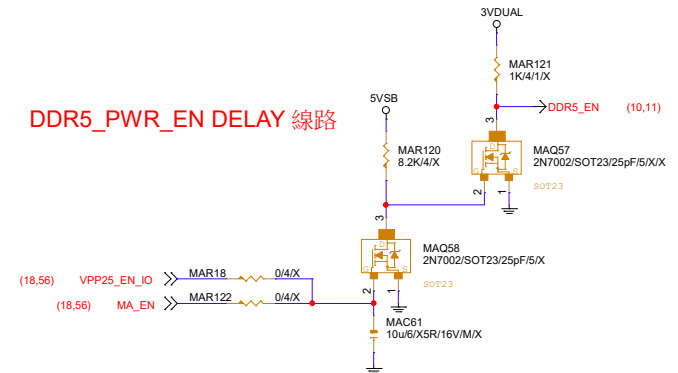
## 5VDUAL\_DDR5切換線路



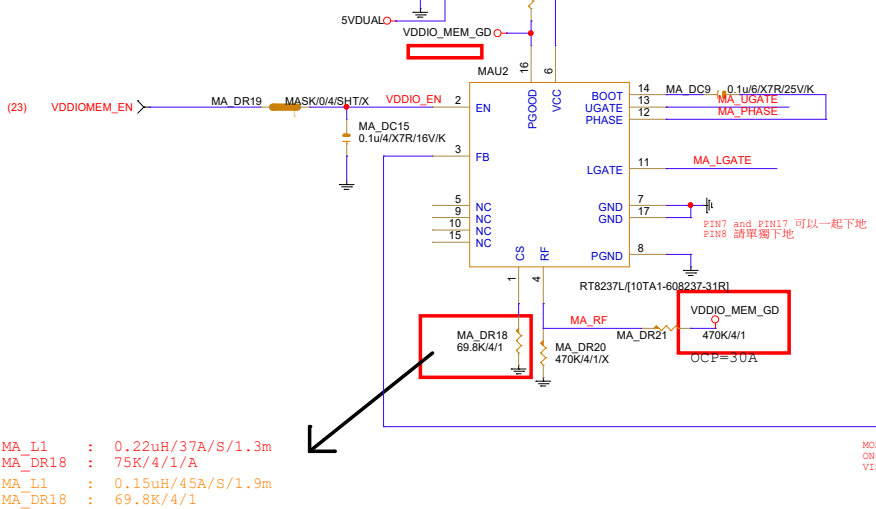
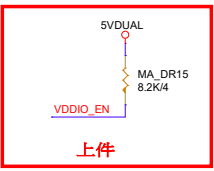
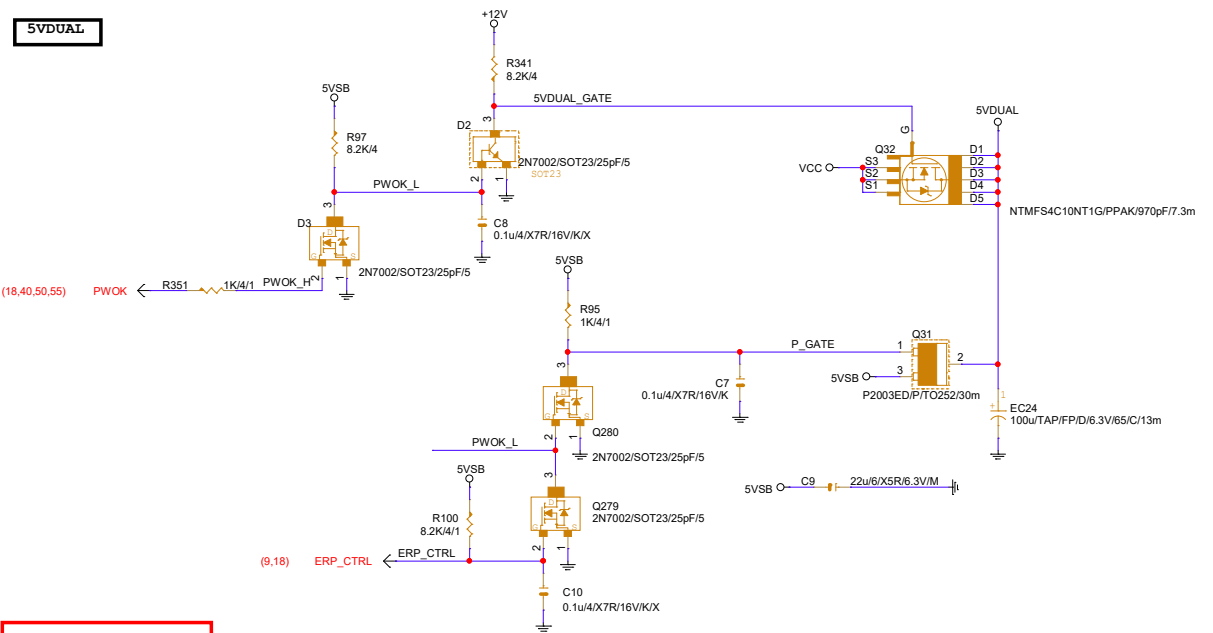
### 5VDUAL\_DDR5放電線路



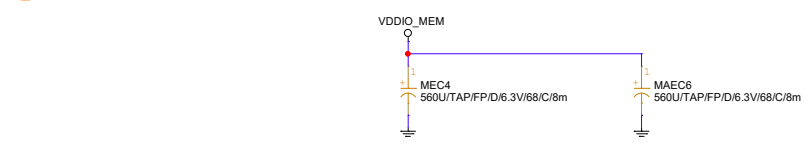
## DDR5\_PWR\_EN DELAY 線路



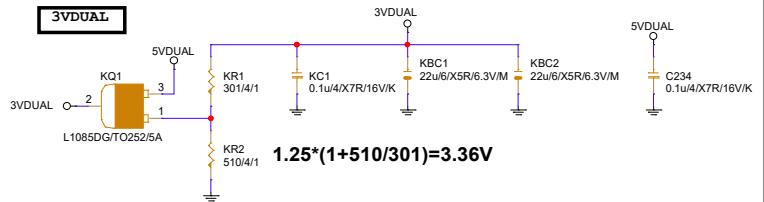
5VDUAL



MA\_L1 : 0.22uH/37A/S/1.3m  
MA\_DR18 : 75K/4/1/A  
MA\_L1 : 0.15uH/45A/S/1.9m  
MA\_DR18 : 69.8K/4/1

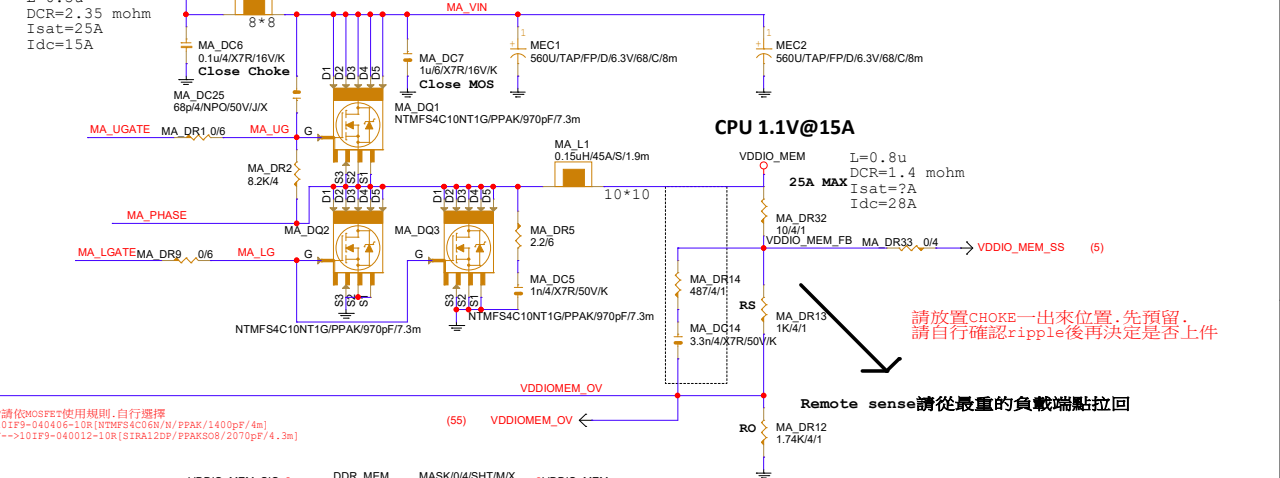


3VDUAL



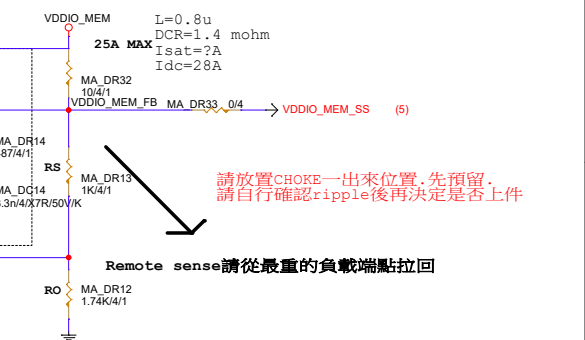
$1.25 \times (1 + 510/301) = 3.36V$

DDR VIN CAP 560u\*2PCS



MOSFET請依MOSFET使用規則,自行選擇  
ON->>101F9-040406-10R[NTMFS4C06N/N/PPAK/1400pF/4m]  
VISHAY->>101F9-040012-10R[SIRAL2DP/PPAKS08/2070pF/4.3m]

CPU 1.1V@15A

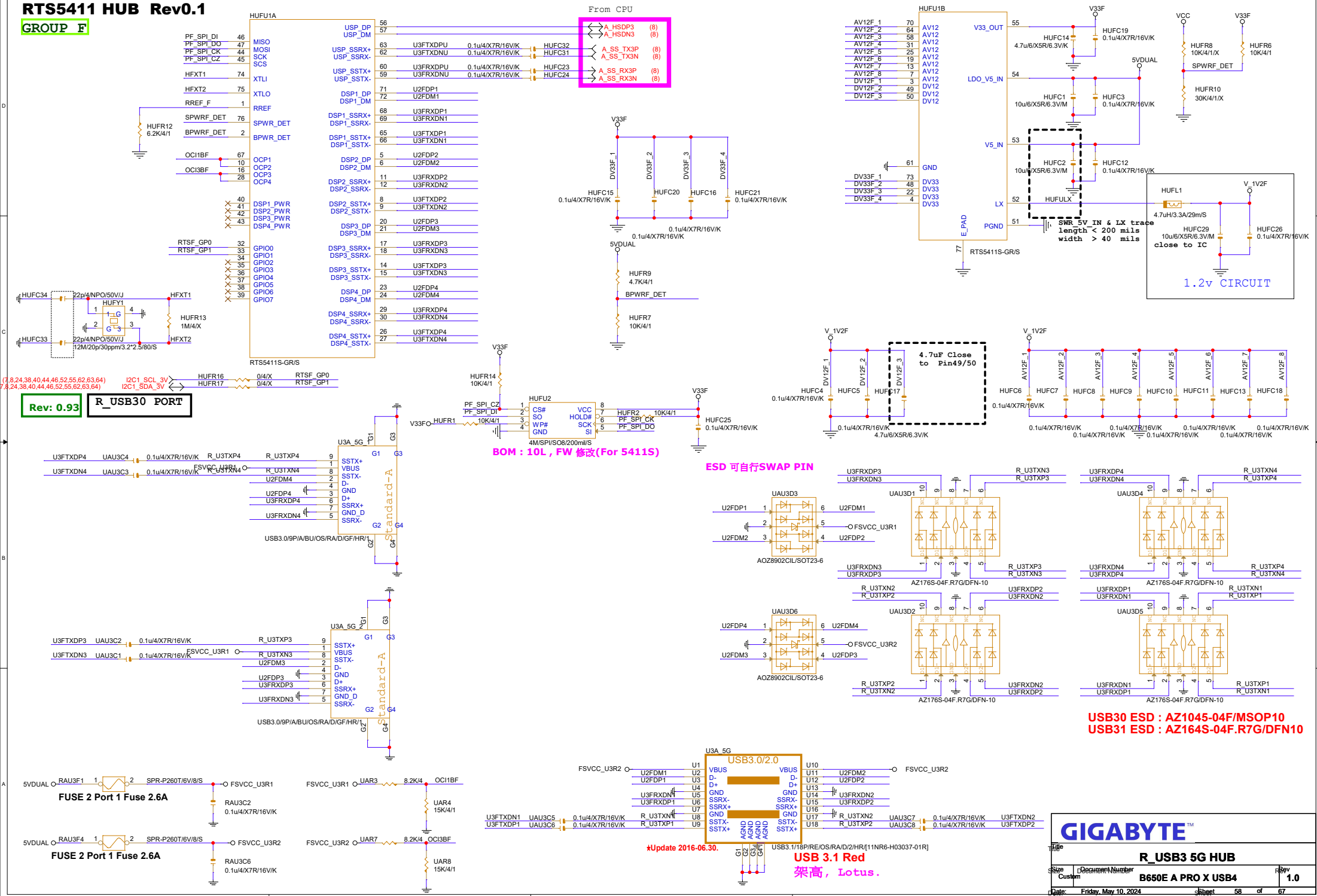


請放置CHOKE一出來位置,先預留.  
請自行確認ripple後再決定是否上件

Remote sense請從最重的負載端點拉回

GIGABYTE™			
File			
DDR PWR, 5VDUAL			
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**GROUP F**



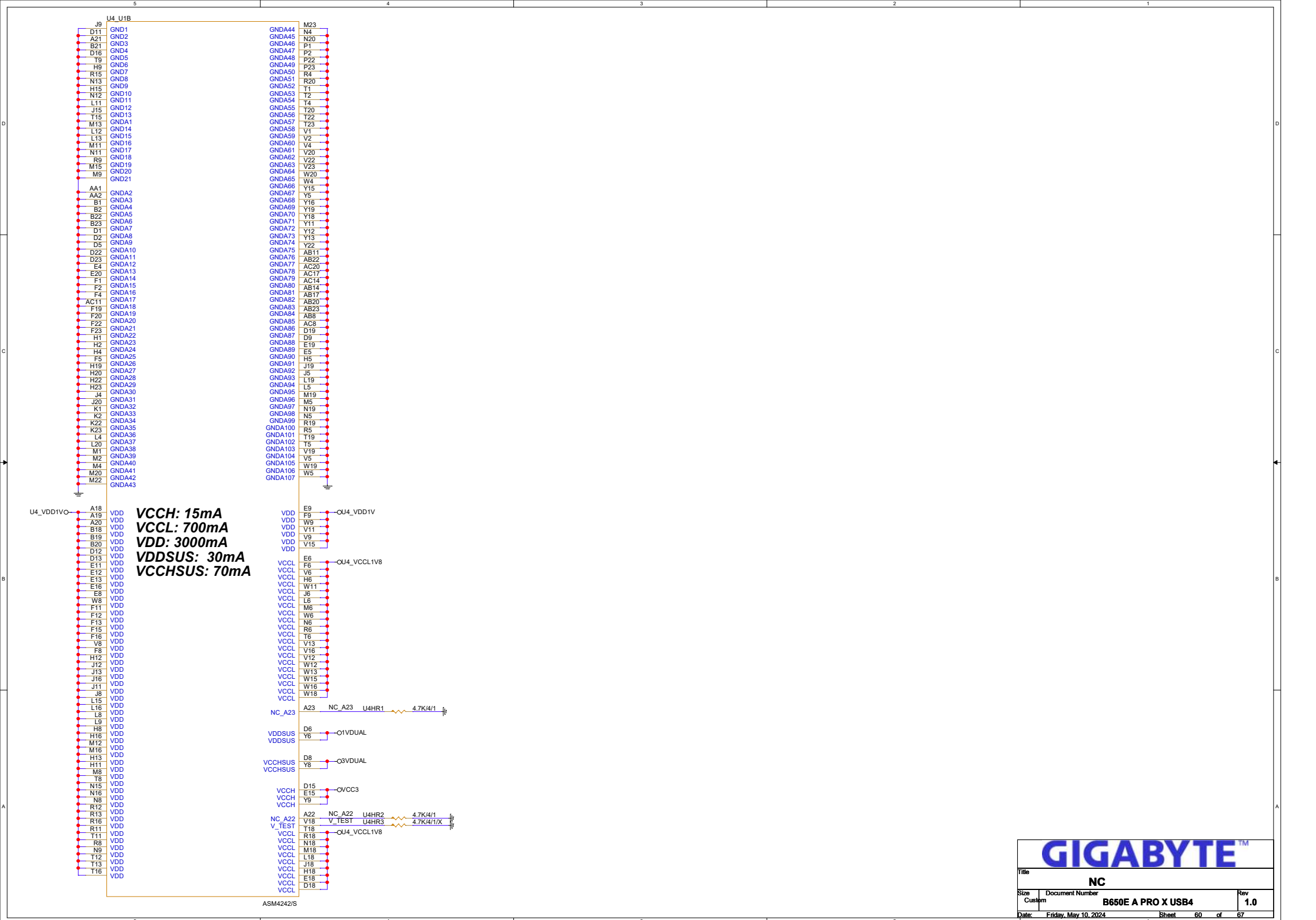
**GIGABYTE**

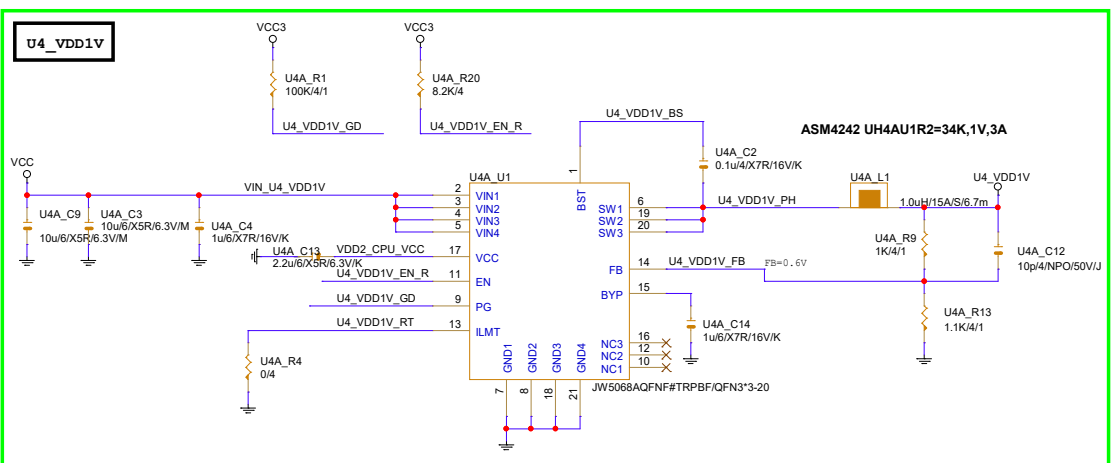
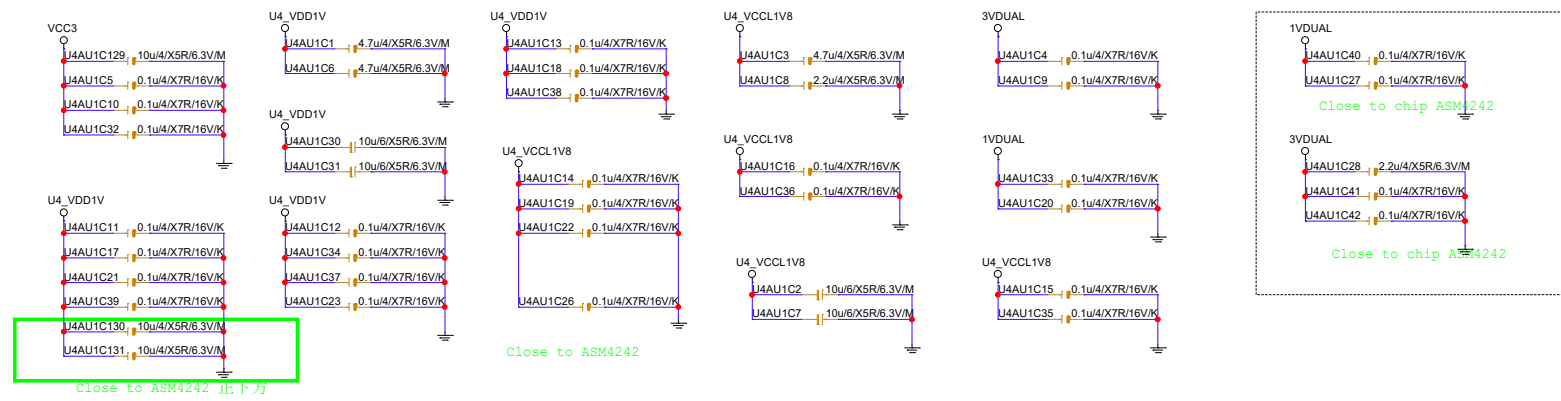
**R\_USB3 5G HUB**

**B650E A PRO X USB4**

Rev 1.







**POWER**

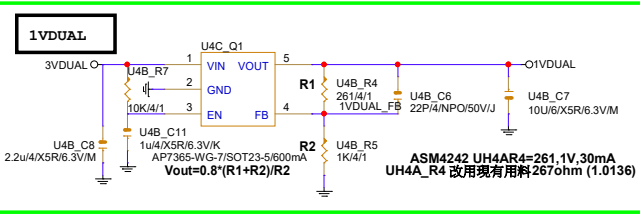
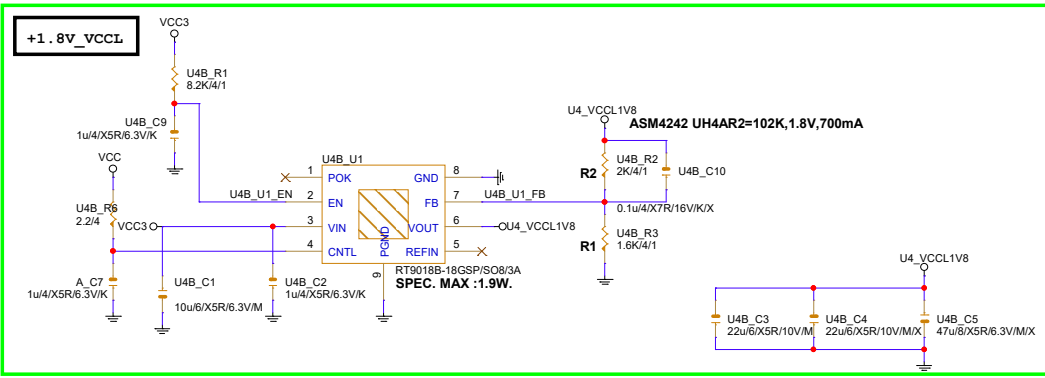
**+3.3V\_VCCH ----- 15mA**

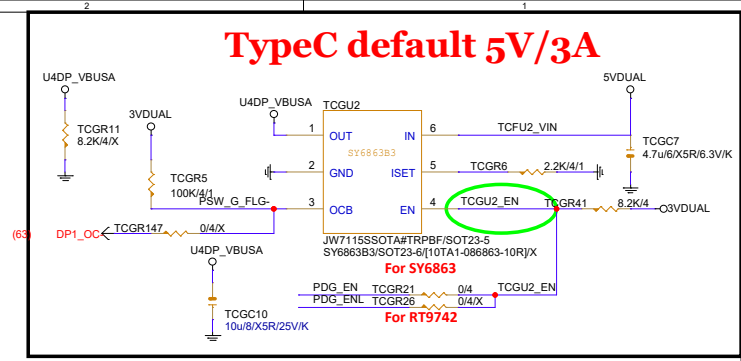
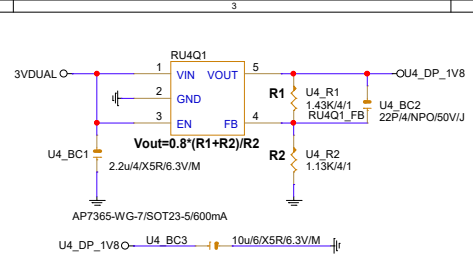
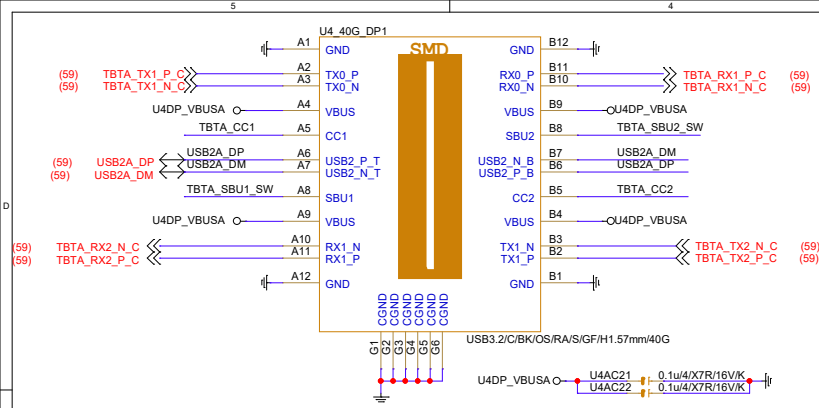
**+1.8V\_VCC1 ----- 700mA**

**+1V\_VDD ----- 3000mA**

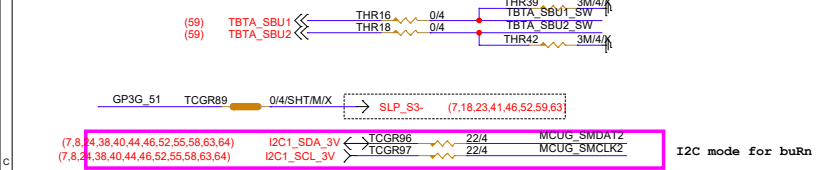
**VSUS\_1V ----- 30mA**

**VSUS\_3V3 ----- 70mA**

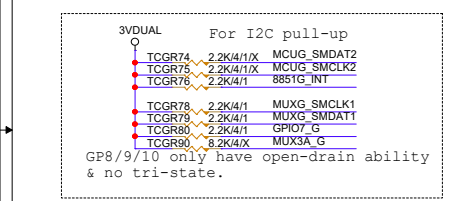
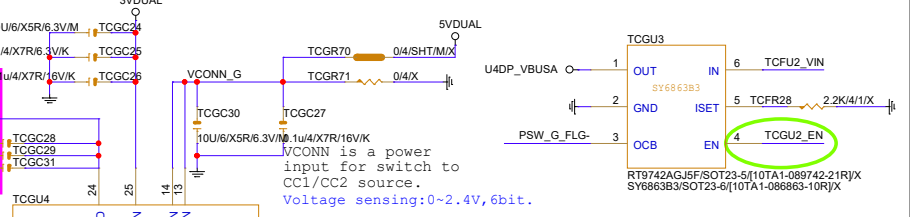




	TCGU2	TCGU3	TCGR13	TCGR14	TCGC10	TCGC7	TCGR147	TCGR11	TCGR5	TCGR41
SY6863B3	SY6863B3	NC	2.2K/4/1	NC	10u/8	4.7u/6	0/4	NC	100K/4/1	8.2K/4
RT9742A*1	RT9742A	NC	NC	NC	22u/8	10u/6	0/4/X	NC	100K/4/1	8.2K/4
RT9742A*2	RT9742A	NC	NC	NC	22u/8	10u/6	0/4/X	NC	100K/4/1	8.2K/4



TCGC28 ITE8851: 10u/6	TCGC28 & TCGC29 RTS5436I: NC
TCGC29 ITE8851: 1u/4	TCGC31 RTS5436I: 6.2K/4
TCGC31 ITE8851: 0.1u/4	



TCGR96/TCGR97 T8851FN-64/GX/S: 0/4 T8851FN/EX-GBA1: 22/4
TCGC35/TCGC34 T8851FN-64/GX/S: NC T8851FN/EX-GBA1: 47P/4

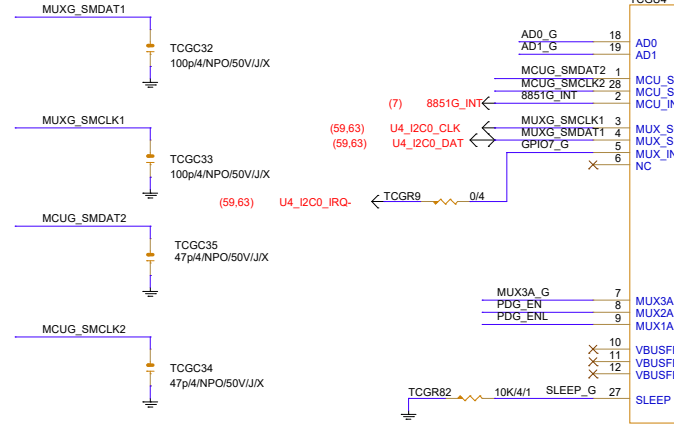
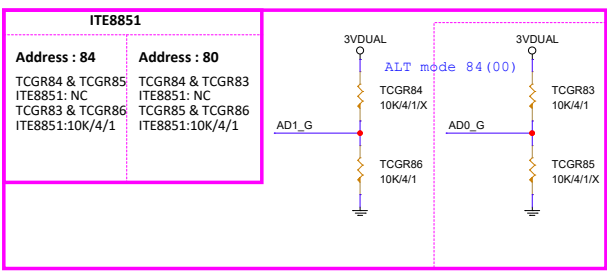
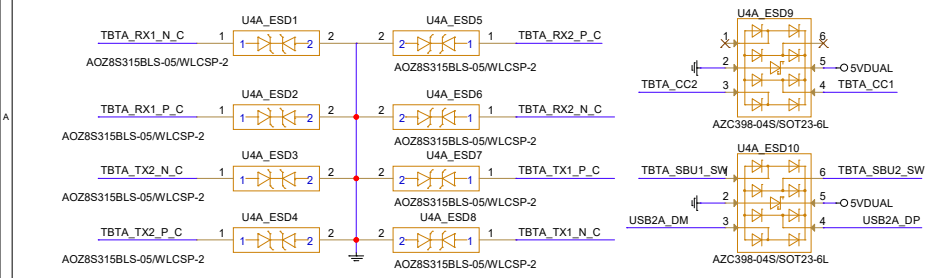
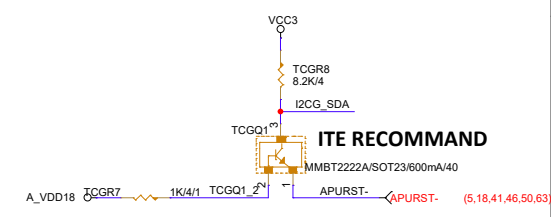
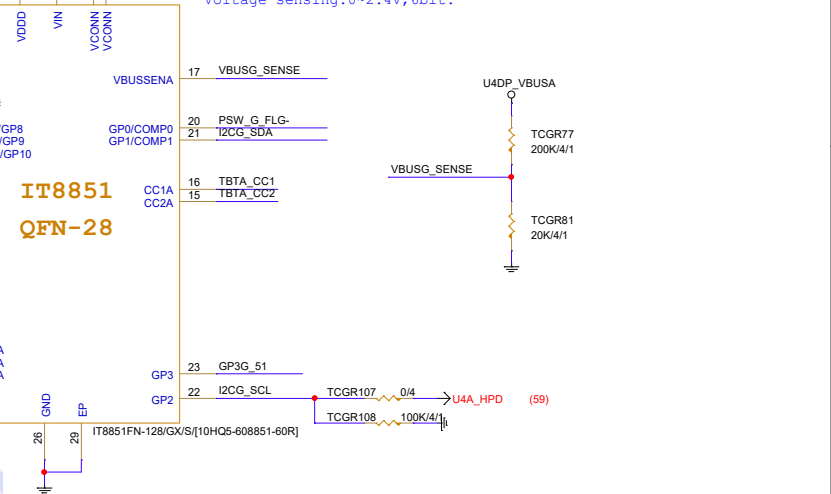
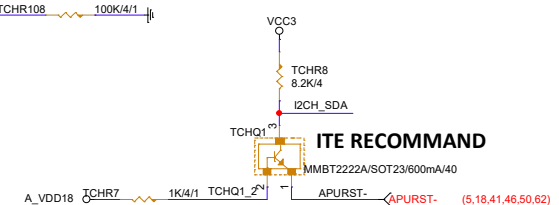
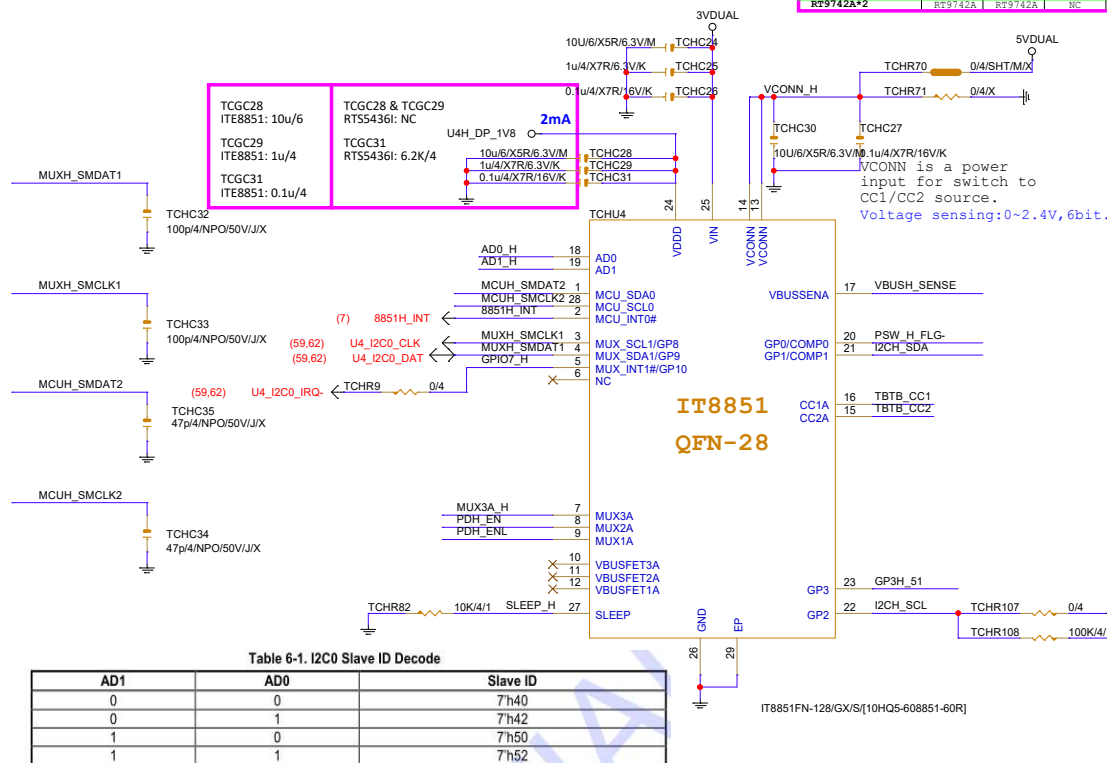
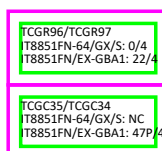
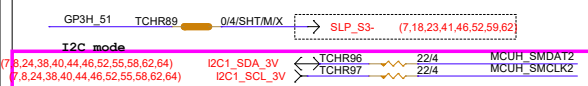
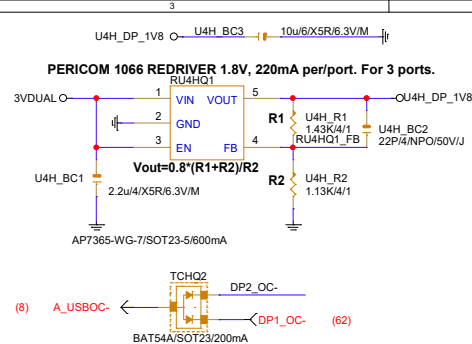
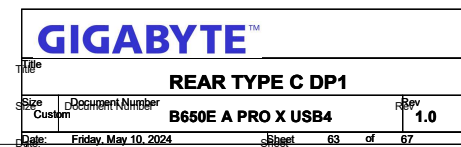
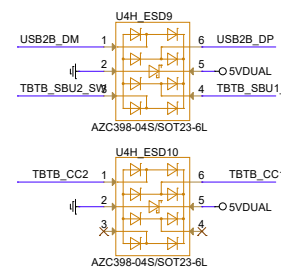
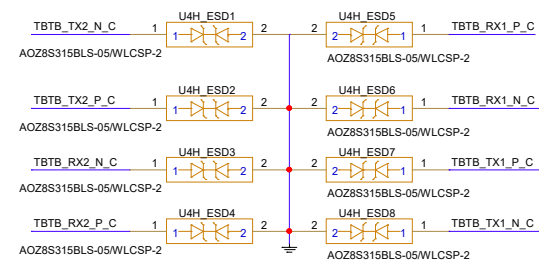


Table 6-1. I2C0 Slave ID Decode		
AD1	AD0	Slave ID
0	0	7'h40
0	1	7'h42
1	0	7'h50
1	1	7'h52





AD1	AD0	Slave ID
0	0	7h40
0	1	7h42
1	0	7h50
1	1	7h52



PCIE GEN 5 ACTITV MUX

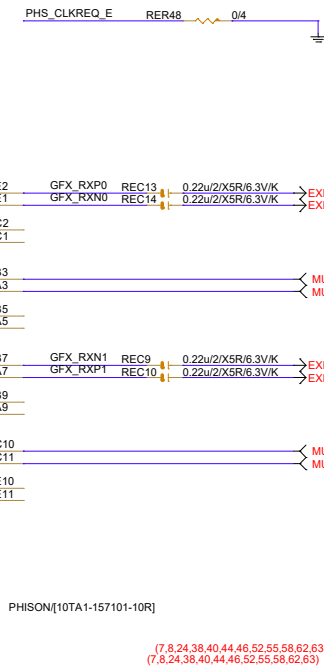
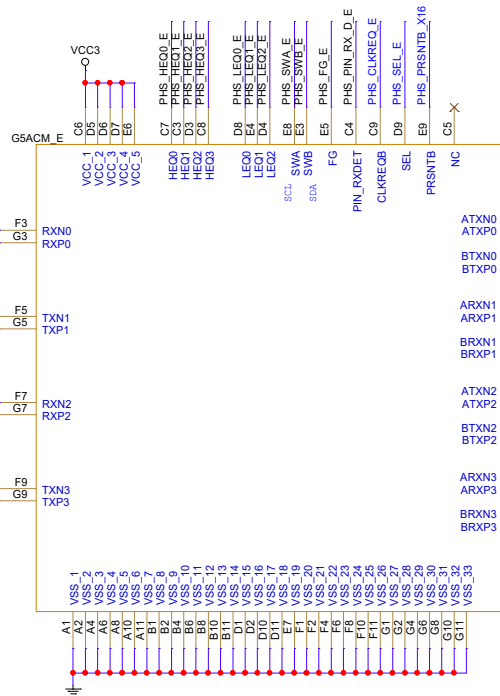
(16) MUX\_RXBP0  
(16) MUX\_RXBN0

(6) EXP\_A\_RXN3  
(6) EXP\_A\_RXP3  
CPU

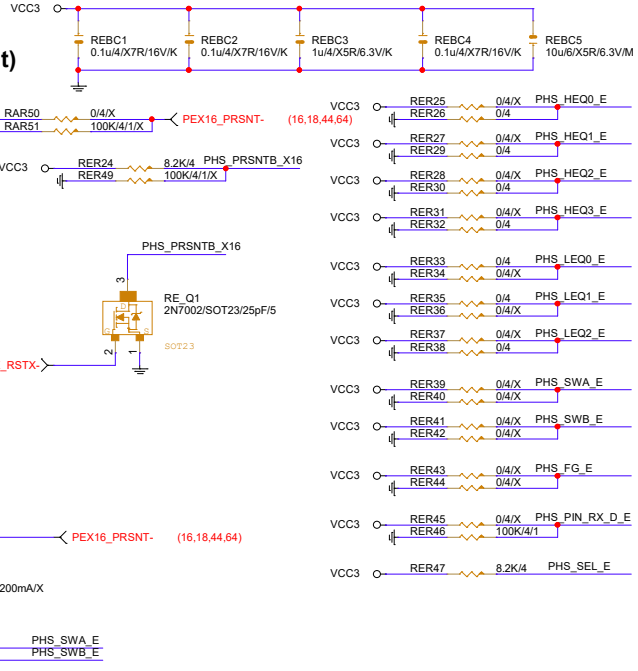
(16) MUX\_RXBN1  
(16) MUX\_RXBP1

(6) EXP\_A\_RXN2  
(6) EXP\_A\_RXP2  
CPU


EXP\_A\_RXP[0..3] >> EXP\_A\_RXP[0..3] (6)  
EXP\_A\_RXN[0..3] >> EXP\_A\_RXN[0..3] (6)



ADDRESS=0x60 (8 bit)







Title

NC

Size

Custom

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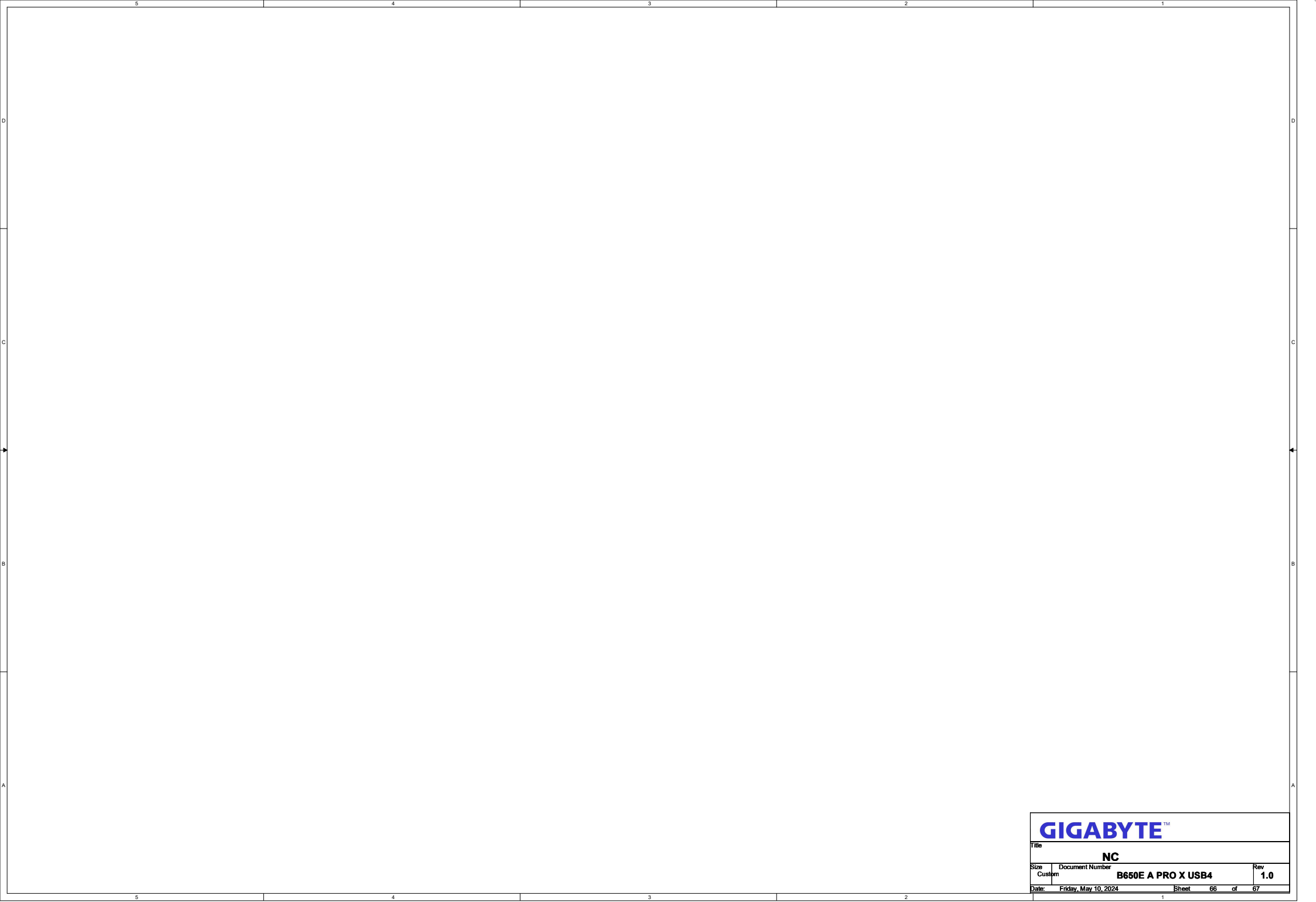
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D

D

C

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B


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A

A

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