SC87550AQ 36V / 65W Automotive Fully Integrated USB PD solution with Integrated Buck-boost Converter

1 Descriptions

The SC87550AQ is a fully integrated USB PD solution. It integrates a Buck-boost converter with 4 integrated power switches and a USB PD controller. The SC87550AQ operates over 4.5V to 36V wide input voltage and can output 3.3V to 22.5V voltage to support a variety of applications. It also supports up to 3.25A continuous output current under certain input supply range.

The SC87550AQ supports USB PD3.1 with PPS and backward supports DCP schemes for Battery Charging specification (BC1.2), The 3A Divider Mode. It also supports QC2.0/QC3.0, Huawei FCP as well.

The SC87550AQ's buck-boost converter employs current mode control scheme. The switching frequency could be set at 280kHz/420kHz/560kHz through I2C. The SC87550AQ also provides optional spread spectrum to optimize EMI performance.

The SC87550AQ supports a flexible power management state machine when the battery voltage is low, or the temperature is high. When two SC87550AQ are used in dual PD ports, the internal power sharing logic can smartly distribute the total power.

The SC87550AQ offers input over-voltage protection, output over-voltage protection, cycle-by-cycle current limit, DP/DM/CCx short to battery protection, output short circuit protection, average output current limit and thermal shutdown protection

The SC87550AQ is available in 22-pin 4mm X 5mm Wettable Flank QFN packages.

2 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: T_A range: -40°C to 125 °C
- Integrated 4-Power Switches Buck-boost Converter
- 4.5V to 36V start up input voltage, 40V ABS rating
- 3.3V to 22.5V output voltage range
- External High-side MOSFET parallel capability
- Support Type-C V2.0
- Support FC2.0/3.0 Specification, Huawei FCP
- Support USB PD3.1 V1.8 and PPS with 7 PDO list
- Support DCP schemes for BC1.2, 3A divider mode, and 1.2V/1.2V Mode
- Programmable Power Supply (PPS) support for USB power delivery
- +/- 3.3% accurate average output current limiting
- CV regulation accuracy +/- 25mA @ 12V –> 3.3V - 20V
- I2C Interface for:
  - 280k/420k/560kHz frequency selectable
  - Auto PFM / Forced PWM
  - Spread spectrum dithering
  - Line drop compensation
  - Current limit setting
- Battery short to ground protection driver
- CCx/DP/DM Short to VBAT(9-16V)/VOUT Protection
- I2C Slave Interface
- Programmable Power Management during low battery or high temperature
- Support two ports PD Power sharing
- Up to 120 Minutes EN off delay

3 Applications

- Automotive USB Charging
- Automotive USB Hub

4 Device Information

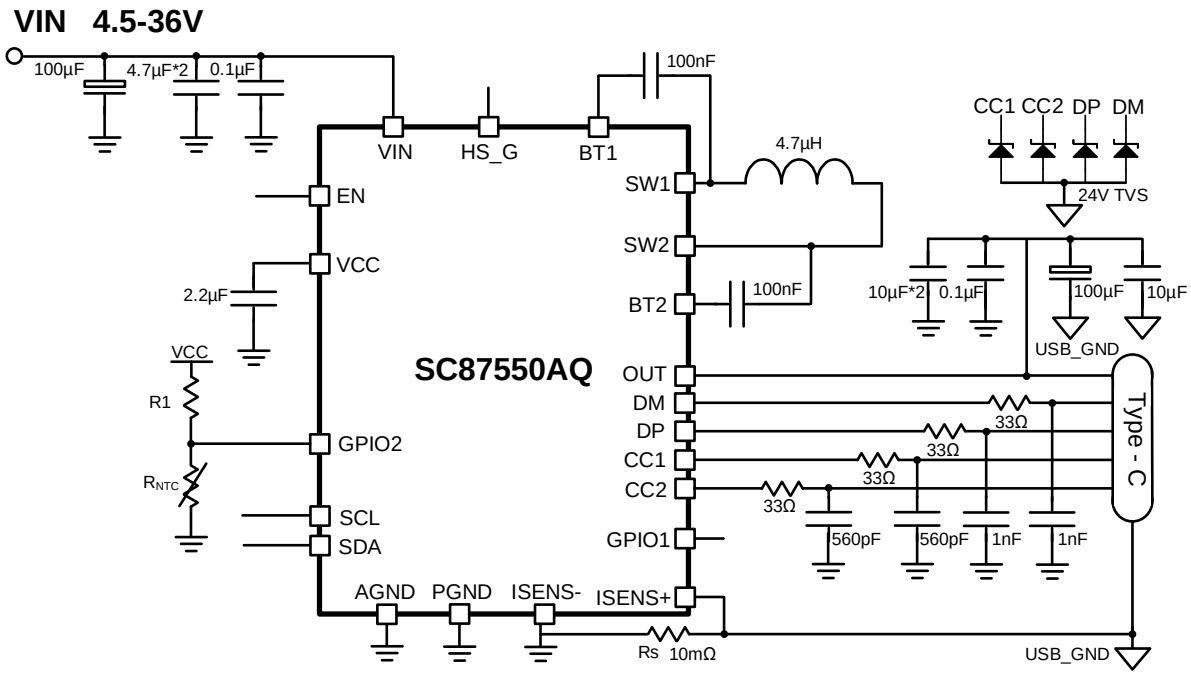
ORDER NUMBER	GPIO1	GPIO2	INPUT VOLTAGE OVP	PACKAGE	BODY SIZE
SC87550AQQFMR	NTC2	NTC	29.5V	22 pin QFN	4mm x 5mm x 0.85mm
SC87550BQQFMR	NTC2	Power Share2	29.5V	22 pin QFN	4mm x 5mm x 0.85mm

*Notes: The power derating strategy is different. Refer to **Table3** on Section15 for more information.

5 Revision History

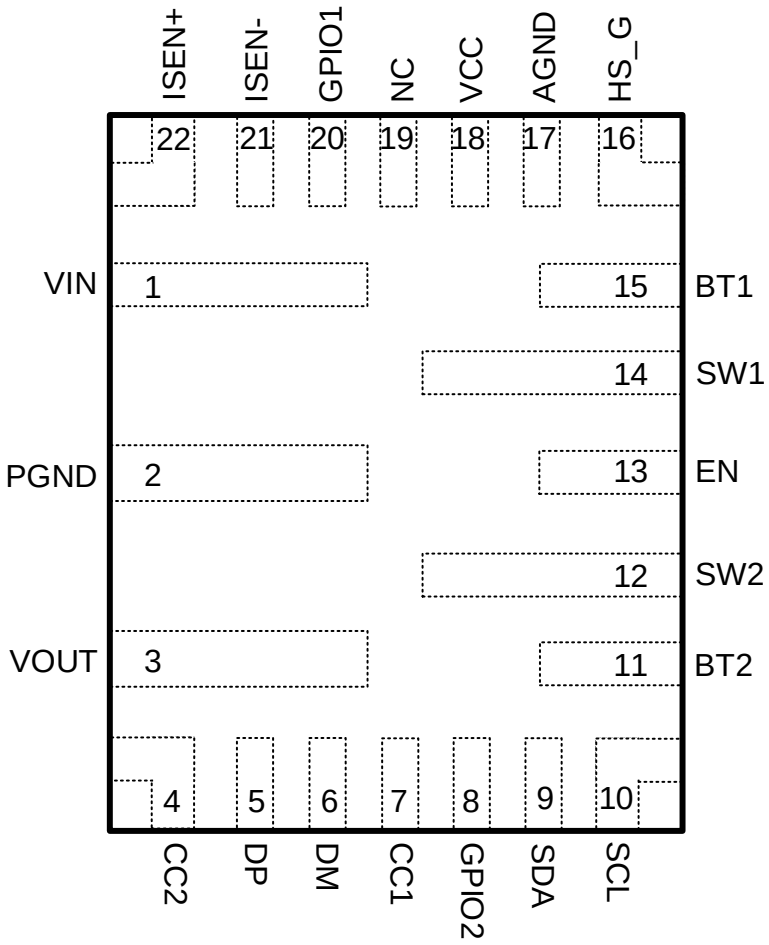
Revision	Date	Page(s) changed	Changes Description
V1.0.0	2024/12	NA	1.Initial Version

6 Typical Application Circuit



7 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VIN	I	Input power supply for the IC.
2	PGND	-	Power Ground. PGND requires extra care during PCB layout. Connect to PGND with copper traces and vias.
3	VOUT	O	Output of the buck-boost converter.
4	CC2	I/O	Type-C configure channel2. It also supports VCONN output

5	DP	I/O	DP is the input/output used to handshake with portable devices.	
6	DM	I/O	DM is the input/output used to handshake with portable devices.	
7	CC1	I/O	Type-C configure channel1. It also supports VCONN output	
8	GPIO2	O	POL	Type-C polarity indication, open drain. When CC1 is selected as CC line, the POL is pull-low; When CC2 is selected as CC line, the POL is open drain.
		I	NTC	NTC thermal sense input.
		I	VCONN_IN	1W VCONN power supply input.
		O	LED_PWM	Output a PWM driver to LED.
		O	Attach	Output to indicate device is attached or not. Active low.
		I	Power Share2	Power sharing 2 input, active high. When this pin voltage >1.87V, the PD power will be reduced to PS_PDP setting.
9	SDA	I	Data of I2C interface	
10	SCL	I	Clock of I2C interface	
11	BT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW2 pin.	
12	SW2	O	Switching node pin of the boost side. It is connected to the drain of the low-side power MOSFET and the source of high-side power MOSFET.	
13	EN	I	EN input. Apply logic high to enable the chip. EN pin has internal 6μA pull-up.	
14	SW1	O	Switching node pin of the buck side. It is connected to the drain of the low-side power MOSFET and the source of high-side power MOSFET.	
15	BT1	O	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW1 pin.	
16	HS_G	O	Gate driver output for high-side MOSFET in buck side	
17	AGND	-	Signal ground of the IC.	
18	VCC	O	Internal LDO regulator output. Decouple with a 2.2μF/0603 capacitor between this pin and the AGND pin.	
19	NC	-	Not connected.	
20	GPIO1	O	GATE	Gate drive pin to drive external MOSFET to do ground short to battery protection.
		I	Power_Share1	Power sharing 1 input.
		O	FAULT	Fault indication, open drain output. It indicates OCP, OTP, OVP, GND/DP/DM/CCx short to battery.
		I	NTC2	Secondary NTC detection input. When it triggers, PDP will reduce to power share set value.
		I	ATTACH_FLT	Attach and fault indicator, open drain output. It pull-low for 12μs when sink plug in if no fault event occurs. When fault happens, it pull-low.
		O	IMON	Current monitor output. Represent signal between ISENS+ and ISENS-.

21	ISEN-	I	Negative node of current sense signal input. An optional current sense resistor could be placed between PGND to output capacitor's GND.
22	ISEN+	I	Positive node of current sense signal input. An optional current sense resistor could be placed between PGND to output capacitor's GND.

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C ~ 150°C (unless otherwise noted). (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals (2)	VIN, EN, SW1	-0.3	40	V
	VOUT, SW2, CC1, CC2, DP, DM	-0.3	25	V
	HS_G	-0.3	VIN+12	V
	BST1	SW1-0.3	SW1+6	V
	BST2	SW2-0.3	SW2+6	V
	All other pins	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage (2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage (3), all pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range after start up	4.5		36	V
V_{OUT}	Output voltage range	3.3		22.5	V
F_{SW}	Buck switching frequency range	280	420	560	kHz
I_{OUT}	Output DC current range	0		3.25	A
L	Effective inductance range	3.3	4.7	6.8	µH
T_J	Operating junction temperature	-40		150	°C
T_A	Operating ambient temperature range	-40		125	°C

8.4 Thermal Information

THERMAL RESISTANCE		FCQFN22 (4mm x 5mm)	UNIT
$R_{\Theta JA}$	Junction to ambient thermal resistance (SC87550AQ EVM) (1)	26	°C/W
$R_{\Theta JA}$	Junction to ambient thermal resistance (JESD 51-7) (2)	35	°C/W
$R_{\Theta JC}$	Junction to case resistance (2)	13	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance (2)	3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (2)	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (2)	2.9	°C/W

(1) Measured on SC87550AQ EVM. 4-layer, 2oz Cu per top and bottom layer and 1oz Cu per inner layer.

(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.

8.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{IN} = 12V and V_{OUT} = 20V, V_{EN} = Float. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		4.3	4.5	V
		V_{IN} falling		4.1	4.3	V
I_Q	Quiescent current when no device attached	I2C set EN='1b'		210	240	μA
	Quiescent current when device attached	I2C set EN ='1b', CC attached, No switching, no load.		1.5		mA
I_{SD}	Shutdown current into the VIN pin	IC disabled, V_{EN}=0V		25	65	μA
V_{CC}	Internal regulator output		4.8	5.0	5.2	V
EN						
$V_{EN\_VCC\_H}$	EN input level to turn on internal LDO	Rising threshold			1.03	V
$V_{EN\_VCC\_L}$	EN input level to turn off internal LDO	Falling threshold	0.4			V
V_{EN_H}	EN input level to start switching	Rising threshold	1.2	1.26	1.32	V
V_{EN_L}	EN input level to stop switching	Falling threshold	0.96	1.00	1.04	V
MOSFETS						
R_{DSON_A}	High-side MOSFET on resistance on buck side			10	20	mΩ
R_{DSON_B}	Low-side MOSFET on resistance on buck side			20	40	mΩ
R_{DSON_C}	High-side MOSFET on resistance on boost side			7	14	mΩ

R_{DSON_D}	Low-side MOSFET on resistance on boost side			7	14	mΩ
External High-side driver						
R_{BUCK_UP}	Buck High side driver pull up resistor			2.2		Ω
R_{BUCK_DN}	Buck High side driver pull down resistor			1		Ω
BOOT UVLO						
$V_{BOOT1\_OK\_F}$	Falling voltage on BT1 pin compared to SW1 which will turn off high-side switch			2.3		V
$V_{BOOT1\_OK\_R}$	Rising voltage on BT1 pin compared to SW1 which will turn on high-side switch			2.5		V
$V_{BOOT2\_OK\_F}$	Falling voltage on BT2 pin compared to SW2 which will turn off high-side switch			2.3		V
$V_{BOOT2\_OK\_R}$	Rising voltage on BT2 pin compared to SW2 which will turn on high-side switch			2.5		V
REFERENCE						
V_{OUT1}	Output Voltage	VDAC=250mV	4.9	5.0	5.1	V
V_{OUT2}		VDAC=600mV	11.9	12.0	12.1	V
V_{OUT3}		VDAC=1000mV	19.85	20.0	20.15	V
OVER VOLTAGE PROTECTION						
$V_{OUT\_OVP\_R}$	Output OVP rising (V_{REF}>0.25V)	V_{REF} =0.6V	115%	120%	125%	V_{FB}
$V_{OUT\_OVP\_F}$	Output OVP falling (V_{REF}>0.25V)		110%	115%	120%	V_{FB}
$V_{OUT\_OVP\_ABS}$	Output absolute OVP rising		24.3	24.8	25.3	V
$V_{OUT\_OVP\_HYS}$	Output voltage protection hysteresis			1.1		V
V_{OVLO_R1}	Voltage on VIN pin to stop buck-boost switching		28.5	29.5	30.5	V
V_{OVLO_R2}	Voltage on VIN pin to stop buck-boost switching		16.5	17.2	17.9	V
V_{OVLO_HYS}	Input voltage protection hysteresis			1.2		V
R_{DIS}	Output discharge resistor			320		Ω
INTERNAL CLOCK						
F_{SW1}	Oscillator frequency			280		kHz
F_{SW2}				420		
F_{SW3}				560		
T_{ON_MIN}	Min on time	Boost low side MOSFET		75		ns
T_{OFF_MIN}	Min off time	Buck low side MOSFET		75		ns
SPREAD SPECTRUM						

F_{SRANGE}	Frequency span of spread spectrum operation - deviation from center frequency			8		%
SOFT START						
T_{SS}	Soft Start Time	For $5V_{OUT}$ condition		0.8		ms
CURRENT LIMIT						
I_{SENS1}	Current loop accuracy	OC threshold=1A, R_{SENSE}=10mΩ	0.85	1	1.15	A
I_{SENS2}		OC threshold=3A, R_{SENSE}=10mΩ	2.9	3	3.1	A
I_{LIMIT1_FPWM}	Buck low-side valley current limit		5.5	6.5	7.5	A
I_{LIMIT2_FPWM}	Boost low-side peak current limit		9	10.5	12.5	A
ZCD	Zero cross			-30		mA
LINE DROP COMPENSATION						
V_{DROP}	Line drop compensation	Set LDC_GAIN=01b, R_{SENSE}=10mΩ, IOUT=3A		100		mV
		Set LDC_GAIN=10b, R_{SENSE}=10mΩ, IOUT=3A		300		mV
		Set LDC_GAIN=11b, R_{SENSE}=10mΩ, IOUT=3A		600		mV
		Set Additional_LDC=1b, LDC_GAIN=11b, R_{SENSE}=10mΩ, IOUT=3A		800		mV
VBUS_UV						
V_{BUS_UV}	V_{BUS_UV} falling voltage			2.7	2.9	V
HICCUP						
T_{HICCUP}	Hiccup on timer			5		ms
	Hiccup off timer			100		ms
V_{HICCUP}	Hiccup Voltage Threshold			0.8		V
MODE TRANSITION						
V_{MODE_TH1}	Buck-boost to buck transition threshold	VIN/VOUT		120		%
V_{MODE_TH2}	Buck-boost to boost transition threshold	VIN/VOUT		85		%
I2C INTERFACE						
V_{IH}	Input logic high				1.3	V
V_{IL}	Input logic low		0.4			V
NTC, NTC2						

V_{NTC_ETY}	External thermal sense trigger voltage			10%		VCC
V_{NTC_RCY1}	External thermal sense recover voltage 1	I2C set NTC_HYS='0b'		20%		VCC
V_{NTC_RCY2}	External thermal sense recover voltage 2	I2C set NTC_HYS='1b'		30%		VCC
GPIO1 – GATE - BATTERY SHORT TO GROUND						
I_{SC}	GND short to battery ISENS threshold	OC threshold=20A, R_{SENSE}=5mΩ		100		mV
		OC threshold=20A, R_{SENSE}=10mΩ		200		mV
GPIO1 – Power Share 1						
V_{IH_PS}	Power share input high		1.5			V
V_{IL_PS}	Power share input low				0.4	V
R_{LKG_PS}	Power Share Pull up resistance			1		MΩ
GPIO1 – FAULT1						
R_{PD_FAULT}	Fault pull-down resistor				40	Ω
I_{LKG_FAULT}	Fault Leakage				3	μA
GPIO2 – POL						
R_{PD_POL}	POL pull-down resistor				40	Ω
I_{LKG_POL}	POL Leakage				3	μA
GPIO2 – LED						
f_{LED}	LED PWM output frequency		20	25	30	kHz
D_{LED}	LED PWM output duty cycle			50		%
Current Monitor Function						
G_{IMON1}	IMON output voltage gain	I2C set R_{SENS}=5mΩ, I_{OUT}=3A		60		V/V
G_{IMON2}		I2C set R_{SENS} =10mΩ, I_{OUT}=3A		30		V/V
GPIO1 – NTC2						
V_{NTC_ETY}	External thermal sense trigger voltage			10%		VCC
V_{NTC_RCY1}	External thermal sense recover voltage 1	I2C set NTC_HYS='0b'		20%		VCC
V_{NTC_RCY2}	External thermal sense recover voltage 2	I2C set NTC_HYS='1b'		30%		VCC
BC1.2 DCP MODE						
R_{DP/DM_SHORT}	DP and DM short resistance	V_{DP} = 0.8V, I_{DM} = 1mA, TJ = -40°C to +150°C			50	Ω
V_{DP/DM_OVP_TH}	DP and DM over-voltage threshold		3.8	4	4.2	V
3A DIVIDER MODE						
$V_{DP\_DIVIDER}$	DP output voltage			2.7		V
$R_{DP\_DIVIDER}$	DP output impedance			30		kΩ
$V_{DM\_DIVIDER}$	DM output voltage			3.3		V

$R_{DM\_DIVIDER}$	DM output impedance			30		kΩ
1.2V/1.2V MODE						
$V_{DP/DM\_1p2\ mode}$	DP/DM output voltage		1.12	1.2	1.28	V
$R_{DP/DM\_1p2\ mode}$	DPDM output impedance		80	100	120	kΩ
QUICK CHARGE 3.0 MODE						
V_{QC_LOW}	DP/DM low voltage	`	0.3	0.35	0.4	V
V_{QC_HIGH}	DP/DM high voltage		2.1	2.2	2.3	V
R_{DP_QC}	Resistance pull down on DP			20		kΩ
R_{DM_QC}	Resistance pull down on DM			20		kΩ
$R_{DP\_500K\_PD}$	Resistance pull down on DP			500		kΩ
$R_{DM\_500K\_PD}$	Resistance pull down on DM			500		kΩ
t_{GLITCH_DM}*	DM low glitch time			1		ms
t_{GLITCH_DP}*	DP high glitch time			1200		ms
$t_{GLITCH\_V\_CHANGE\_QC2}$*	Output voltage change glitch time			40		ms
$t_{GLITCH\_V\_CHANGE\_QC3}$*	Output voltage change glitch time			60		ms
$V_{BUS\_CONT\_STEP}$	Bus voltage (VBUS) step			200		mV
VBUS SLEW RATE						
$t_{SLEWRATE}$	Rising slew rate for VBUS			0.1		mV/μs
	Falling slew rate for VBUS			0.1		mV/μs
CDP MODE						
V_{DM_SRC}	DM CDP output voltage	DM data output high, VBUS >=3.3V	0.6	0.65	0.7	V
		DM data output low			20	mV
V_{DA_REF}	DP rising lower window threshold for V_{DM_SRC}	Force DM>0.4V, DM output low, measure sink current		0.35		V
V_{LGC_SRC}	DP rising upper window threshold for VDM_SRC		0.9	1	1.1	V
$t_{IN\_CDP\_START\_DEGH}$*	CDP_DET mode、DP_PU DET mode to CDP_start mode deglich			4		ms
$t_{IN\_CDP\_DET\_DEGH}$*	CDP_START mode、DP_PU DET mode to CDP_start mode deglich			10		ms
$t_{IN\_DPPU\_DET\_DEGH}$*	CDP_START mode、CDP_start mode to DP_PU DET mode deglich			2		ms
FCP MODE						
V_{DATA_HIGH}	DM data output high voltage	DM data output high, VBUS ≥ 3.3V	3	3.3	3.6	V

I_{DM_HIGH}	DM output high capability	Force DM < 2.9V, DM output high, measure source current	5			mA
I_{DM_LOW}	DM output low sink capability	Force DM>0.4V, DM output low, measure sink current	2		6	mA
V_{IH_TH}	DM input data rising threshold		1.1	1.2	1.3	V
V_{IL_TH}	DM input data falling threshold		0.9	1	1.1	V
t_{RX_PING}*	PING length			2.56		ms
$t_{RX\_UI/4}$*	UI/4 length		33		47	μs
t_{TUI}/t_{RUI}*				100		%
USB Type-C						
R_{p_180uA}	CC Rp pull up 180μA capabilitiy		165.6	180	194.4	μA
R_{p_330uA}	CC Rp pull up 330μA capabilitiy		303.6	330	356.4	μA
$t_{CC\_DEBOUNCE\_F}$*	CC voltage falling debounce timer			150		mS
$t_{CC\_DEBOUNCE\_R}$*	CC voltage rising debounce timer			10		mS
P_{CONN}	V_{CONN} output power		1			W
I_{VCONN_OCP1}	Internal V_{CONN} over current threshold		30	35		mA
I_{VCONN_OCP2}	Internal V_{CONN} over current threshold		200			mA
$t_{VCONN\_OC\_DEG}$*	Internal VCONN over-current deglitch time			24		μs
V_{CCOVP_TH}	CC OVP rising threshold		5.7	6	6.3	V
V_{CCOVP_HYST}	CC OVP hysteresis			0.26		V
$f_{BITRATE}$*	Bit rate		270		330	kbps
$p_{BitRate}$*	Maximum difference between the bitrate during the part of the packet following the Preamble and the reference bitrate.				0.25	%
$t_{EndDriveBMC}$*	Time to cease driving the line after the end of the last bit of the Frame.				23	μs
$t_{InterFrameGap}$*	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble		25			μs
t_{RISE}*	Rise time	C = 330pF	300			ns
t_{FALL}*	Fall time	C = 330pF	300			ns
Z_{Driver}*	PD data Tx output impedance			66		Ω
V_{Swing}	High level voltage for CC PD data		1.05	1.125	1.2	V
THERMAL SHUTDOWN						
T_{SD}*	Thermal shutdown temperature	TJ rising		165		°C
	Thermal shutdown hysteresis	TJ falling below T_{SD}		20		°C

* Guarantee by Design

8.6 Typical Characteristics

V_{IN}=12V, V_{OUT}=5V, L=4.7μH, F_{SW}=420kHz, mode=FPWM with spread spectrum, T_A=25°C, unless otherwise noted.

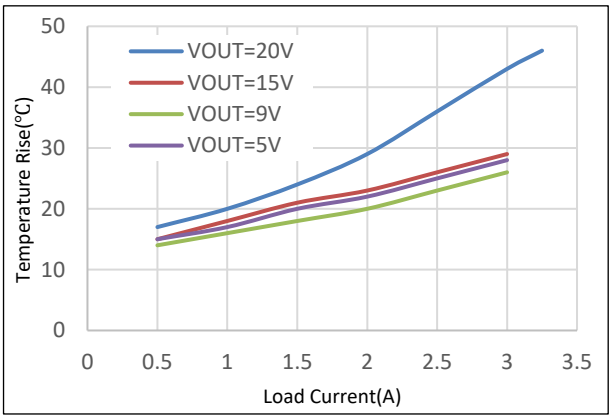


Figure 8-1. Case Temperature Rise, disable external Q1, DCR=9mR

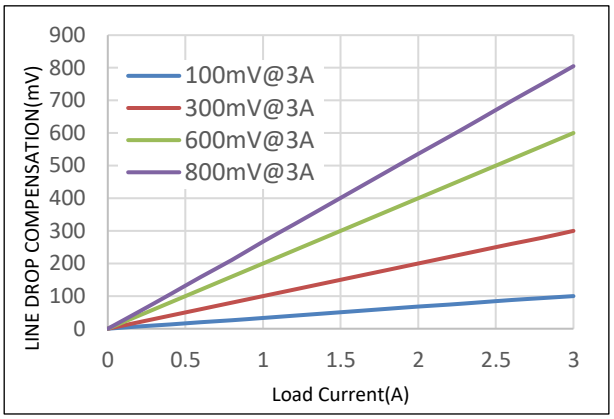


Figure 8-2. Line Drop Compensation

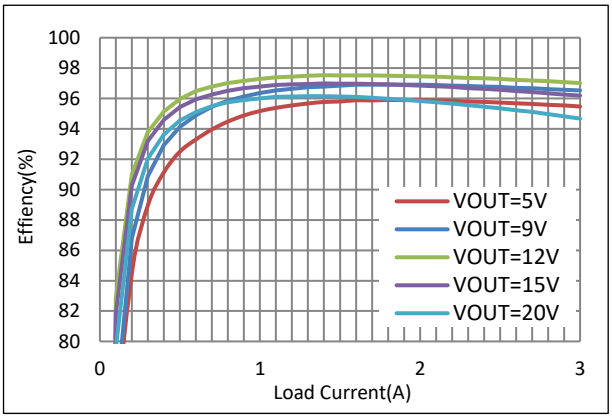


Figure 8-3. Effiency,V_{IN}=9V, disable external Q1, DCR=9mR

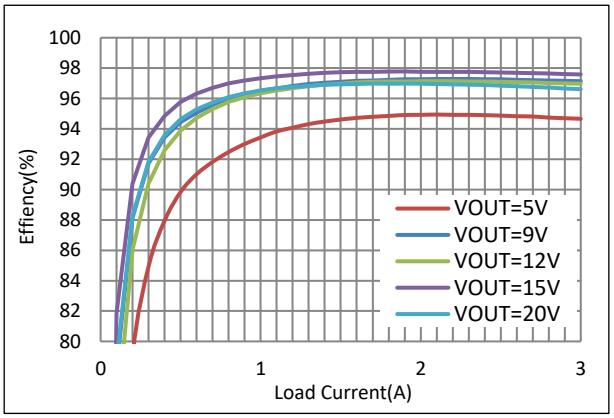


Figure 8-4. Effiency,V_{IN}=12V, disable external Q1, DCR=9mR

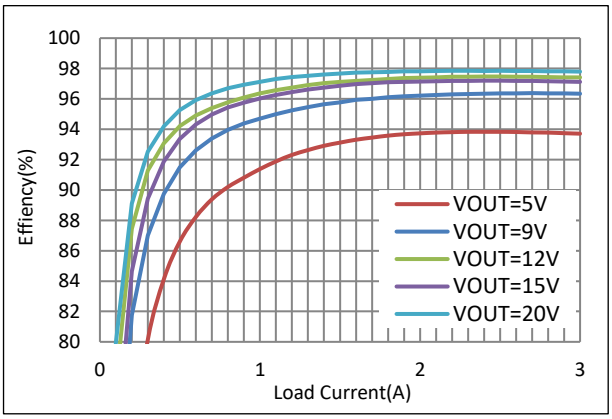


Figure 8-5. Effiency,V_{IN}=16V, disable external Q1, DCR=9mR

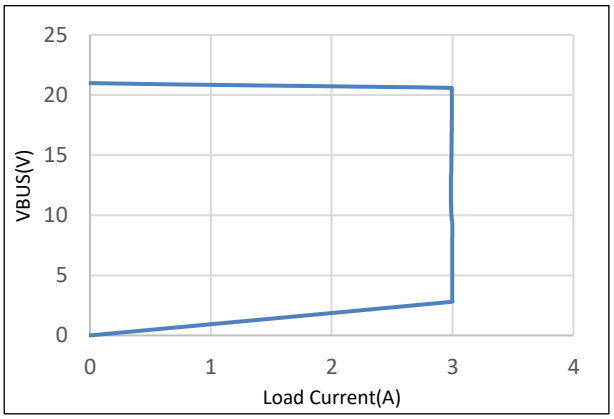


Figure 8-6. CC/CV Curve

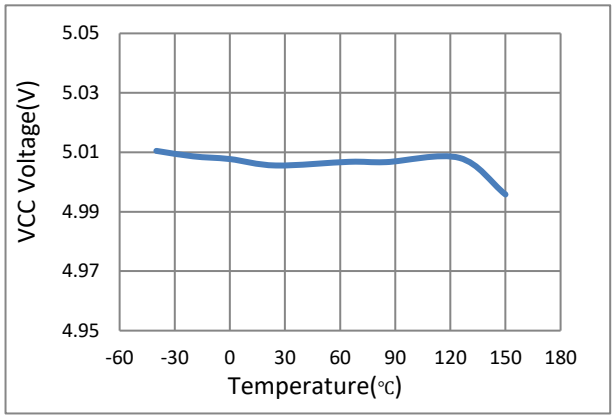


Figure 8-7. VCC Voltage

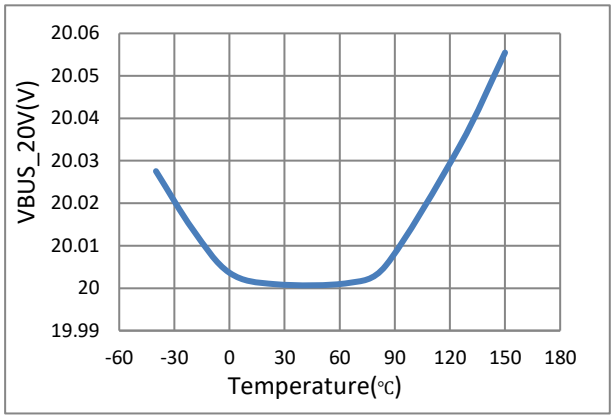


Figure 8-8. V_{BUS} Voltage-20V

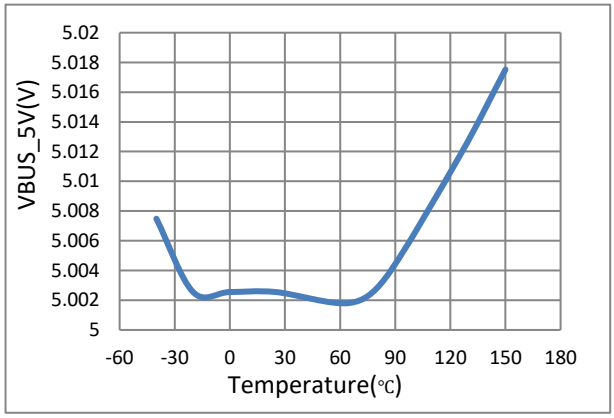


Figure 8-9. V_{BUS} Voltage-5V

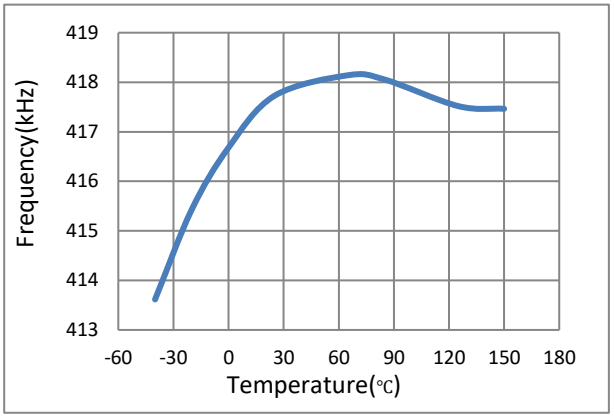


Figure 8-10. Switching Frequency

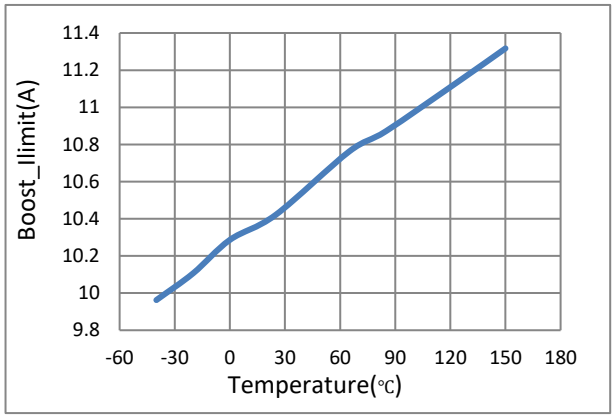


Figure 8-11. Boost low-side peak current limit1

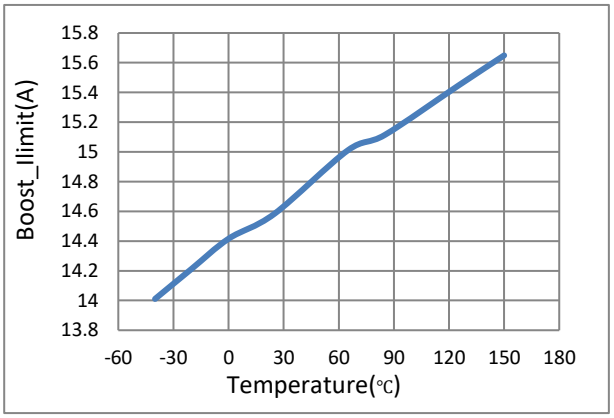


Figure 8-12. Boost low-side peak current limit2

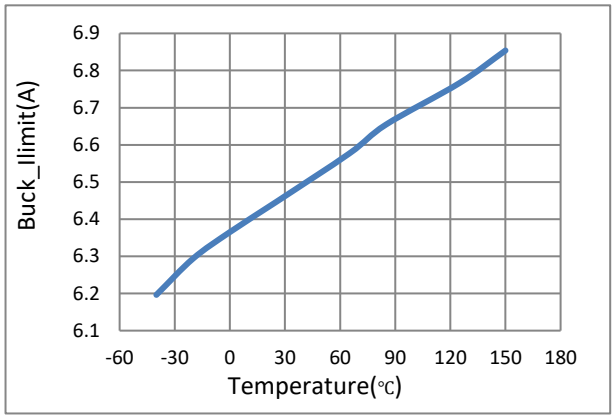


Figure 8-13. Buck low-side valley current limit

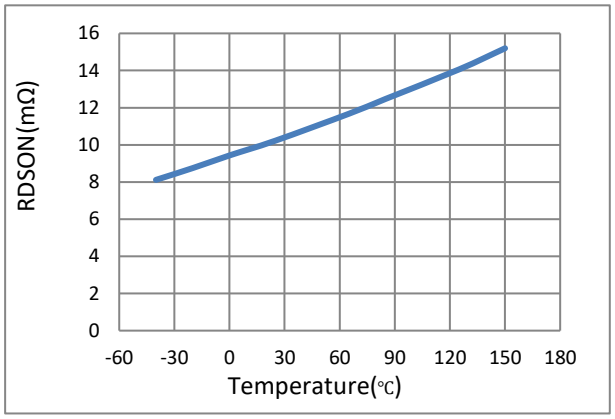


Figure 8-14. Buck high-side fet on-resistance

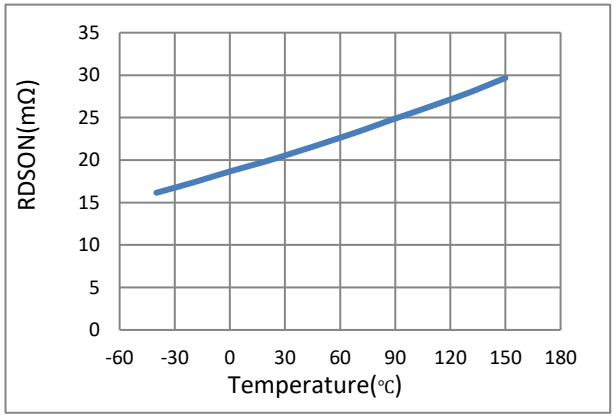


Figure 8-15. Buck low-side fet on-resistance

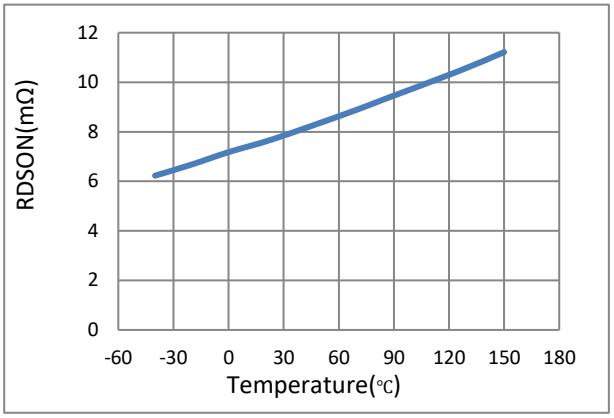


Figure 8-16. Boost high-side fet on-resistance

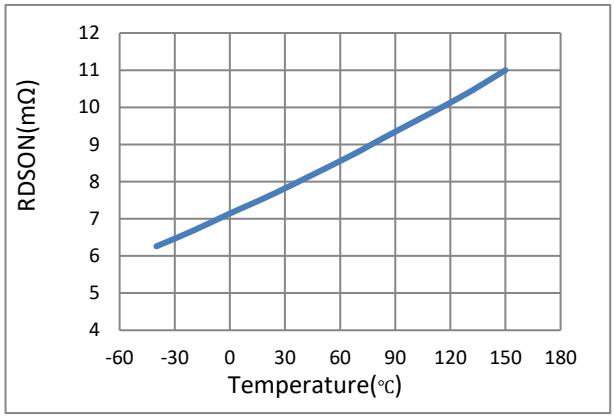


Figure 8-17. Boost low-side fet on-resistance

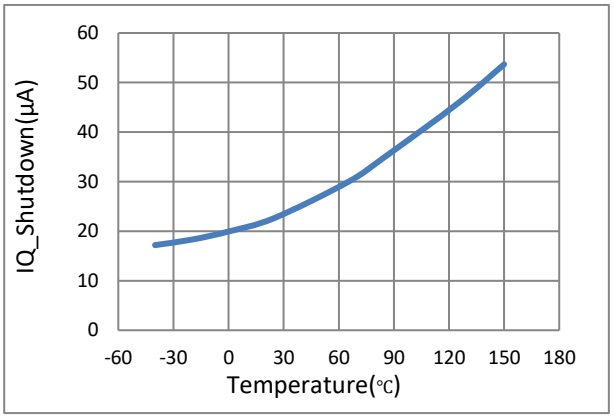


Figure 8-18. IQ Shutdown

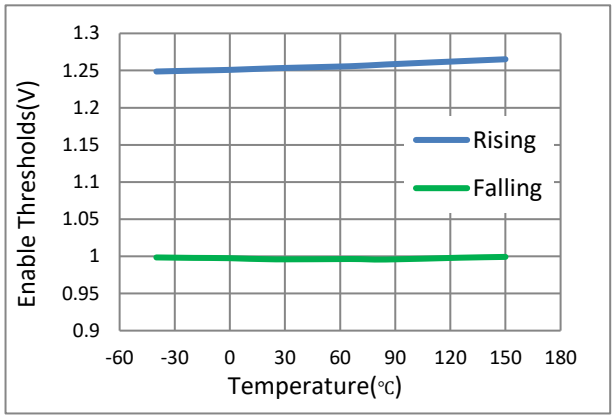


Figure 8-19. Enable Thresholds

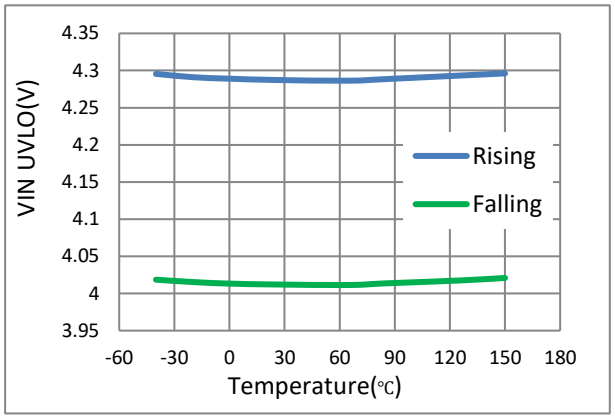


Figure 8-20. VIN UVLO

8.7 Typical Performance Characteristics

V_{IN}=12V, V_{OUT}=5V, L=4.7µH, F_{SW}=420kHz, mode=FPWM with spread spectrum, T_A=25°C, unless otherwise noted.

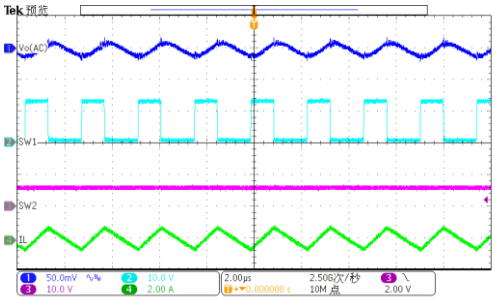


Figure 8-21. Steady State, V_{OUT}=5V, I_{OUT} =0A

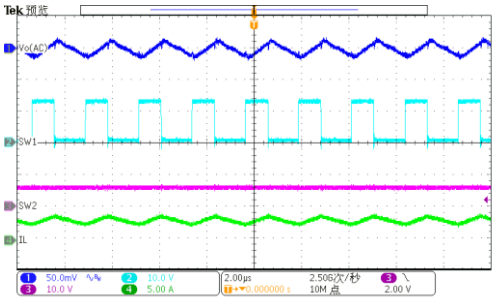


Figure 8-22. Steady State, V_{OUT}=5V, I_{OUT} =3A

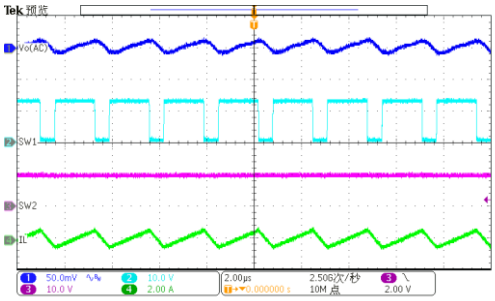


Figure 8-23. Steady State, V_{OUT}=9V, I_{OUT} =0A

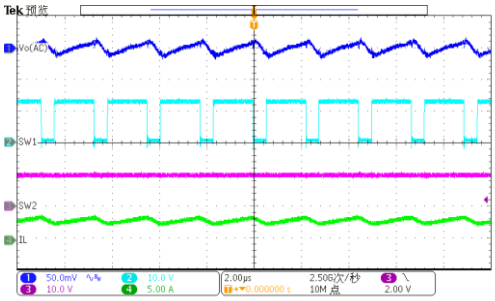


Figure 8-24. Steady State, V_{OUT}=9V, I_{OUT} =3A

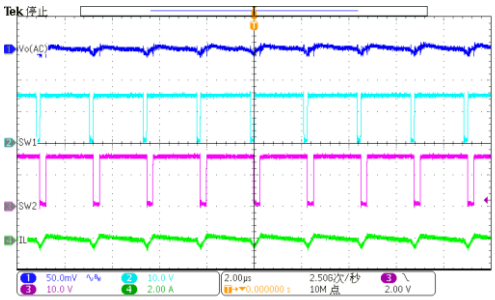


Figure 8-25. Steady State, V_{IN}=14V, V_{OUT}=15V, I_{OUT} =0A

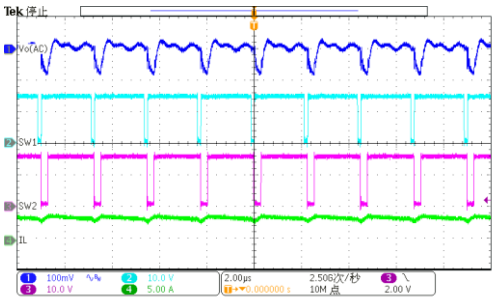


Figure 8-26. Steady State, V_{IN}=14V, V_{OUT}=15V, I_{OUT} =3A

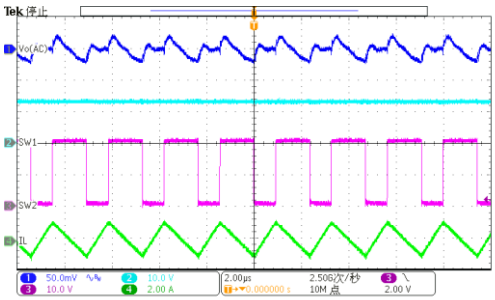


Figure 8-27. Steady State, V_{OUT}=20V, I_{OUT} =0A

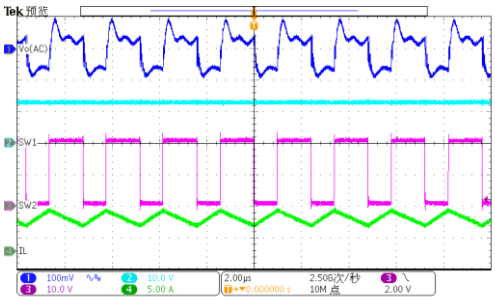


Figure 8-28. Steady State, V_{OUT}=20V, I_{OUT} =3A

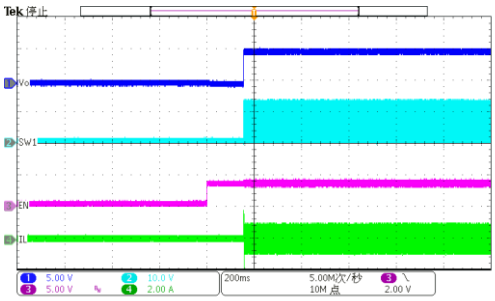


Figure 8-29. Start up through EN; I_{OUT} =0A

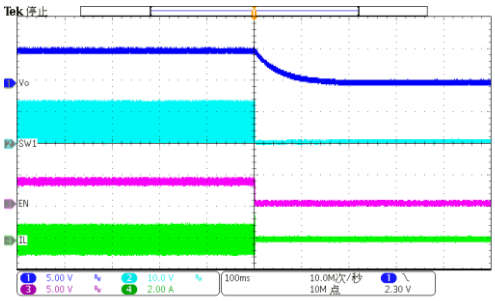


Figure 8-30. Shut down through EN; I_{OUT} =0A

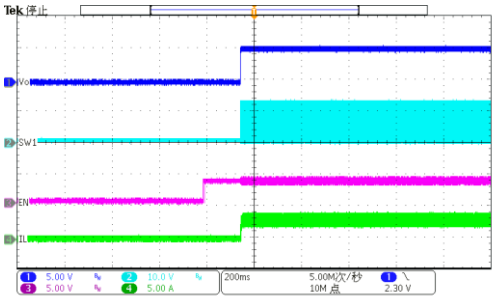


Figure 8-31. Start up through EN; I_{OUT} =3A

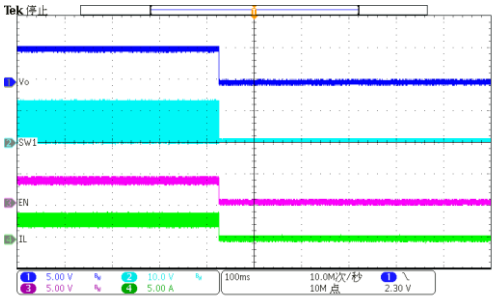


Figure 8-32. Shut down through EN; I_{OUT} =3A

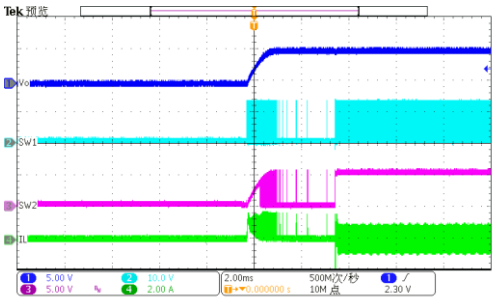


Figure 8-33. Start up through V_{IN}; I_{OUT} =0A

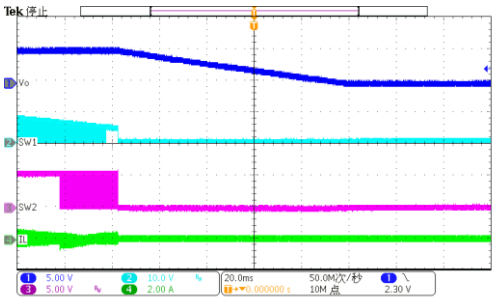


Figure 8-34. Shut down through V_{IN}; I_{OUT} =0A

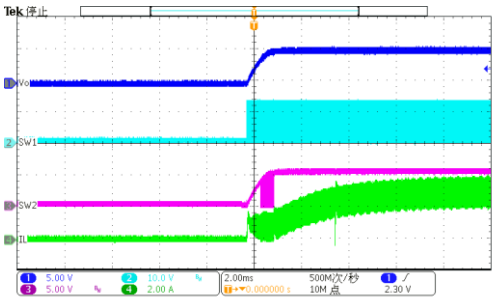


Figure 8-35. Start up through V_{IN}; I_{OUT} =3A

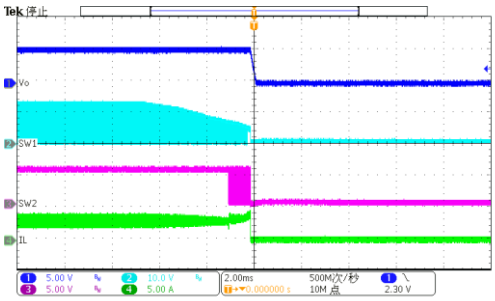


Figure 8-36. Shut down through V_{IN}; I_{OUT} =3A

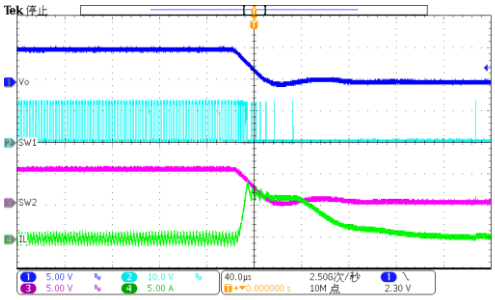


Figure 8-37. SCP Entry

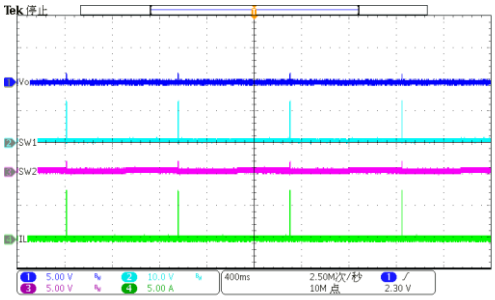


Figure 8-38. SCP Steady State

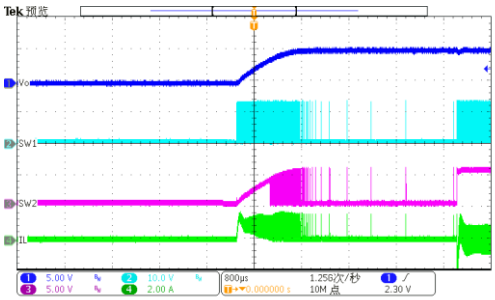


Figure 8-39. SCP Recovery

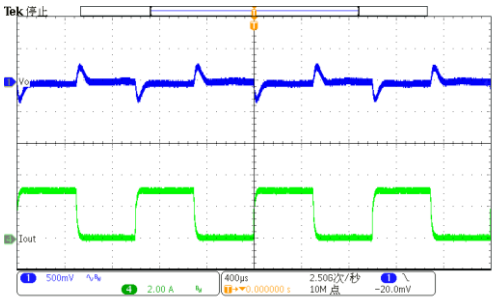


Figure 8-40. Load Transient, V_{OUT}=5V, I_{OUT} =0-3A

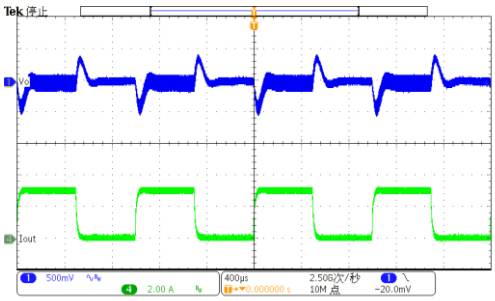


Figure 8-41. Load Transient, V_{OUT}=20V, I_{OUT} =0-3A

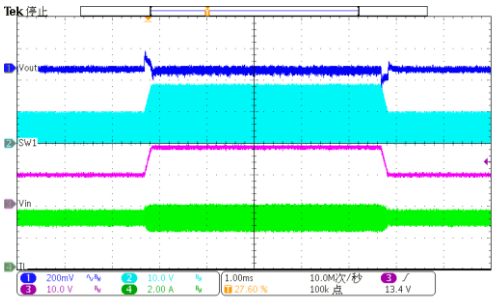


Figure 8-42. Line Transient, V_{IN}=9-18V, V_{OUT}=5V, I_{OUT} =3A

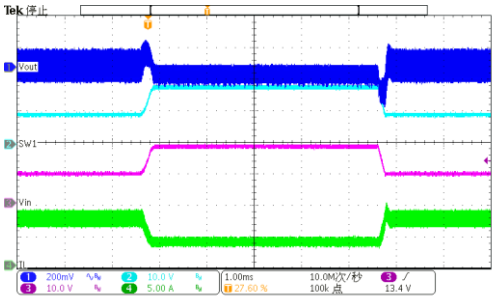


Figure 8-43. Line Transient, V_{IN}=9-18V, V_{OUT}=20V, I_{OUT} =3A

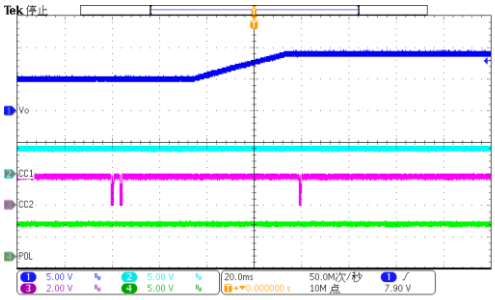


Figure 8-44. PDO Transition 5V-9V

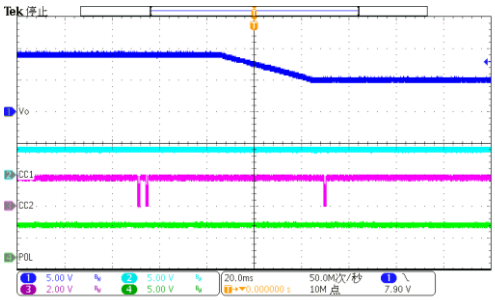


Figure 8-45. PDO Transition 9V-5V

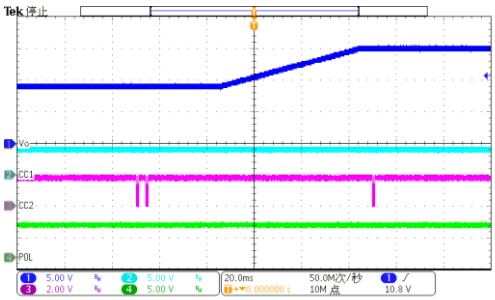


Figure 8-46. PDO Transition 9V-15V

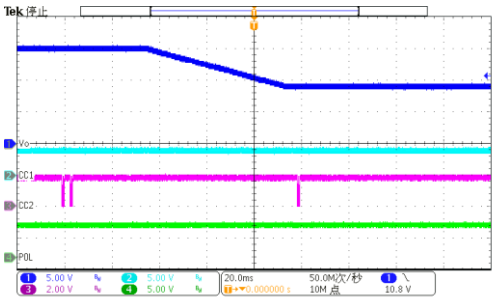


Figure 8-47. PDO Transition 15V-9V

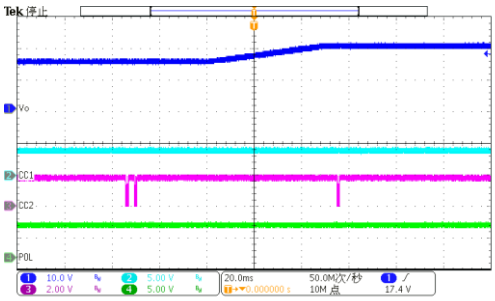


Figure 8-48. PDO Transition 15V-20V

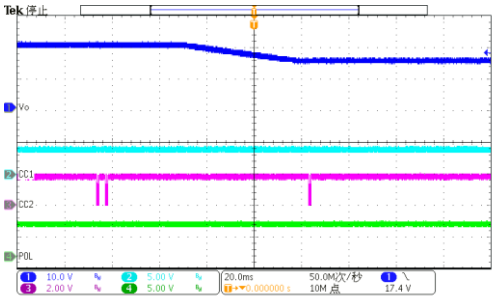


Figure 8-49. PDO Transition 20V-15V

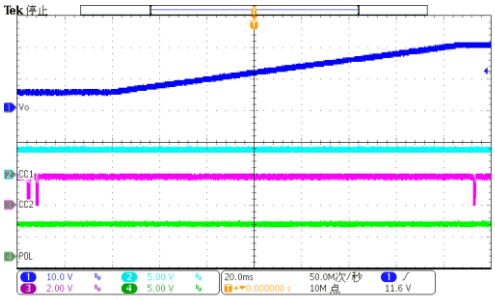


Figure 8-50. PDO Transition 5V-20V

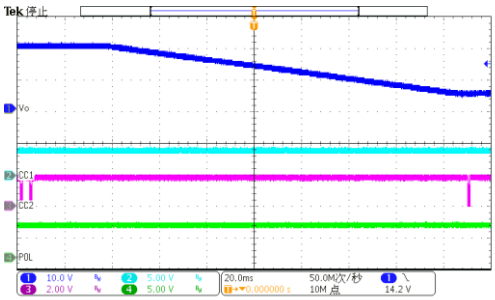


Figure 8-51. PDO Transition 20V-5V

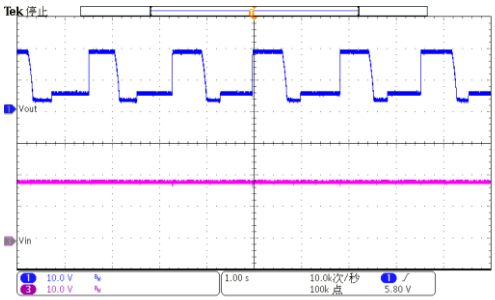


Figure 8-52. VOUT Short to 18V Battery

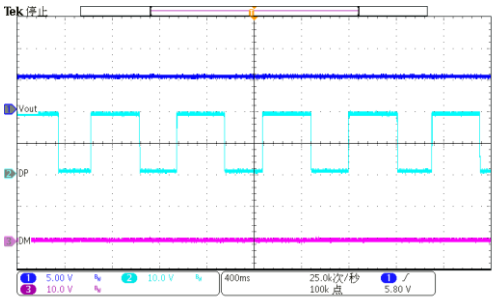


Figure 8-53. DP Short to 18V Battery

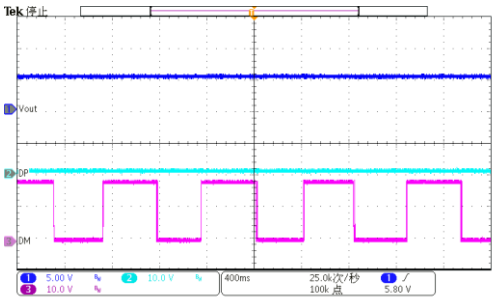


Figure 8-54. DM Short to 18V Battery

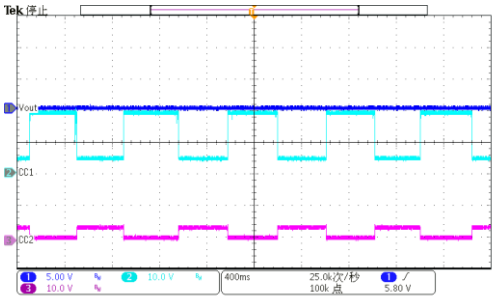


Figure 8-55. CC1 Short to 18V Battery (Detach)

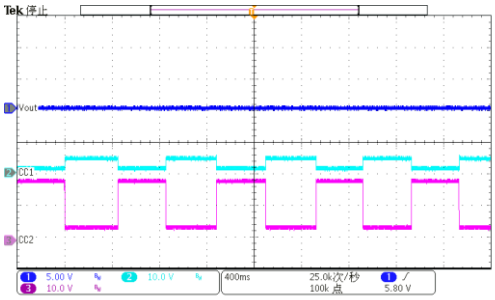


Figure 8-56. CC2 Short to 18V Battery (Detach)

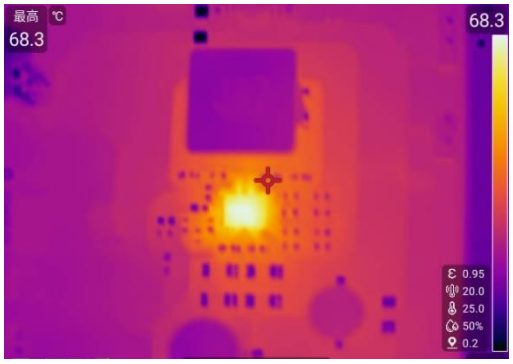


Figure 8-57. Thermal Image;

V_{IN}=12V, V_{OUT}=20V, I_{OUT}=3A, f_{SW}=420kHz, top/bottom layer: 2oz, mid-layer: 1oz, disable external switch Q1

Figure 8-58. Thermal Image;

V_{IN}=12V, V_{OUT}=20V, I_{OUT}=3.25A, f_{SW}=420kHz, top/bottom layer: 2oz, mid-layer: 1oz, disable external switch Q1

9 Functional Block Diagram

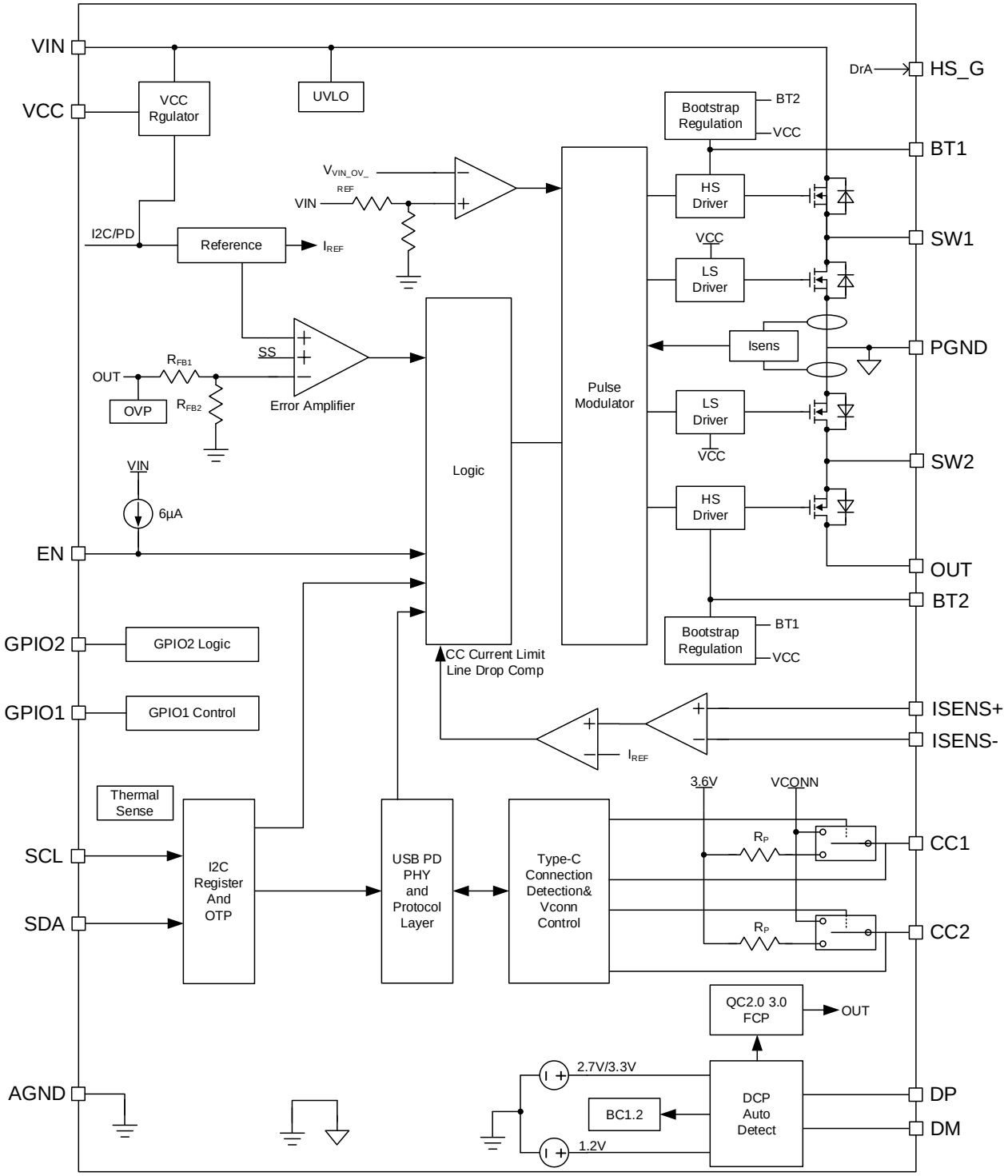


Figure 9-1. Function Block

10 Feature Description

10.1 Overview

SC87550AQ is a wide range of 4.5-V to 36-V input voltage and an output voltage of 3.3-V to 22.5-V buck-boost DCDC converter with 4-MOSFETs and USB Charging protocols integrated. It can transition among buck mode, buck-boost mode, and boost mode smoothly when the input voltage is higher or lower than the output voltage. Implementing valley-current mode control in buck mode and peak current in boost mode, SC87550AQ is able to provide excellent line and load transient performance. SC87550AQ could be configured during three frequency options 280kHz / 420kHz/ 560kHz to achieve small filter size or higher efficiency.

10.2 Device Operation Modes

10.2.1 Buck Mode

When the input voltage is higher than output voltage, SC87550AQ works in buck mode. The buck side MOSFET SWA and SWB switch for the buck regulation, while boost side MOSFET SWC is off and SWD keeps on to conduct the inductor current.

In buck modes, SC87550AQ employs adaptive ON time and valley current control. Once the internal FB voltage drops below reference voltage, SWA will turn on. After an adaptive ON time, SWB turn on to conduct the inductor current until trigger COMP control signal.

10.2.2 Boost Mode

When the input voltage is lower than output voltage, SC87550AQ works in boost mode. The boost side MOSFET SWC and SWD switch for the boost regulation, while buck side MOSFET SWB is off and SWA keeps on to conduct the inductor current.

In boost modes, SC87550AQ employs peak current control and adaptive OFF time. SWC turns on to conduct the inductor current until it rises to trigger the control signal. After SWC turns off, SWD will turn off and remain for adaptive time to regulate the output voltage.

10.2.3 Buck-Boost Mode

When the input voltage is close to the output voltage, SC87550AQ works in buck-boost mode. The MOSFET turning on sequence are SWA&SWC -> SWA&SWD -> SWB&SWD.

10.3 VCC Power Supply

An internal LDO to supply SC87550AQ outputs regulated 5-V at the VCC pin. The VCC will get the source from VIN. Both VCC and BT should have enough voltage to enable SC87550AQ. A high-quality ceramic cap of 2.2μF or higher is required between this pin and AGND.

10.4 Input Undervoltage Lockout

When the input voltage is above than 4.5V, the SC87550AQ can be enabled by pulling EN pin to a high voltage above 1.32V. When it starts running, SC87550AQ couldn't be disabled until the input voltage is below 4.3V.

10.5 EN Control

The SC87550AQ has an enable control pin(EN). The voltage on the EN pin controls the ON/OFF operation. A voltage of less than 0.96V shuts down the device, while a voltage of greater than 1.32V is required to start the device. EN pin has internal 6μA pull-up.

SC87550AQ EN is a high voltage pin, it can be connected to VIN directly or through resistor. It could establish a precision system UVLO level by inserting a resistor. An external logic signal can also be used to drive EN input for system sequencing and protection.

10.6 Soft Start

The integrated soft-start circuit prevents input inrush current and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up.

10.7 Output Current Limit and Hiccup

The output current limit is programmable from 0A to 6.35A by placing a 10mΩ current sensing resistor between ISNS+ pin and the ISNS- pin. If I_{OUT} current exceeds the set constant current limit threshold in PPS mode, SC87550AQ will enter constant current limit mode. In this mode the current amplitude is limited. As the reducing of load resistance, output voltage drops. Once the output voltage is lower than 2.7V, SC87550AQ will enters hiccup mode to periodically restart the part. The SC87550AQ exits hiccup mode once the output voltage is higher than 3V.

10.8 Switching Current Limit

SC87550AQ provides valley current limit in buck mode and peak current limit in boost and buck-boost mode by sensing LS-FET current. In buck mode, the next period won't start before IL drops to the valley current limit, which prevents inductor current runaway during short circuits on the output. In boost or buck-boost mode, SWC peak current limit works as a threshold.

10.9 Output Over-Voltage Protection

SC87550AQ has output overvoltage protection, When the output voltage at the VOUT pin is detected above 24.8V typically or the output voltage is higher than 120% of V_{REF}, the SC87550AQ turns off both high-side switches and low-side switches. The discharge path from VOUT pin to ground will turn on. If the VOUT pin voltage drops to 115% of V_{REF}, the device will return to normal operation.

10.10 Input Over-Voltage Protection

SC87550AQ has Input over-voltage protection. If the input voltage is higher than VIN OVP rising threshold (typical 29.5V), the SC87550AQ turns off both high-side switches and low-side switches. When the input voltage drops to VIN OVP falling threshold (typical 28.3V), the chip returns to normal operation. VIN OVP is controlled by I2C or OTP trim.

10.11 Switching Frequency and Spread Spectrum Function

SC87550AQ frequency could be selectable at 280kHz, 420kHz and 560kHz with a 2-bit FREQ register. Normally a 420kHz frequency is recommended. SC87550AQ has a frequency spread spectrum function, which could help minimize the peak emissions. SC87550AQ uses a triangle wave to modulate the internal oscillator, whose frequency is 1/128 of the switching frequency. The frequency span of the spread spectrum operation is 8%.

10.12 Shutdown and Load Discharge

When EN pin voltage is pulled down below 0.96V, the SC87550AQ is in shutdown mode and all functions are disabled. All internal registers are reset to default values. SC87550AQ integrates output discharge function when the output voltage needs to be discharged to the goal voltage.

10.13 Output Line Drop Compensation

SC87550AQ is capable of compensating an output voltage drop, which is helpful when there is high impedance at the output side. The compensated voltage is impacted by the output current, sense resistors and the line drop compensation gain. Refer to the register map description for detail line drop compensation amplitude.

10.14 Thermal Shutdown

SC87550AQ is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 165C(Typical). The internal soft-start circuit is reset but all internal registers values remain unchanged. The DCDC portion will automatically restarts when the junction temperature drops below the thermal shutdown hysteresis.

10.15 CC Interface

SC87550AQ use the function of the configuration channel (CC1/CC2 pin) to detect connections and configure the interface across the USB Type-C cables. The detection concept is based on being able to detect terminations in the product. To define the functional behavior of CC, a pull-up resistor (RP) and pull-down resistor termination model is used ad below. A pull-up termination can be replaced by a current source.

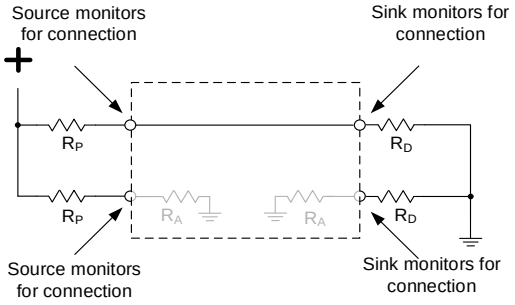


Figure 10-1 USB Type-C Connection

10.16 DPDM Interface

The SC87550AQ contains DPDM interface. The DPDM interfaces are available for USB-A port applications or Type-C port applications. It supports Apple-3A, 1.2V/1.2V Mode, BC1.2 DCP/CDP, HVDCP, QC2.0, QC3.0, FCP.

SC87550AQ supports Apple-3A mode, which broadcasts 2.7V voltage on DP and 3.3V voltage on DM pin with 30kΩ output impendence.

If a BC1.2 device is attached, SC87550AQ operates in 1.2V/1.2V and DCP mode, which complies with the BC1.2 specification. SC87550AQ shorts DP and DM pin through a 20Ω resistor.

SC87550AQ supports HVDCP mode for some high voltage protocols. Under HVDCP mode, DP and DM can check the voltage by internal comparators or detect some proprietary fast charging protocols such as FCP, QC2.0 or QC3.0.

SC87550AQ also supports BC1.2 CDP (Charging Downstream Port) handshaking as well. It can be enabled by I2C or OTP (Set CDP_EN="1b").

10.17 VCONN Switch

SC87550AQ features a 20mA VCONN power with a fixed Overcurrent Protection (OCP) of 35mA.

The IC supports electronically marked cables assembly for more than 3A power delivery. By default, passive cables

support up to 3A. The IC can check the cable types through internal CC comparators. If an e-marker cable is detected, the IC supplies the cable with VCONN and communicates with it to check the cable current ratings. Therefore, source power supply advertises any PDO if cable is identified as able to sustain such current. Refer to PD specification, the IC supports up to 5A power delivery application.

When VCONN switch is turned on, SC87550AQ will continuously monitor current on CC pin. If VCONN output current is above 35mA, VCONN switch is turned off.

10.18 USB PD Protocol

The IC provides USB PD physical layer for PD protocols communication. The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.1 standard. Once the insertion direction of Type-C port is detected by CC comparator, the IC can select either CC1 or CC2 channels to send and receive PD packets. All processes of PD communication are controlled by state machine.

10.19 LED PWM Driver

The GPIO2 pin can be configured as a PWM output to drive an LED. By default, it is 25kHz, with a 50% duty cycle PWM and a maximum 15mA capability.

The PWM duty cycle can be set between 0% and 100% (with a 1% resolution) through the I2C.

10.20 En Off Time

SC87550AQ has a configurable EN off time. When the EN pin is pulled low, the device will operate at full functionality until the timer ends. The maximum EN off delay is 120 minutes. If the EN pin is pulled high within this time, the counter will reset.

10.21 Current Monitor Output

When the GPIO1 pin is set to IMON, SC87550AQ senses the average load current through a current-sense resistor. The IMON amplifier outputs a voltage signal on the GPIO1 pin. This signal is amplified from the voltage difference between the ISEN+ and ISEN - pins. It is recommended to place a 4.7nF+4.7kΩ filter on the GPIO1 pin (see Figure 10-2). The minimum load that IMON can recognize is 0.2A.

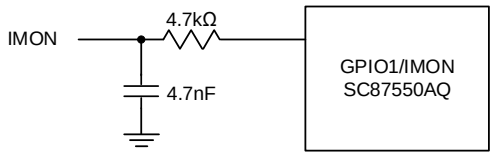


Figure 10-2 IMON Connection

The relationship between IMON voltage and load current can be calculated with Equation (1):

$$V_{IMON} = Gain \times I_{OUT} \times R_{SENSE} \quad (1)$$

Where the Gain is 30V/V, and R_{SENSE} is 10mΩ. When PFM mode is set up, the IMON function can only work normally when the part enters CCM.

10.22 Battery Short to Ground Protection Driver

SC87550AQ integrates a gate driver to realize the battery short to ground protection. Once the output ground short to battery, SC87550AQ sensed the voltage across exceeds 200mV, VGATE pin will be pulled low and isolate MOSFET will be turned off. When battery short to ground happened, DCDC will also be turned off. Figure 10-3 shows the battery to ground short driver.

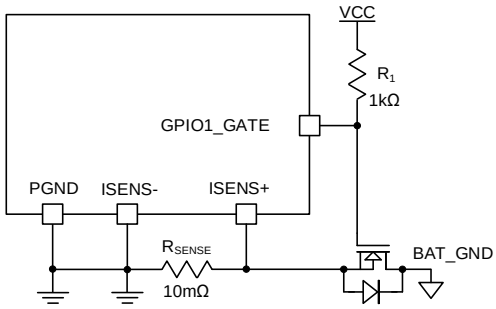


Figure 10-3 Battery Short-to-Ground Driver

10.23 NTC Function

When the GPIO2 pin is set to the NTC function, the device compares the NTC voltage to V_{REF} (0.5V Typical). If the NTC voltage is below the threshold, the device will either shut down or reduce the PD power. The response can be selected via NTC_MODE.

If NTC_MODE is set to 1, OTW2_NTC_PDP determines the value to which PD power should be reduced. See Table 1 for more details.

PD power of NTC status can also be configured via one-time-programmable (OTP) memory by OTW2_NTC_PDO_SELECT in Table 2.

If the NTC voltage rises above the recovery threshold, the device recovers to a normal state. The I2C or OTP can set one of two NTC recovery hysteresis values.

10.24 NTC2 Function

When the GPIO1 pin is set to the NTC2 function, the device compares the NTC2 voltage to V_{REF} (0.5V Typical). If the

NTC2 voltage is below the threshold, the device will reduce the PD power. PD power rating drops to the value set by PS_PDP. Table 1 shows the PDO / APDO voltage and current.

PD power of NTC2 status can also be configured via OTP by POWER_SHARE_PDO_SELECT in Table 2.

If the NTC2 voltage rises above the recovery threshold, the device recovers to a normal state. NTC_HYSTERESIS sets the hysteresis, which is also sets the hysteresis for the GPIO1 pin's NTC function.

If GPIO2 is set to the power share function while GPIO1 is set for the NTC2 function, the SC87550AQ enters power sharing when either NTC2 or GPIO2_POWER_SHARE is triggered.

10.25 Over Temperature Warning (OTW) Function

The SC87550AQ senses its die temperature internally. If the chip's temperature exceeds the OTW1 threshold, the SC87550AQ reduces the PD power state to the value set by OTW1_PDP. Table 1 shows the OTW1_PDP function.

If the die temperature continues increasing and triggers the second threshold set by OTW2, the SC87550AQ reduces the PD power to the level set by OTW2_NTC_PDP. The SC87550AQ waits 16 seconds after the OTW condition is removed before recovering to a normal PD rating.

PD power of OTW status can also be configured via OTP by OTW1_PDO_SELECT and OTW2_NTC_PDO_SELECT in Table 2.

10.26 Low-Battery Operation

During the first VIN start-up, the SC87550AQ is delayed for 1s before detecting VIN. If the SC87550AQ detects that the battery voltage (its VIN voltage) is lower than the VBATT_LOW_THLD1 falling threshold for the VBATT_LOW_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT_LOW1_FLAG is set. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP.

If the SC87550AQ detects that the battery voltage (its VIN voltage) is below the VBATT_LOW_THLD2 falling threshold for the VBATT_LOW_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT_LOW2_FLAG is set. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP.

PD power of Low-Battery status can also be configured via OTP by VBATT_LOW1_PDO_SELECT and VBATT_LOW2_PDO_SELECT in Table 2.

If the SC87550AQ detects that the battery voltage (its VIN voltage) is below the VBATT_LOW_THLD3 falling threshold for the VBATT_LOW_BLK deglitch time, it shuts down. When the battery voltage recovers and exceeds the VBATT_LOW_THLD rising threshold with a 1s digital deglitch time, the PDO recovers to normal PDP.

There are three battery voltage (VBATT) low thresholds: VBATT_LOW_THLD1, VBATT_LOW_THLD2, and VBATT_LOW_THLD3. During the SC87550AQ's first start-up, the internal VBATT_LOW_FLAG default state is 0. The VBATT_LOW detection circuitry starts to work when a USB Type-C receptacle is attached; it is reset by UVLO or an EN shutdown.

10.27 GPIO1 Power Share1 Function

The GPIO1_POWER_SHARE falling threshold is typically 0.5V. If the second SC87550AQ (SC87550AQ-B) detects that a valid sink is attached in, the first SC87550AQ's (SC87550AQ-A) GPIO1_POWER_SHARE pin is pulled down by the SC87550AQ-B's GPIO2_ATTACH pin (see Figure 10-4).

When the power share function is triggered, the PDO list and current are determined by PS_PDP. For example, a 3.3V to 21V APDO current rating is can be calculated as 45W / 21V = 2.1A.

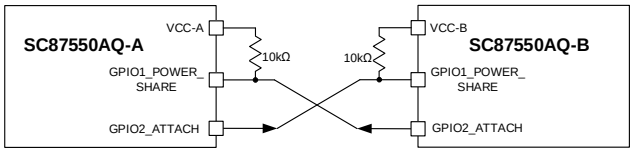


Figure 10-4 GPIO1 Power Share Connection Between Two SC87550AQs

10.28 GPIO2 Power Share2 Function

The GPIO2_POWER_SHARE rising threshold is typically 1.87V(VTH_PS_R). When the GPIO2 pin is set for the power share function, and the SC87550AQ-A detects that its GPIO2 voltage exceeds VTH_PS_R, the power share function is triggered. The PDO list and current is determined by PS_PDP (see Table 1).

The SC87550AQ exits the power sharing status after the GPIO2 voltage drops below VTH_PS_F (typically 1.67V). Figure 10-5 shows the GPIO2_POWER_SHARE connection block. When VBUS exceeds 11.2V, the power share function is triggered.

PD power of Power Share1 and Power Share2 status can also be configured via OTP by POWER_SHARE_PDO_SELECT in Table 2.

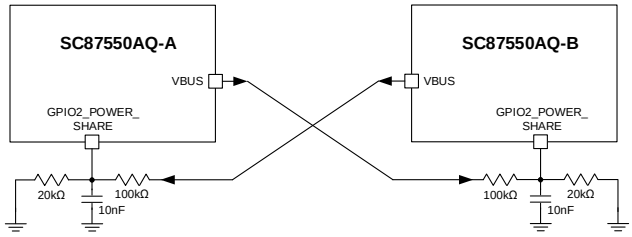


Figure 10-5 GPIO2 Power Share Connection Between Two SC87550AQs

Figure 10-6 shows the PDP state machine.

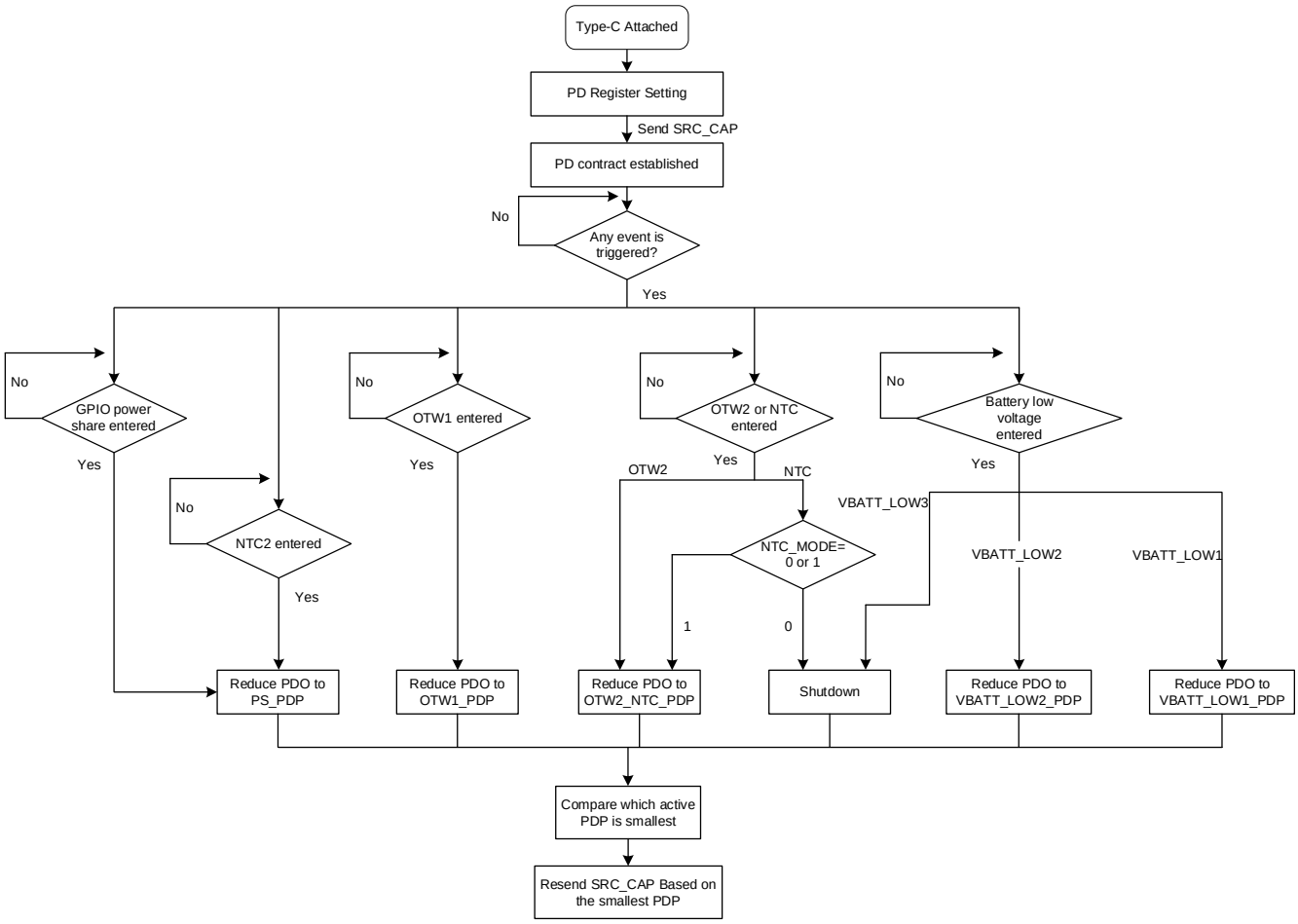


Figure 10-6 PDP State Machine

11 Application Information

11.1. Capacitor Selection

SC87550AQ has three frequency options of 280kHz / 420kHz/ 560kHz. The high capacitance polymer capacitor or tantalum capacitor can be used for input and output but capacitor voltage rating must be higher than the highest operating voltage with enough margin. The high frequency characteristics of these capacitors are not as good as ceramic capacitor, so at least 10μF ceramic capacitor should be placed in parallel to reduce high frequency ripple.

11.2. Inductor Selection

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). Normally 2.2 μH to 10 μH inductor is recommended here.

The peak inductor current can be calculated as:

$$I_{L\_PEAK} = I_{OUT} + \frac{V_{OUT}\cdot(V_{IN} - V_{OUT})}{2\cdot F_{SW}\cdot L\cdot V_{IN}\cdot\eta} \quad (V_{IN}>V_{OUT}) \qquad (2)$$

$$I_{L\_PEAK} = I_{IN} + \frac{V_{IN}\cdot(V_{OUT}-V_{IN}\cdot\eta)}{2\cdot F_{SW}\cdot L\cdot V_{OUT}} \quad (V_{IN}\le V_{OUT}) \qquad (3)$$

η is the power conversion efficiency. User can use 95% for calculation.

F_{SW} is the switching frequency

L is the inductor value

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$P_{L\_DC} = I_L^2\cdot DCR \qquad (4)$$

I_L is the average value of inductor current.

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user can consult with the inductor vendor to select the inductors which have small ESR at high frequency and small core loss.

11.3. Current Sense Resistor

The ISNS+ and ISNS- are current sense resistors. 10 mΩ should be used to sense the current (10 mΩ supports higher battery current limit accuracy, and 5 mΩ supports higher efficiency). Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

The resistor power rating and temperature coefficient should be considered. The power dissipation is roughly calculated as $P=I^2R$, and I is the highest current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

11.4. BOOT Capacitor Selection

The SC87550AQ requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the high-side power MOSFET. A high-quality (X7R) ceramic capacitor of 100nF and at least 50V is recommended.

11.5. BOOT Resistor Selection

A BOOT resistor and capacitor can be connected in series between the BOOT and SW pins. Unless EMI for the application being designed is critical, R_{BOOT} can be shorted. To maximize efficiency, 0 Ω is chosen for this example. Under most circumstances, selecting an R_{BOOT} resistor value above 20Ω is undesirable since the resulting small improvement in EMI is not enough to justify further decreased efficiency.

11.6. VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a 2.2μF, 16V ceramic capacitor connected from VCC to GND for proper operation. Avoid loading this output with any external circuitry.

11.7. External MOSFET Selection

The IC integrates four power MOSFETs. When the total power does not exceed 65W, there is no need to use an external MOSFET (Buck High Side Q1). When the total power exceeds 65W, an external MOSFET Q1 needs to be added.

The V_{DS} of MOSFET should be higher than the highest operating voltage with enough margin (recommend more than 10V higher).

The V_{GS} voltage rating of MOSFET should be selected higher than 8V. Considering PCB parasitic parameters during operation, MOSFET V_{GS} voltage might be higher than

V_{DRV} voltage due to transient overshoot, so 10V V_{GS} is recommended to secure sufficient margin.

The MOSFET current I_D should be higher than the highest battery current with enough margin.

To ensure the sufficient current capability in relatively high temperature circumstance, the current rate at T_A=70˚C or T_C = 100˚C should be considered. In addition, the power dissipation value P_D should also be considered and higher P_D is better in applications. Make sure that MOSFET power consumption must not exceed P_D value.

The MOSFET $R_{DS(ON)}$ and input capacitor C_{ISS} impact power efficiency directly. Typically, lower $R_{DS(ON)}$ MOSFET has higher C_{ISS}. The $R_{DS(ON)}$ is related to conduction loss. Higher R_{DSON} results in higher conduction loss, thus lower efficiency and higher thermal dissipation; the C_{ISS} is related to MOSFET switch on/off time, and longer on/off time results in higher switching loss and lower efficiency. The proper MOSEFT should be selected based on tradeoff between the $R_{DS(ON)}$ and C_{ISS}.

If high C_{ISS} MOSFET is selected, the switching on and off time become longer, then the dead time should be adjusted to avoid simultaneous turn on for both high side and low side MOSFETs.

11.8. Driver Resistor and SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add series resistor for gate driving signal (HS_G to MOS gate), and RC snubber circuit at SW1 and SW2

The driver resistor should be placed near MOS. At first, use 0Ω resistors; if switching overshoot is big, increase the resistor value to slow down the switching speed. It is suggested to keep the resistor value < 10 Ω. While the switching speed gets slower, the default dead time may not be enough to avoid overshoot of the power MOSFETs. So if higher than 10Ω is needed, user should increase the dead time if necessary.

The RC snubber circuit at SWx node is also helpful in absorbing the high frequency spike at SWx node, so to improve EMC performance. User can leave RC components as NC at the beginning, and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and 1nF for the snubber. If EMC should be improved further, reduce the resistor value (like 1 Ω or even lower) and increase the capacitor value (like 2.2nF or even higher).

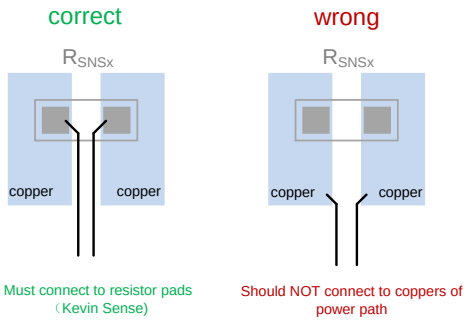
12 Layout Guide

The PCB layout is critical to get the optimal performance and thermal dissipation. For SC87550AQ, the loop consisting of VIN-SW1-GND and SW2-VOUT-GND is the most important. Poor layout means larger parasitic parameters and noise. Generally, to reduce the PCB inductance, the area of this loop must be small, and the trace must be wide. **Figure 12-1** shows a recommended layout.

1. The 1μF ~ 4.7μF capacitors connected at VCC pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.

2. Put I_{OUT} current sense resistor and bulk capacitor at V_{OUT} side as close as possible.

3. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and add filter for each current sense near the IC.



4. Place PGND vias close to PGND pin and under the IC's body.

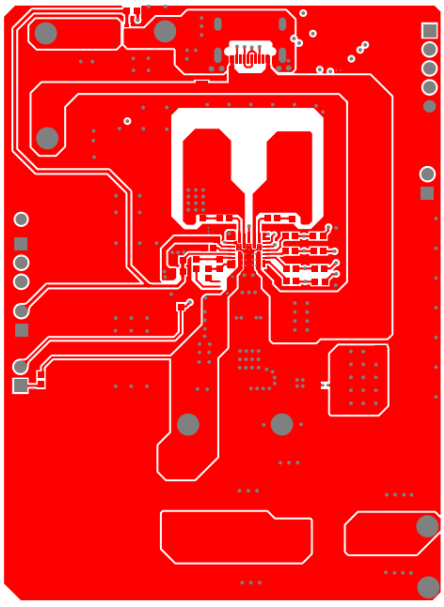
5. Place the ceramic capacitors as close to VIN and VOUT pin as possible, especially the small package size (recommend 0603) bypass capacitor.

6.Connect a large ground plane to GND on all layers. Add vias near GND if there are several ground planes on different layers.

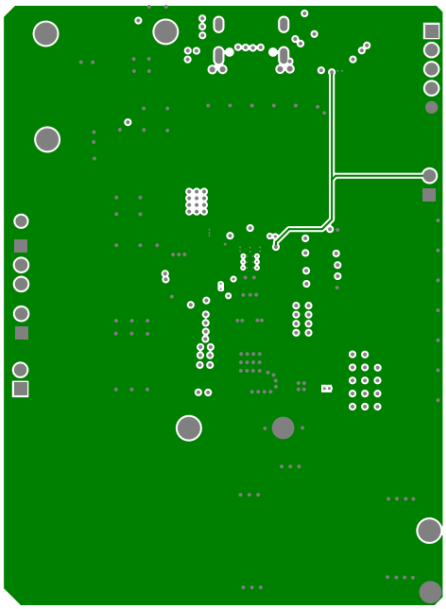
7. If an R_{BOOT1} or R_{BOOT2} resistor is used, place it as close as possible to BT1 or BT2 pins. If high efficiency is desired, R_{BOOT} can be shorted.

8.The VIN, SW1, SW2, VOUT and GND paths must be wide and short enough to reduce any voltage drops on the input or output paths of the converter.

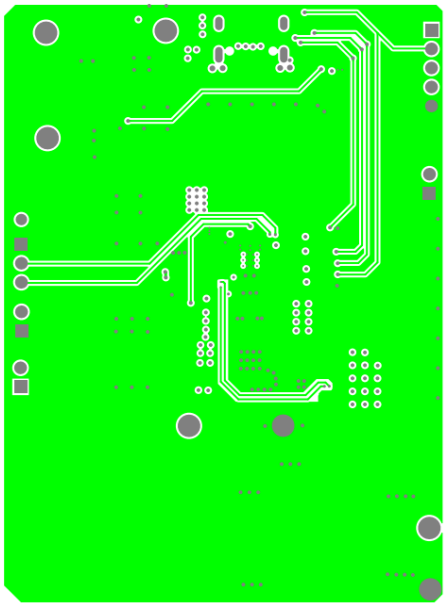
9. The area of SW1-BT1 and SW2-BT2 should be small to reduce EMC noise.



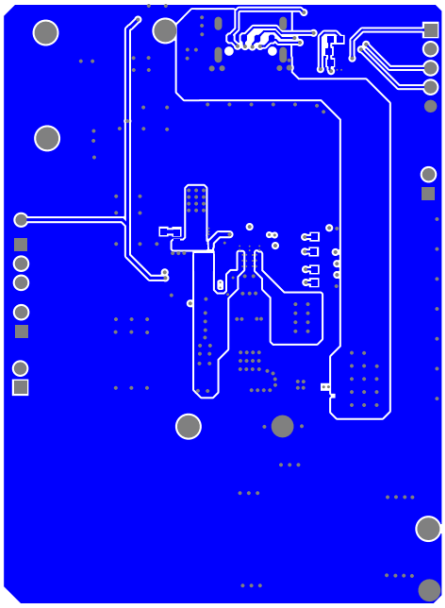
(a) Top Layer



(b) GND1 Layer



(c) GND2 Layer



(d) Bottom Layer

Figure 12-1 Layout Example

13 Typical Application Circuits

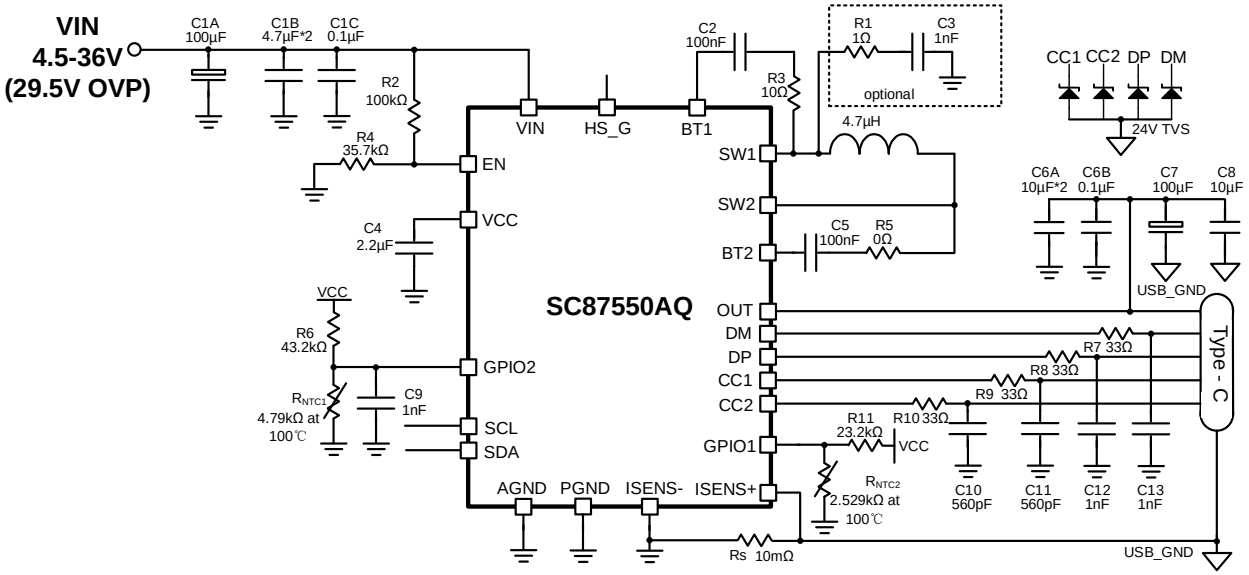


Figure 13-1 SC87550AQ 60W PD Application

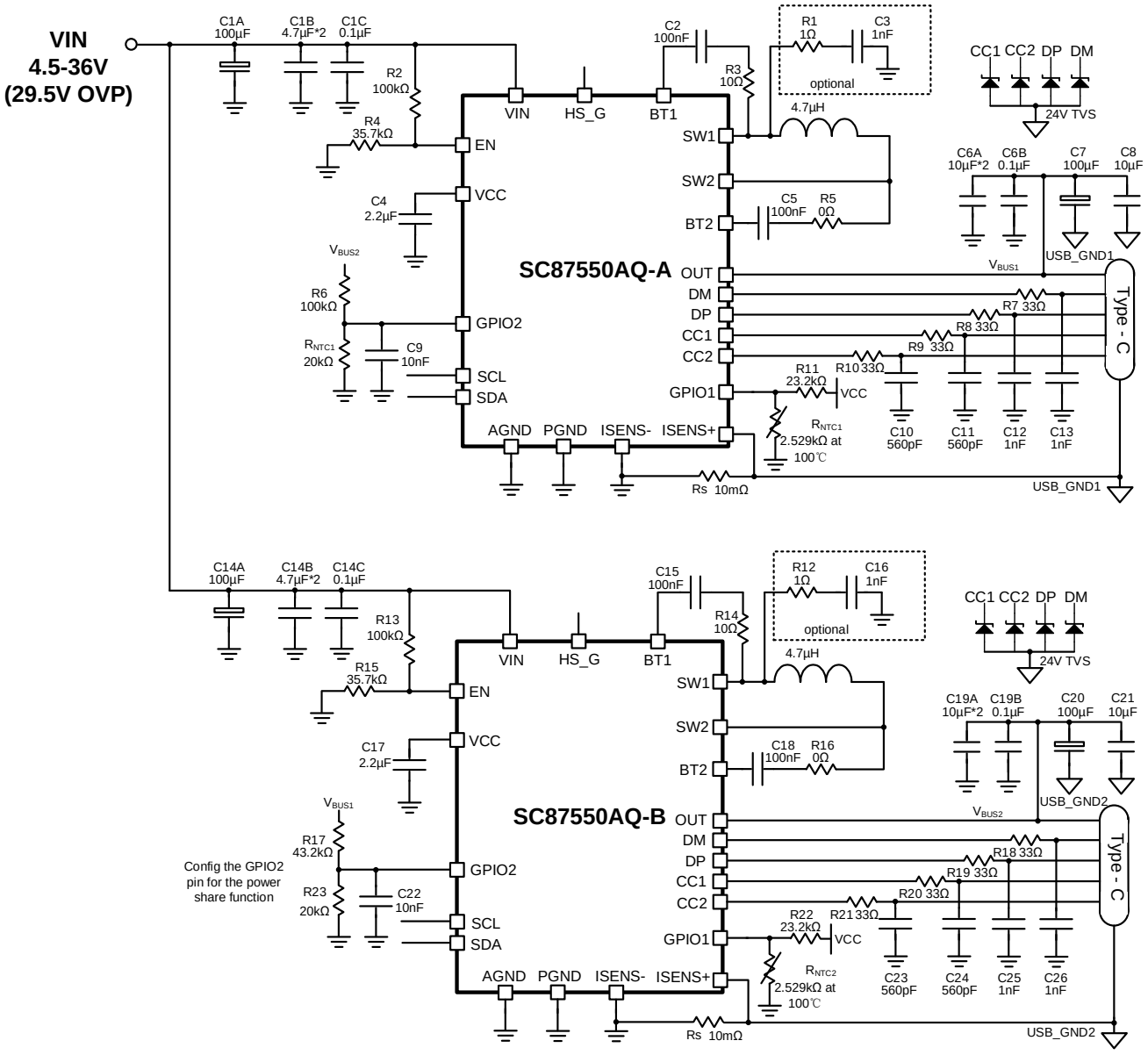


Figure 13-2 SC87550AQ Dual-Channel 45W PD Application with GPIO2_POWER_SHARE (1)(2)

Notes:

(1) See figure10-6 for the GPIO2 power share PDP management. V_{BUS} exceeds 11.2V to trigger power share function (GPIO2 input voltage > 1.87V).

(2) TVS diodes are required to pass the ±8kV contact and ±15kV air discharge per IEC ESD specifications.

14 Register Maps

Table1 SC87550AQ Register Maps

The 7-bit I2C address of the chip is 0x61H Default

ADD (HEX)	Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	PDO_SET1	RW	RESERVED		PDO7_EN*	PDO6_EN*	PDO5_EN*	PDO4_EN*	PDO3_EN*	PDO2_EN*
0x01	PDO_SET2	RW	RESERVED		PDO7_TYPE*	PDO6_TYPE*	PDO5_TYPE*	PDO4_TYPE*	PDO3_TYPE*	PDO2_TYPE*
0x02	HOST_SET	RW	RESERVED							
0x03	PDO_I1	RW	PDO1_CUR_SET [7:0] * (3A DEFAULT)							
0x04	PDO_V2L	RW	PDO_V2_L[7:0] * (9V DEFAULT)							
0x05	PDO_V2H	RW	PDO_V2_H[7:0] * (0x00)							
0x06	PDO_I2	RW	PDO2_CUR_SET [7:0] * (3A DEFAULT)							
0x07	PDO_V3L	RW	PDO_V3_L[7:0] * (15V DEFAULT)							
0x08	PDO_V3H	RW	PDO_V3_H[7:0] * (0x00)							
0x09	PDO_I3	RW	PDO3_CUR_SET [7:0] * (3A DEFAULT)							
0x0A	PDO_V4L	RW	PDO_V4_L[7:0] * (20V DEFAULT)							
0x0B	PDO_V4H	RW	PDO_V4_H[7:0] * (0x00)							
0x0C	PDO_I4	RW	PDO4_CUR_SET [7:0] * (3A DEFAULT)							
0x0D	PDO_V5L	RW	PDO_V5_L[7:0] * (3.3V DEFAULT)							
0x0E	PDO_V5H	RW	PDO_V5_H[7:0] * (11V DEFAULT)							
0x0F	PDO_I5	RW	PDO5_CUR_SET [7:0] * (3A DEFAULT)							
0x10	PDO_V6L	RW	PDO_V6_L[7:0] * (3.3V DEFAULT)							
0x11	PDO_V6H	RW	PDO_V6_H[7:0] * (16V DEFAULT)							

0x12	PDO_I6	RW	PDO6_CUR_SET [7:0] * (3A DEFAULT)					
0x13	PDO_V7L	RW	PDO_V7_L[7:0] * (3.3V DEFAULT)					
0x14	PDO_V7H	RW	PDO_V7_H[7:0] * (21V DEFAULT)					
0x15	PDO_I7	RW	PDO7_CUR_SET [7:0] * (3A DEFAULT)					
0x16	PD_CTL1	RW	CDP_EN*	LEGACY_CHARGING_MODE_SEL[1:0] *	USBCOMMUNICATE*	NTC_CTL_RP*	TOUCH TEMP[1:0] *	TYPE-C_MODE*
0x17	PD_CTL2	RW	HDRST	USB SUSPEND*	TOUCH CURRENT[2:0] *		COMPLIANCE[2:0] *	
0x18	PWR_CTRL1	RW	EN	MODE*	FREQ[1:0] *	DITHER*	LINE_DROP_COMP[1:0] *	SLEW_RATE*
0x19	PWR_CTRL2	RW	EN_VBUS	PPS_MIN_SEL*	OTW1_THRESHOLD[2:0] *		OTP_THRESHOLD[2:0] *	
0x1A	VOUTL	RW	VOUT_L[7:0]					
0x1B	VOUTH	RW	RESERVED			VIN_OVP[1:0] *	VOUT_H[1:0]	
0x1C	IOUT_LIM	RW	RESERVED	IOUT_LIM[6:0] *				
0x1D	CTL_SYS0	RW	RESERVED					GO_BIT
0x1E	CTL_SYS1	RW	SENT_SRC CAP	RESERVED	EN_OFF_TIMER[1:0] *	I2C_SLAVE_ADDRESS[3:0] *		
0x1F	CTL_SYS2	RW	GPIO1[2:0] *		GPIO2[2:0] *		I2C_CTL_VOUT_EN	RSNS *
0x20	CTL_SYS3	RW	PS_PDP[7:0] *					
0x21	CTL_SYS4	RW	PS_PDP_SEL[7:0] *					
0x22	CTL_SYS5	RW	RESERVED	PPS_3A_5A *	OC_BLANK_TIMER[2:0] *		BB2T_REG*	PD_CAP_PEAK_CURRENT[1:0]
0x23	CTL_SYS6	RW	VBATT_LOW1_PDP[7:0] *					
0x24	CTL_SYS7	RW	VBATT_L1_PDP_SEL[7:0] *					
0x25	CTL_SYS8	RW	VBATT_LOW2_PDP[7:0] *					
0x26	CTL_SYS9	RW	VBATT_L2_PDP_SEL[7:0] *					

0x27	CTL_SYS10	RW	OTW1_PDP[7:0] *						
0x28	CTL_SYS11	RW	OTW1_PDP_SEL[7:0] *						
0x29	CTL_SYS12	RW	OTW2_NTC_PDP[7:0] *						
0x2A	CTL_SYS13	RW	OTW2_NTC_PDP_SEL[7:0] *						
0x2B	CTL_SYS14	RW	VBATT_LOW_THLD1[3:0] *				VBATT_LOW_THLD2[3:0] *		
0x2C	CTL_SYS15	RW	VBATT_LOW_THLD3[3:0] *				VBATT_LOW_BLK[1:0] *	VCONN_OCP_BLK*	
0x2D	CTL_SYS16	RW	RESERVED				OTW2_THRESHOLD[2:0] *		VCONN_OCP_EN_SYN
0x2E	CTL_SYS17	RW	PEAK_CL*	INCC_BLK*		NTC_HYSTERESIS*	NTC_MODE*	VOUT OVP*	VBUS_VOLTAGE[1:0] *
0x2F	CTL_SYS18	RW	RESERVED	LED_PWM_DUTY[6:0] *					
0x30	STATUS1	R	ATTACHED	NTC2_ENTER	POL	SHORT_VBATT	FAULT	VCONN STATUS	CC_CV	NTC_ENTER
0x31	STATUS2	R	VBATT_LOW1_FLAG	VBATT_LOW2_FLAG	OTW1	OTW2	SELECTED_PDO_INDEX[2:0]			PDO_TYPE
0x32	STATUS3	R	Contract Power[7:0]						
0x35	FW_REV	R	Reserved		CABLE_CAP	Reserved			
0x36	MAX_REQ_CUR	R	MAX_REQ_CUR[7:0]						

Note: All *registers are OTP programmable

Address 0x00H: PDO_SET1

Bit	Type	Bit Name	Default	Description
7:6	NA			
5	R/W	PDO7_EN	1b	PDO7 enable setting. 0b: The output is off; 1b: The output is on.
4	R/W	PDO6_EN	0b	PDO6 enable setting. 0b: The output is off; 1b: The output is on.
3	R/W	PDO5_EN	0b	PDO5 enable setting. 0b: The output is off; 1b: The output is on.
2	R/W	PDO4_EN	1b	PDO4 enable setting. 0b: The output is off; 1b: The output is on.
1	R/W	PDO3_EN	1b	PDO3 enable setting. 0b: The output is off; 1b: The output is on.
0	R/W	PDO2_EN	1b	PDO2 enable setting. 0b: The output is off; 1b: The output is on.

Address 0x01H: PDO_SET2

Bit	Type	Bit Name	Default	Description
7:6	RESERVED			
5	R/W	PDO7_TYPE	1b	PDO7 type setting. 0b: Fixed PDO; 1b: APDO.
4	R/W	PDO6_TYPE	1b	PDO6 type setting. 0b: Fixed PDO; 1b: APDO.
3	R/W	PDO5_TYPE	1b	PDO5 type setting. 0b: Fixed PDO; 1b: APDO.
2	R/W	PDO4_TYPE	0b	PDO4 type setting. 0b: Fixed PDO; 1b: APDO.
1	R/W	PDO3_TYPE	0b	PDO3 type setting. 0b: Fixed PDO; 1b: APDO.
0	R/W	PDO2_TYPE	0b	PDO2 type setting. 0b: Fixed PDO; 1b: APDO.

Address 0x03H: PDO_I1

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO1_CUR_SET	0x96	PDO1's maximum output current setting in 20mA units. Default is 3A. or "0x96". When this bit is set >3A, will check the cable current rating firstly, if it's 5A, then send with >3A setting; If the cable is 3A, only send 3A maximum current capability.

Address 0x04H: PDO_V2_L

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V2_L	0x5A	If the PDO2_TYPE is fixed PDO: PDO2's output voltage setting in 100mV units. Default is 9V, or

				"0x5A". The maximum voltage can be set by this register is 22.97 If the PDO2_TYPE is APDO: Minimum Voltage in 100mV increments

Address 0x05H: PDO_V2_H

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V2_H	0b	If the PDO2_TYPE is APDO: Maximum Voltage in 100mV increments

Address 0x06H: PDO_I2

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO2_CUR_SET	0x96	PDO2's maximum output current setting in 20mA units for fixed PDO; 50mA units for APDO(PPS). Default is 3A and fixed PDO. or "0x96". When this bit is set >3A, will check the cable current rating firstly, if it's 5A, then send with >3A setting; If the cable is 3A, only send 3A maximum current capability.

Address 0x07H: PDO_V3_L

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V3_L	0x96	If the PDO3_TYPE is fixed PDO: PDO3's output voltage setting in 100mV units. Default is 15V, or "0x96". The maximum voltage can be set by this register is 22.97V. If the PDO3_TYPE is APDO: Minimum Voltage in 100mV increments

Address 0x08H: PDO_V3_H

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V3_H	0b	If the PDO3_TYPE is APDO: Maximum Voltage in 100mV increments

Address 0x09H: PDO_I3

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO3_CUR_SET	0x96	PDO3's maximum output current setting in 20mA units for fixed PDO; 50mA units for APDO(PPS). Default is 3A and fixed PDO. or "0x96". When this bit is set >3A, will check the cable current rating firstly, if it's 5A, then send with >3A setting; If the cable is 3A, only send 3A maximum current capability.

Address 0x0AH: PDO_V4_L

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V4_L	0XC8	If the PDO4_TYPE is fixed PDO: PDO4's output voltage setting in 100mV units. Default is 20V, or "0xC8". The maximum voltage can be set by this register is 22.97V. If the PDO4_TYPE is APDO: Minimum Voltage in 100mV increments

Address 0x0BH: PDO_V4_H

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V4_H	0b	If the PDO4_TYPE is APDO: Maximum Voltage in 100mV increments

Address 0x0CH: PDO_I4

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO4_CUR_SET	0x96	PDO4's maximum output current setting in 20mA units for fixed PDO; 50mA units for APDO(PPS). Default is 3A and fixed PDO. or "0x96". When this bit is set >3A, will check the cable

				current rating firstly, if it's 5A, then send with >3A setting; If the cable is 3A, only send 3A maximum current capability.

Address 0x0DH: PDO_V5_L

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V5_L	0x32	If the PDO5_TYPE is fixed PDO: PDO5's output voltage setting in 100mV units If the PDO5_TYPE is APDO: Minimum Voltage in 100mV increments. Default 5V, or "0x32"

Address 0x0EH: PDO_V5_H

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V5_H	0X6E	If the PDO5_TYPE is APDO: Maximum Voltage in 100mV increments. Default 11V, or "0x6E"

Address 0x0FH: PDO_I5

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO5_CUR_SET	0x3C	PDO5's maximum output current setting in 20mA units for fixed PDO; 50mA units for APDO(PPS). Default is 3A and APDO. When this bit is set >3A, will check the cable current rating firstly, if it's 5A, then send with >3A setting; If the cable is 3A, only send 3A maximum current capability.

Address 0x10H: PDO_V6_L

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V6_L	0x32	If the PDO6_TYPE is fixed PDO: PDO6's output voltage setting in 100mV units If the PDO6_TYPE is APDO: Minimum Voltage in 100mV increments. Default 5V, or "0x32"

Address 0x11H: PDO_V6_H

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V6_H	0XA0	If the PDO6_TYPE is APDO: Maximum Voltage in 100mV increments. Default 16V, or "0xA0"

Address 0x12H: PDO_I6

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO6_CUR_SET	0x3C	PDO6's maximum output current setting in 20mA units for fixed PDO; 50mA units for APDO(PPS). Default is 3A and APDO. When this bit is set >3A, will check the cable current rating firstly, if it's 5A, then send with >3A setting; If the cable is 3A, only send 3A maximum current capability.

Address 0x13H: PDO_V7_L

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V7_L	0x32	If the PDO7_TYPE is fixed PDO: PDO7's output voltage setting in 100mV units If the PDO7_TYPE is APDO: Minimum Voltage in 100mV increments. Default 5V, or "0x32"

Address 0x14H: PDO_V7_H

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO_V7_H	0XD2	If the PDO7_TYPE is APDO: Maximum Voltage in 100mV increments. Default 21V, or "0xD2"

Address 0x15H: PDO_I7

Bit	Type	Bit Name	Default	Description
7:0	R/W	PDO7_CUR_SET	0x3C	PDO7's maximum output current setting in 20mA units for fixed PDO; 50mA units for APDO(PPS). Default is 3A and APDO. When this bit is set >3A, will check the cable current rating firstly, if it's 5A, then send with >3A setting; If the cable is 3A, only send 3A maximum current capability.

Address 0x16H: PD_CTL1

Bit	Type	Bit Name	Default	Description
7	R/W	CDP_EN	0b	Select CDP mode. Once this bit is set to "1", all the DCP/QC/Apple mode are disabled. Device only works as CDP handshaking mode.
6:5	R/W	LEGACY_CHARGING_MODE_SEL	0b	CDP_EN: 1 / 0 / 0 / 0 CHARGING_MODE: X / 00 / 01 / 10/11 TRUTH TABLE: CDP Mode / All DPDM Modes / Apple mode and 1.2V/1.2V mode / Only DCP
4	R/W	USB COMMUNICATE	0b	USB Communication Capable or not. 0b: Not support. 1b: Support.
3	R/W	NTC_CTL_RP	0b	Select NTC, OTW event triggers Type-C 3A or 1.5A mode. "0b" means If PDP<15W, Rp=1.5A; Otherwise, it's 3A Rp. "1b" means when NTC or OTW1/OTW2 happens, it's 1.5A mode.
2:1	R/W	TOUCH TEMP	0b	Set the touch temp default value "00b"
0	R/W	TYPE-C MODE	0b	Select 3A or 1.5A Type-C mode. "0b" means 3A Type-C mode; "1b" means 1.5A Type-C mode. In 5V@3A Type-C mode, the Rp pull-up current is 330uA and Rd detection range is 0.85V-2.45V

Address 0x17H: PD_CTL2

Bit	Type	Bit Name	Default	Description
7	R/W	HDRST	0b	Send HardReset command. 0b: normal state. 1b: Send hardreset to Sink. After the HDRST message is sent, this bit auto reset to "0b".
6	R/W	USB SUSPEND	0b	USB Suspend supported or not. 0b: Not support. 1b: Support.
5:3	R/W	TOUCH CURRENT	0b	Set the touch current bit 0 to bit 2: "000b" for default. D[5] indicates touch current bit 2.
2:0	R/W	COMPLIANCE	0b	Set the bit 2, bit 1 and bit 0 value of Compliance byte. D[2] sets the bit 2 value.

Address 0x18H: PWR_CTL1

Bit	Type	Bit Name	Default	Description
7	R/W	EN	1b	I2C controlled turn-on or turn-off the part. When external EN pin is low, the converter is off and I2C is also shutdown. When EN pin is high, the EN bit will take over. The default EN bit is "1". When set this EN bit to "0", the part is off but the I2C register doesn't reset. When EN=0, the Type-C logic is off
6	R/W	MODE	1b	0b: enables auto PFM/PWM mode, 1b: set force PWM mode.
5:4	R/W	FREQ	1b	Set switching frequency:

				00b: 280kHz 01b: 420kHz 10b: 560kHz
3	R/W	DITHER	1b	Set the spread spectrum feature: 0b: No frequency spread spectrum; 1b: Enable frequency spread spectrum.
2:1	R/W	LINE_DROP_COMP	00b	Set output voltage compensation vs load feature: 00b: No compensation 01b: Vout compensates 100mV@3A Iout 10b: Vout compensates 300mV@3A Iout 11b: Vout compensates 600mV@3A Iout Above compensation amplitude is fixed for any output voltage. Line drop compensation has a max clamp at 800mV no matter how large is the output current. Line drop compensation is disabled once enter PPS PDO for default IC. The Line drop compensation can be enabled in PPS PDO through factory OTP trim.
0	R/W	SLEW_RATE	0b	Set output slew rate during adjust VBUS: 0b: 0.1mV/us VBUS rising slew rate, 0.1mV/us VBUS falling slew rate; 1b: 1mV/us VBUS rising slew rate, 1mV/us VBUS falling slew rate; Vout slew rate=Vref_slew rate*Feedback resistor ratio (20)

Address 0x19H: PWR_CTL2

Bit	Type	Bit Name	Default	Description
7	R/W	EN_VBUS	0b	Enable the power converter output directly, even the Type-C sink device is not attached: 0b: Default, power converter's on/off status is controlled by Type-C controller. 1b: Power converted will be enabled.
6	R/W	PPS_MIN_SEL	0b	This bit controls the 3.3V or 5V minimum PPS voltage. 0b: 5V min PPS voltage application. 1b: 3.3V min PPS voltage application.
5:3	R/W	OTW1_THRESHOLD	000b	Set over temperature warning threshold: 000b: Disable OTW function 001b: 105degC 010b: 115degC 011b: 125degC 100b: 135degC 101b: 145degC 110b: 155degC 111b: 165degC Default value "000"; The OTW warning has 20degC hysteresis for recover.
2:0	R/W	OTP_THRESHOLD	010b	Set over temperature shutdown threshold: 000b: 155degC 001b: 165degC 010b: 175degC 011b: 185degC 100-111b: Reserved Default value "010"; The OTP has 20degC hysteresis for recover.

Address 0x1A: VOUT_L

Bit	Type	Bit Name	Default	Description
7:0	R/W	VOUT_L	0x96	Vout=V*20 +2000 mV V is a 10 bit unsigned binary integer of VOUT[9:0]. V's range is from 0 to 1023; The Vout resolution or minimum step is 20mV.

Address 0x1B: VOUT_H

Bit	Type	Bit Name	Default	Description

7:4	RESERVED			
3:2	R/W	VIN_OVP	10b	00b：disable 01b：17.1V 10/11b：29.5V
1:0	R/W	VOUT_H	0b	Vout=V*20 +2000 mV V is a 10 bit unsigned binary integer of VOUT[9:0]. V's range is from 0 to 1023; The Vout resolution or minimum step is 20mV.

Address 0x1C: IOUT_LIM

Bit	Type	Bit Name	Default	Description
7	RESERVED			
6:0	R/W	IOUT_LIM	0x48	Buck-Boost output CC current limit setting in 50mA units. Default is 3.6A. or "0x48"

Address 0x1D: CTL_SYS0

Bit	Type	Bit Name	Default	Description
7:1	RESERVED			
0	R/W	GO_BIT	0b	0b: Vout/Iout_Ilimit will not change; 1b: Vout/Iout_Ilimit changes based on VOUT/IOUT_LIM register setting, after VOUT/IOUT_LIM scaling finishes, this bit reset to 0 automatically.

Address 0x1E: CTL_SYS1

Bit	Type	Bit Name	Default	Description
7	R/W	SEND_SRC_CAP	0b	Send Source capability message. Write “1” to this bit can force the SC87550AQ sends Src_cap message, this bit auto resets to “0” after Src_cap message is sent out.
6	RESERVED			
5:4	R/W	EN_OFF_TIMER	0b	Set different EN off timer. When pull down EN pin, the chip will delay below timer then shutdown. If EN is pull high during below counter increasing, the counter will be reset. 00b: no delay; 01b: 20 minutes; 10b: 40 minutes; 11b: 120 minutes.
3:0	R/W	I2C_SLAVE_ ADDRESS	1b	Set I2C slave address I2C slave address is (0x61|(I2C_SLAVE_ADDRESS))(7BIT)

Address 0x1F: CTL_SYS2

Bit	Type	Bit Name	Default	Description
7:5	R/W	GPIO1	011b	Set the GPIO1 pin function: 000b: Power_Share 1 function. Refer to detail description of power sharing. 001b: GATE function for GND short battery protection drive; 010b: FLT function which indicates a fault has happened when pull-low. Fault condition includes OCP, OTP, GND/DP/DM/CCx Short to battery. Open drain output. OTP: means TSD happens, Fault will be pulled low. 011b: NTC2 function. When this function is selected, the power share input is controlled by NTC2. NTC_Mode bit doesn’t control NTC2 behavior. NTC_HYSTERESIS sets the hysteresis. 100/101b: Attach_FLT_ALT. open drain output. It pull-low for 12μs at attach rising edge if no fault event occurs. When fault happens, it pull-low. 111b: Current monitor output. Represent signal between ISENS+ and ISENS-.
4:2	R/W	GPIO2	010b	Set the GPIO2 pin function: 000b: Independent communication alert, open drain output, active low. 001b: POL function which indicates the Type-C plug's polarity.

				Open drain output. When CC1 is selected as CC line, the POL is pull-low; When CC2 is selected as CC line or unattached, the POL is open drain. 010b: NTC function. It's an input pin to sense external thermal. Refer to NTC function description 011b: VCONN_IN function. Apply a 5V/1.5W power supply on this pin. 100b: LED_PWM Output. It's a 25kHz PWM signal output with duty cycle adjustable. Refer to LED_PWM_DUTY register. 101b: Attach. To indicate the Type-C port is attached or unattached. Only high or low two states. 110b: Power_Share 2 function. GPIO2 power share is triggered when GPIO2 voltage is higher than 1.87V. Refer to detail description of power sharing.
1	R/W	I2C_CTL_VOUT_EN	0b	Enable control of I2C register 0x1A, 0x1B 0x1C and 0x1D: 0b: Vout and Iout limit will not change even send command to VOUT_L, VOUT_H, Go_BIT and ILIMIT. The Vout voltage is controlled by USB PD engine. 1b: Vout changes based on VOUT/Iout_CC register setting.
0	R/W	RSNS	1b	Select the RSNS resistor value 0b: 5mR, Current Sense Gain=40, Current Monitor Gain=60, 1b: 10mR, Current Sense Gain=20, Current Monitor Gain=30,

Address 0x20: CTL_SYS3

Bit	Type	Bit Name	Default	Description
7:0	R/W	PS_PDP	0x3C	Those bits set the threshold of PDO power rating reduce to. When the GPIO (If GPIO is set as Power_SHARE function) is pull low, the IC's PD power will reduce to PS_PDP setting. "0x01" means "0.5Watt"; "0xFF" means "127.5Watt".

Address 0x21: CTL_SYS4

Bit	Type	Bit Name	Default	Description
7:0	R/W	PS_PDP_SEL	0xBE	Those bits select which voltage is enabled in the PDO list. Refer to Address 4. Final PDO current is determined by PS_PDP. Default is: 5V/9V/15V/20V/3.3-5.9V/3.3V-11V/3.3V-16V

Address 0x22: CTL_SYS5

Bit	Type	Bit Name	Default	Description
7	RESERVED			
6	R/W	PPS_3A_5A	0b	Set the maximum current of APDO after enter power share, Vbatt low, OTW or NTC state. 0b: 3A 1b: 5A - which requires 5A cable.
5:3	R/W	OC_BLANK_TIMER	100b	Set the blank time when the output CC over current is reached: 000b: 6.25us 001b: 2ms; 010b: 4ms; 011b: 8ms 100b: 12ms; 101b: 16ms; 110b: 24ms; 111b: 32ms
2	R/W	BB2T_REG	0b	Set frequency in Buck-boost mode 0b: Reduce frequency to half of Buck and Boost mode 1b: keep the same frequency as Buck and Boost mode
1:0	R/W	PD_CAP_PEAK _CURRENT	0b	Enable/disable peak current 1-3 capability in the Source_cap_extend message 00b: Not support 01b: Support peak current 1 10b: Support peak current 1-2 11b: Support peak current 1-3

Address 0x23: CTL_SYS6

Bit	Type	Bit Name	Default	Description
7:0	R/W	VBATT_LOW1_PDP	0x5A	Set the maximum power rating when Vbattery is lower than 1st threshold. PDP will reduce to this setting. "0x01" means "0.5Watt"; "0xFF" means "127.5Watt".

Address 0x24: CTL_SYS7

Bit	Type	Bit Name	Default	Description
7:0	R/W	VBATT_L1_PDP_SEL	0xBE	Those bits select which voltage is enabled in the PDO list. Refer to Address 4. Final PDO current is determined by PDP_L. Default is: 5V/9V/15V/20V/3.3-5.9V/3.3V-11V/3.3V-16V

Address 0x25: CTL_SYS8

Bit	Type	Bit Name	Default	Description
7:0	R/W	VBATT_LOW2_PDP	0x1E	Set the maximum power rating when Vbattery is lower than 1st threshold. PDP will reduce to this setting. "0x01" means "0.5Watt"; "0xFF" means "127.5Watt". Default value is 15W.

Address 0x26: CTL_SYS9

Bit	Type	Bit Name	Default	Description
7:0	R/W	VBATT_L2_PDP_SEL	0xBE	Those bits select which voltage is enabled in the PDO list. Refer to Address 4. Final PDO current is determined by PDP_L. Default is: 5V/9V/15V/20V/3.3-5.9V/3.3V-11V/3.3V-16V

Address 0x27: CTL_SYS10

Bit	Type	Bit Name	Default	Description
7:0	R/W	OTW1_PDP	0x3C	Set the maximum power rating when die temp is lower than threshold. PDP will reduce to this setting. "0x01" means "0.5Watt"; "0xFF" means "127.5Watt".

Address 0x28: CTL_SYS11

Bit	Type	Bit Name	Default	Description
7:0	R/W	OTW1_PDP_SEL	0xBE	Those bits select which voltage is enabled in the PDO list. Final PDO current is determined by PDP_L. Default is: 5V/9V/15V/20V/3.3-5.9V/3.3V-11V/3.3V-16V.

Address 0x29: CTL_SYS12

Bit	Type	Bit Name	Default	Description
7:0	R/W	OTW2_NTC_PDP	0x5A	Set the maximum power rating when die temp is lower than threshold. PDP will reduce to this setting. "0x01" means "0.5Watt"; "0xFF" means "127.5Watt".

Address 0x2A: CTL_SYS13

Bit	Type	Bit Name	Default	Description
7:0	R/W	OTW2_NTC_PDP_SEL	0xBE	Those bits select which voltage is enabled in the PDO list. Refer to Address 4. Final PDO current is determined by PDP_L. Default is: 5V/9V/15V/20V/3.3-5.9V/3.3V-11V/3.3V-16V

Address 0x2B: CTL_SYS14

Bit	Type	Bit Name	Default	Description
7:4	R/W	VBATT_LOW_THLD1	0x8	Those bits set the threshold of input voltage detection.

				b[3:0] Input Voltage Falling 0x0: This function is disabled 0x1: 12.6V 0x2: 12.2V 0x3: 11.8V 0x4: 11.4V 0x5: 11V 0x6: 10.6V 0x7: 10.2V 0x8: 9.8V 0x9: 9.4V 0xA: 9V 0xB: 8.6V 0xC: 8.2V 0xD: 7.8V 0xE: 7.4V 0xF: 7V
3:0	R/W	VBATT_LOW_THLD2	0xC	Those bits set the threshold of input voltage detection 0x0 This function is disabled 0x1: 11.8V 0x2: 11.4V 0x3: 11V 0x4: 10.6V 0x5: 10.2V 0x6: 9.8V 0x7: 9.4V 0x8: 9V 0x9: 8.6V 0xA: 8.2V 0xB: 7.8V 0xC: 7.4V 0xD: 7V 0xE: 6.6V 0xF: 6.2V

Address 0x2C: CTL_SYS15

Bit	Type	Bit Name	Default	Description
7:4	R/W	VBATT_LOW_THLD3	0xA	Those bits set the threshold of input voltage detection. Refer to detail description of battery low operation. b[3:0] Input Voltage Falling 0x0: This function is disabled 0x1: 9.8V 0x2: 9.4V 0x3: 9V 0x4: 8.6V 0x5: 8.2V 0x6: 7.8V 0x7: 7.4V 0x8: 7V 0x9: 6.6V 0xA: 6.2V 0xB: 5.8V 0xC: 5.4V 0xD: 5V 0xE: 4.6V 0xF: 4.2V
3:2	R/W	VBATT_LOW_BLK	10b	Set the Vbattery low 1, Vbattery low2 and Vbattery low3 blank time: 00b: 10ms 01b: 160ms 10b: 320ms 11b: 640ms
1:0	R/W	VCONN_OCP_BLK	10b	00b: 3.125 + 3.125 01b: 6.25 + 3.125us 10b: 18.75us+ 3.125us 11b: 43.75 + 3.125us (+3.125 means time till vconn turn-off)

Address 0x2D: CTL_SYS16

Bit	Type	Bit Name	Default	Description

7:4	RESERVED			
3:1	R/W	OTW2_THRESHOLD	0b	Set over temperature warning threshold: 000b: Disable OTW function 001b:105degC 010b:115degC 011b:125degC 100b:135degC 101b:145degC 110b:155degC 111b:165degC The OTW warning has 20degC hysteresis for recover
0	R/W	VCONN_OCP_EN_SYN	0b	0b: vconn ocp en is active after vconn on 1b: vconn ocp en and vconn are active together

Address 0x2E: CTL_SYS17

Bit	Type	Bit Name	Default	Description
7	R/W	PEAK_CL	0b	Set the high-side peak current limit in Boost mode 0b:10.5A 1b:14.5A
6:5	R/W	INCC_BLK	1b	Set entering CC loop blanking time 00b: 6.25us 01b: 128us 10b: 400us 11b: 5ms
4	R/W	NTC_HYSTERESIS	1b	Set the NTC thermal recovery hysteresis: 0b: 10% 1b: 20% This bit controls both NTC and NTC2.
3	R/W	NTC_MODE	1b	Set the behavior when NTC function is triggered: 0b: Shutdown. 1b: Reduce PD power to OTW2_NTC_PDP set value.
2	R/W	VOUT OVP	1b	Set whether the output OVP function is active 0b: Disable output OVP function 1b: Enable output OVP function
1:0	R/W	VBUS_VOLTAGE	11b	Set default V_{BUS} voltage: 00b: 5.00V; 01b: 5.06V; 10b: 5.10V; 11b: 5.16V.

Address 0x2F: CTL_SYS18

Bit	Type	Bit Name	Default	Description
7	RESERVED			
6:0	R/W	LED_PWM_DUTY	0x32	Set the LED_PWM output duty cycle. Minimum value is 5%, maximum is 100%. 0x05: 5%; 0x64: 100%.

Address 0x30: STATUS1

Bit	Type	Bit Name	Default	Description
7	R	ATTACHED	0b	Sink device is attached or not: 0b: Unattached; 1b: Attached.
6	R	NTC2_ENTER	0b	NTC2 event is entered or not: 0b: Not enter; 1b: Entered.
5	R	POL	0b	Type-C polarity indication: 0b: CC1 is selected as CC line; 1b: CC2 is selected as CC line.
4	R	SHORT_VBATT	0b	Output bus voltage status indication: 0b: Normal state; 1b: DP/DM/CC1/CC2 or USB_GND is shorted with battery voltage.
3	R	FAULT	0b	FLT function indicates a fault has happened. Fault condition includes OCP, OTP, GND/DP/DM/CCx Short to battery.

				0b: No fault. 1b: One or more fault events occur.
2	R	VCONN STATUS	0b	0b: VCONN is off 1b: VCONN is on
1	R	CC_CV	0b	Output power status: 0b: CV state; 1b: output is in CC current limit state.
0	R	NTC_ENTER	0b	NTC event is entered or not: 0b: Not enter; 1b: Entered.

Address 0x31: STATUS2

Bit	Type	Bit Name	Default	Description
7	R	VBATT_LOW1_FLAG	0b	Sink device is attached or not: 0b: Unattached; 1b: Attached.
6	R	VBATT_LOW2_FLAG	0b	NTC2 event is entered or not: 0b: Not enter; 1b: Entered.
5	R	OTW1	0b	Over temperature warning indication: 0b: Not in over temp warning; 1b: In over temp warning state.
4	R	OTW2	0b	over temperature warning indication: 0b: Not in over temp warning; 1b: In over temp warning state. .
3:1	R	SELECTED_ PDO_INDEX	0b	Report the Sink selected PDO index: 0b: No PD contract; 1-7: PDO 1 to 7 is selected.
0	R	PDO_TYPE	0b	Indicate the Sink selected PDO is Fixed PDO or APDO (PPS): 0b: Fixed PDO; 1b: APDO.

Address 0x32: STATUS3

Bit	Type	Bit Name	Default	Description
7:0	R	Contract Power	0b	PD contracted power in 0.5W unit. Fix PDO: Calculate using Voltage * Maximum Current; PPS: Calculate using Request Voltage * Request Current. If no PD contract, the value is 7.5W or 15W depending on Rp.

Address 0x35: FW_REV

Bit	Type	Bit Name	Default	Description
7:6	RESERVED			
5	R	CABLE_CAP	0b	1b: It is 5A cable; 0b: Cable can handle 3A only.
4:0	RESERVED			

Address 0x36: MAX_FEQ_CUR

Bit	Type	Bit Name	Default	Description
7:0	R	MAX_REQ_CUR	0b	Sink max requested operation current (Mismatch bit=1) in 20mA unit, only valid when Givebackflag=0, Fix PDO

15 Configuration Table

Table2 OTP Description

OTP Items	Description	Value
PDP_SELECT	Set SC87550AQ output power	1: 15W 2: 18W 3: 20W 4: 27W 5: 30W 6: 33W 7: 40W 8: 45W 9: 50W 10: 60W 11: 65W 12: 67W 13: 80W 14: 88W 15: 100W
GPIO1	Configures the GPIO1 pin's function.	0: Power_Share 1 1: GATE 2: fault 3: NTC2 4: Attach_FLT_ALT 5: Attach_FLT_ALT 6: NA 7: IMON
GPIO2	Configures the GPIO2 pin's function.	0: INT_ALT 1: POL 2: NTC 3: VCONN_IN 4: LED_PWM 5: ATTACH 6: POWER_SHARE2 7: NA
OTP_THLD	Sets the over-temperature shutdown threshold.	0: 155degC 1: 165degC 2: 175degC 3: 185degC
OTW1_THLD	Sets-the over temperature warning threshold.	0: Disable OTW function 1: 105degC 2: 115degC 3: 125degC 4: 135degC 5: 145degC 6: 155degC 7: 165degC
OTW1_PDO_SELECT	Sets the maximum power rating when the die temp rises above its threshold.	1: 15W 2: 18W 3: 18W 4: 18W 5: 18W 6: 18W 7: 27W 8: 20W 9: 30W 10: 45W 11: 45W 12: 45W 13: 60W 14: 65W 15: 80W
OTW2_THLD	Sets the over-temperature warning threshold.	0: Disable OTW function 1: 105degC 2: 115degC 3: 125degC 4: 135degC

		5: 145degC 6: 155degC 7: 165degC
OTW2_NTC_PDO_SELECT	Sets the maximum power rating when the die temp rises above its threshold.	1: 15W 2: 15W 3: 15W 4: 15W 5: 15W 6: 15W 7: 15W 8: 15W 9: 20W 10: 20W 11: 20W 12: 27W 13: 45W 14: 45W 15: 45W
NTC_HYSTERESIS	Sets the NTC thermal recovery hysteresis.	0: 10% 1: 20%
NTC_MODE	Sets the behavior when the NTC is triggered.	0: Shutdown device 1: Reduce PD power to OTW2_NTC_PDP set value
VBATT_LOW_THLD1	Sets the first threshold for VIN detection.	0: This function is disabled 1: 12.6V 2: 12.2V 3: 11.8V 4: 11.4V 5: 11V 6: 10.6V 7: 10.2V 8: 9.8V 9: 9.4V 10: 9V 11: 8.6V 12: 8.2V 13: 7.8V 14: 7.4V 15: 7V
VBATT_LOW_THLD2	Sets the second threshold for VIN detection.	0: This function is disabled 1: 11.8V 2: 11.4V 3: 11V 4: 10.6V 5: 10.2V 6: 9.8V 7: 9.4V 8: 9V 9: 8.6V 10: 8.2V 11: 7.8V 12: 7.4V 13: 7V 14: 6.6V 15: 6.2V
VBATT_LOW_THLD3	Sets the third threshold for VIN detection. The device shuts down after this threshold is triggered.	0: This function is disabled 1: 9.8V 2: 9.4V 3: 9V 4: 8.6V 5: 8.2V 6: 7.8V 7: 7.4V 8: 7V 9: 6.6V 10: 6.2V 11: 5.8V 12: 5.4V 13: 5V 14: 4.6V

		15: 4.2V
VBATT_LOW_BLK	Sets the VBATT low 1 and VBATT low 2 blank times.	0: 10ms 1: 160ms 2: 320ms 3: 640ms
VBATT_LOW1_PDO_SELECT	Sets the maximum power rating when VBATT falls below its first threshold.	1: 15W 2: 18W 3: 18W 4: 18W 5: 18W 6: 18W 7: 27W 8: 20W 9: 30W 10: 45W 11: 45W 12: 45W 13: 60W 14: 60W 15: 65W
VBATT_LOW2_PDO_SELECT	Sets the maximum power rating when VBATT falls below its first threshold.	0 to 15: 15W
POWER_SHARE_PDO_SELECT	Set the thresholds to which the PDO power rating is reduced.	1: 15W 2: 18W 3: 18W 4: 18W 5: 18W 6: 18W 7: 20W 8: 27W 9: 30W 10: 30W 11: 30W 12: 30W 13: 40W 14: 40W 15: 50W
VBUS_VOLTAGE	Sets the default VBUS voltage.	0: 5V 1: 5.06V 2: 5.1V 3: 5.16V
PWM_MODE	Sets the PFM/FPWM mode.	0: FPWM 1: PFM
FREQ	Sets the switching frequency.	1: 280kHz 0: 420kHz 3: 560kHz 2: NA
DITHER	Sets the spread spectrum feature	0: Disable 1: Enable
EN_OFF_TIMER	Sets the EN off timer.	0: no delay 1: 20min 2: 40min 3: 60min
LINE_DROP_COMP	Sets the output voltage compensation vs load feature.	0: No LDC 1: 100mV@3A 2: 300mV@3A 3: 600mV@3A
Additional Line Drop Comp	Output line drop compensation increase 200mV.	0: Disable 1: 200mV
PPS_LDC_EN	Enable line drop compensation even in PPS.	0: Disable 1: Enable
SLEW RATE	Set output slew rate during adjust Vout.	0: 0.1mV/μs 1: 1mV/μs
PEAK_CL	Sets the high-side peak current limit in boost mode.	0: 10.5A 1: 14.5A
RSNS_5m10m	Sets the external CC limit RSENS resistor value.	0: 5m 1: 10m
EX_HS	Select Buck HighSide-Q1 is internal or external	0: Internal 1: External

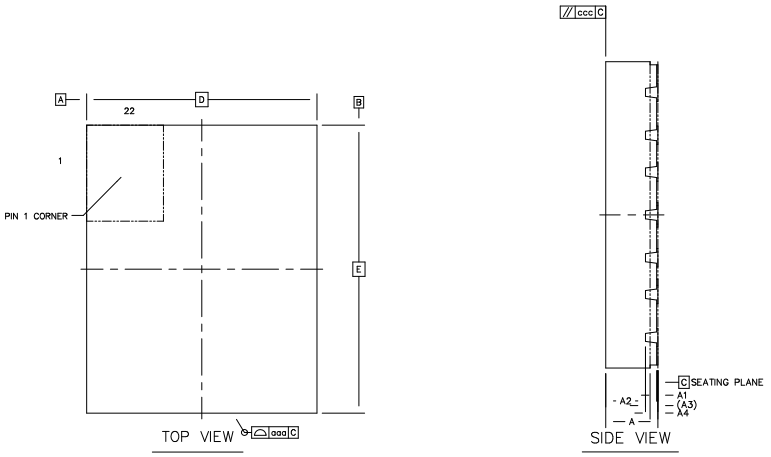
OC_BLANK_TIMER	Sets the blank time when the output over-current condition is reached.	0: disabled 1: 2ms 2: 4ms 3: 8ms 4: 12ms 5: 16ms 6: 24ms 7: 32ms
LEGACY_CHARGING_ MODE_SEL	Selects DPDM Charging mode.	0: AppleMode+1.2VMode+DCP+QC +FCP 1: AppleMode+1.2VMode 2: DCP 3: DCP
SAMSUNG_EN	Whether to En Samsung 1.2V Mode	0: Disable 1: Enable
I2C_SLAVE_ADDRESS	Set I2C slave address	0: 0X61 1: 0X60 2: 0X63 3: 0X62
VIN_OVP	. VIN_OVP function	0: disable 1: 17.1V 2/3: 29.5V
IOUT_LIM	Default output current Limit	0: 3.6A 1: 5.4A

Table3 The different default value of SC87550AQ / SC87550BQ

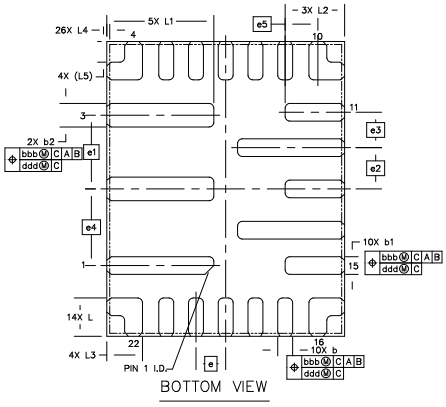
OTP Items	SC87550AQ	SC87550BQ
PDP_SELECT	60W	60W
GPIO1	NTC2	NTC2
GPIO2	NTC	POWER_SHARE2
OTP_THLD	175degC	175degC
OTW1_THLD	Disable OTW function	135degC
OTW1_PDO_SELECT	30W	27W
OTW2_THLD	Disable OTW function	155degC
OTW2_NTC_PDO_SELECT	45W	27W
NTC_HYSTERESIS	20%	20%
NTC_MODE	Reduce PD power to OTW2_NTC_PDP set value	Reduce PD power to OTW2_NTC_PDP set value
VBATT_LOW_THLD1	9.8V	9V
VBATT_LOW_THLD2	7.4V	This function is disabled
VBATT_LOW_THLD3	6.2V	7.8V
VBATT_LOW_BLK	640ms	320ms
VBATT_LOW1_PDO_SELE CT	45W	27W
VBATT_LOW2_PDO_SELE CT	15W	15W
POWER_SHARE_PDO_SE LECT	30W	27W
VBUS_VOLTAGE	5.16V	5.16V
PWM_MODE	FPWM	FPWM
FREQ	420kHz	420kHz
DITHER	Enable	Enable

EN_OFF_TIMER	no delay	no delay
LINE_DROP_COMP	No LDC	No LDC
Additional Line Drop Comp	Disable	Disable
PPS_LDC_EN	Disable	Disable
SLEW RATE	0.1mV/μs	0.1mV/μs
PEAK_CL	10.5A	10.5A
RSNS_5m10m	10m	5m
EX_HS	Internal	Internal
OC_BLANK_TIMER	12ms	12ms
LEGACY_CHARGING_ MODE_SEL	AppleMode+1.2VMode+DCP+QC+FCP	AppleMode+1.2VMode+DCP+QC+FCP
SAMSUNG_EN	Enable	Enable
I2C_SLAVE_ADDRESS	0X61	0X61
VIN_OVP	29.5V	29.5V
IOUT_LIM	3.6A	3.6A

MCHANICAL DATA

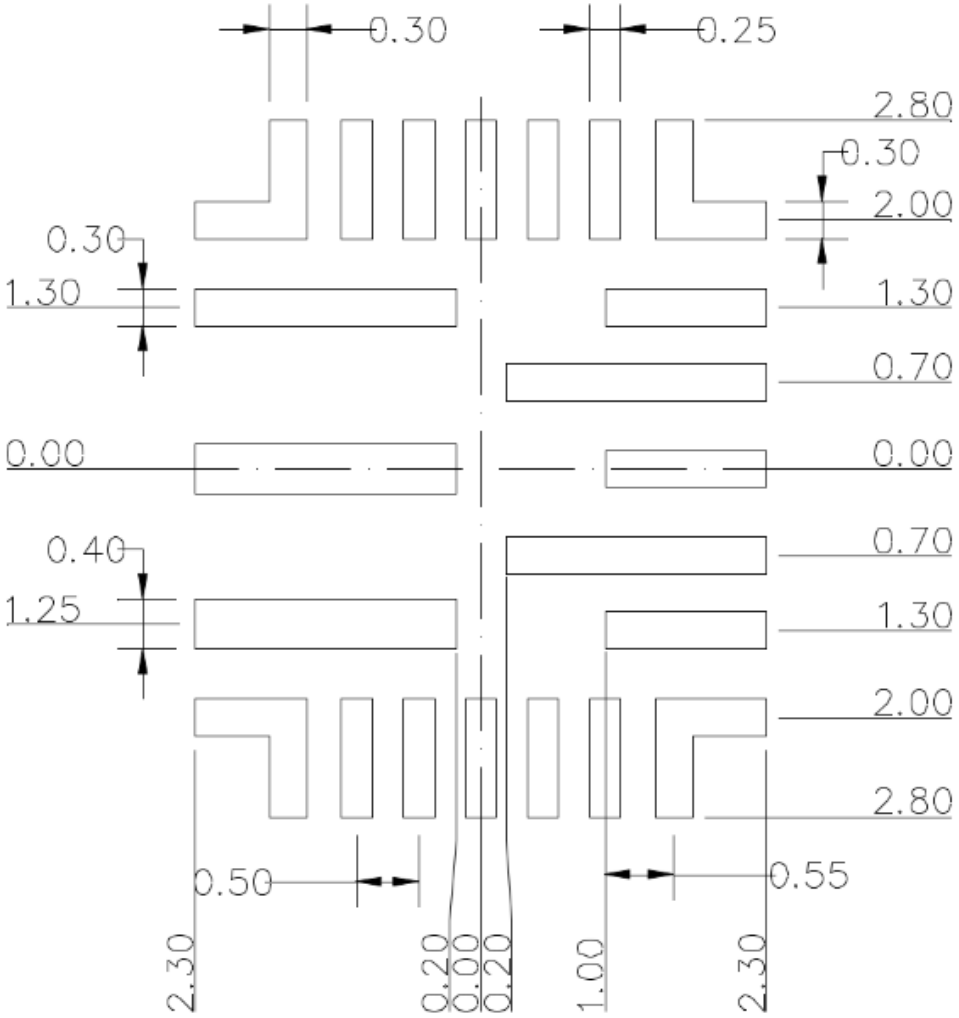


Unit:mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.25	0.3	0.35
		b2	0.35	0.4	0.45
BODY SIZE	X	D		4 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		1.25 BSC	
		e2		0.7 BSC	
		e3		0.6 BSC	
		e4		1.3 BSC	
		e5		0.55 BSC	
LEAD LENGTH		L	0.55	0.65	0.75
		L1	1.7	1.8	1.9
		L2	0.9	1	1.1
		L3	0.5	0.6	0.7
SIDE WETTABLE WIDTH		L4	0.01	---	0.09
LEAD EDGE TO PKG EDGE		L5		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	

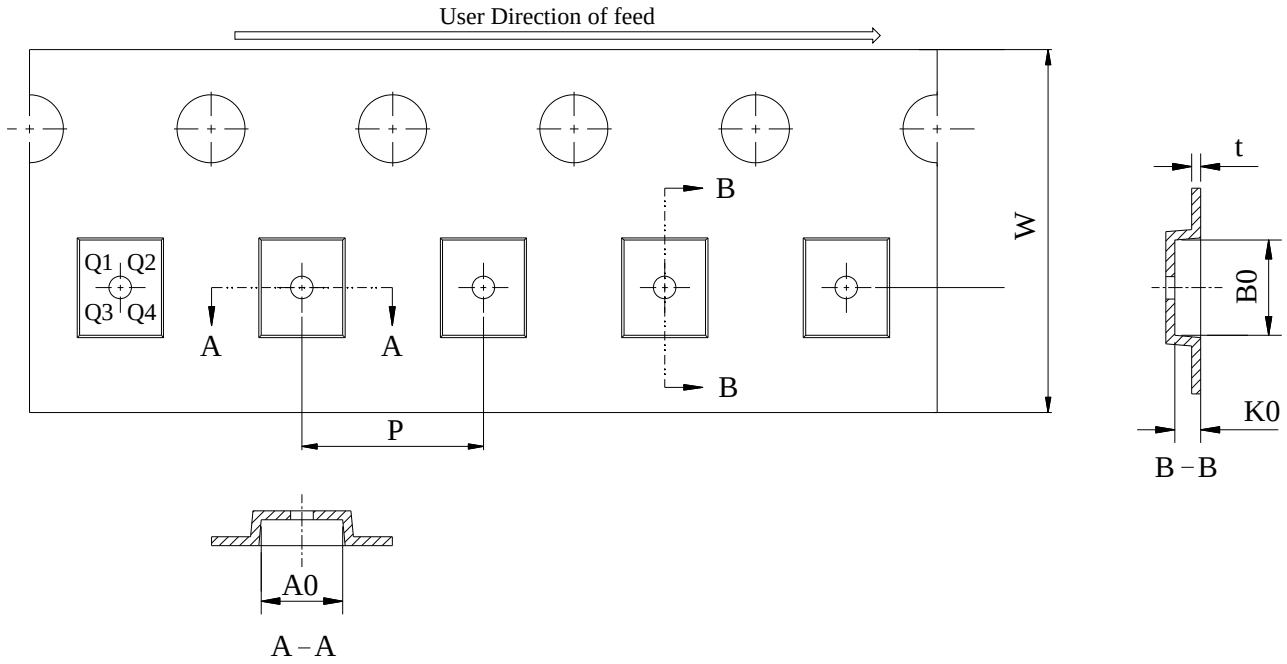
RECOMMENDED FOOTPRINT



Unit: mm

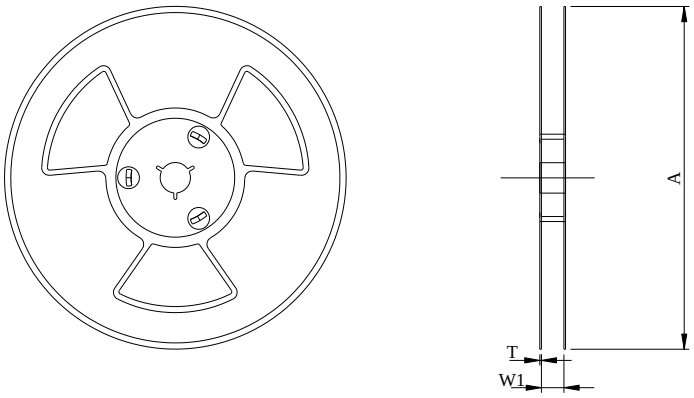
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	$12.0^{+0.3}_{-0.1}$	8.0±0.10	4.25±0.05	5.25±0.05	1.02±0.05	0.25±0.02	Q1

REEL



Item	A	W1	T
Size (mm)	330.0±1.0	$12.4^{+1.0}_{-0.0}$	$2.6^{+1.0}_{-0.0}$

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