

# B650E AORUS PRO X USB4

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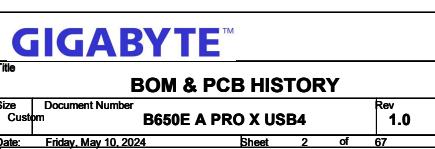
# Model Name: B650E AORUS PRO X USB4

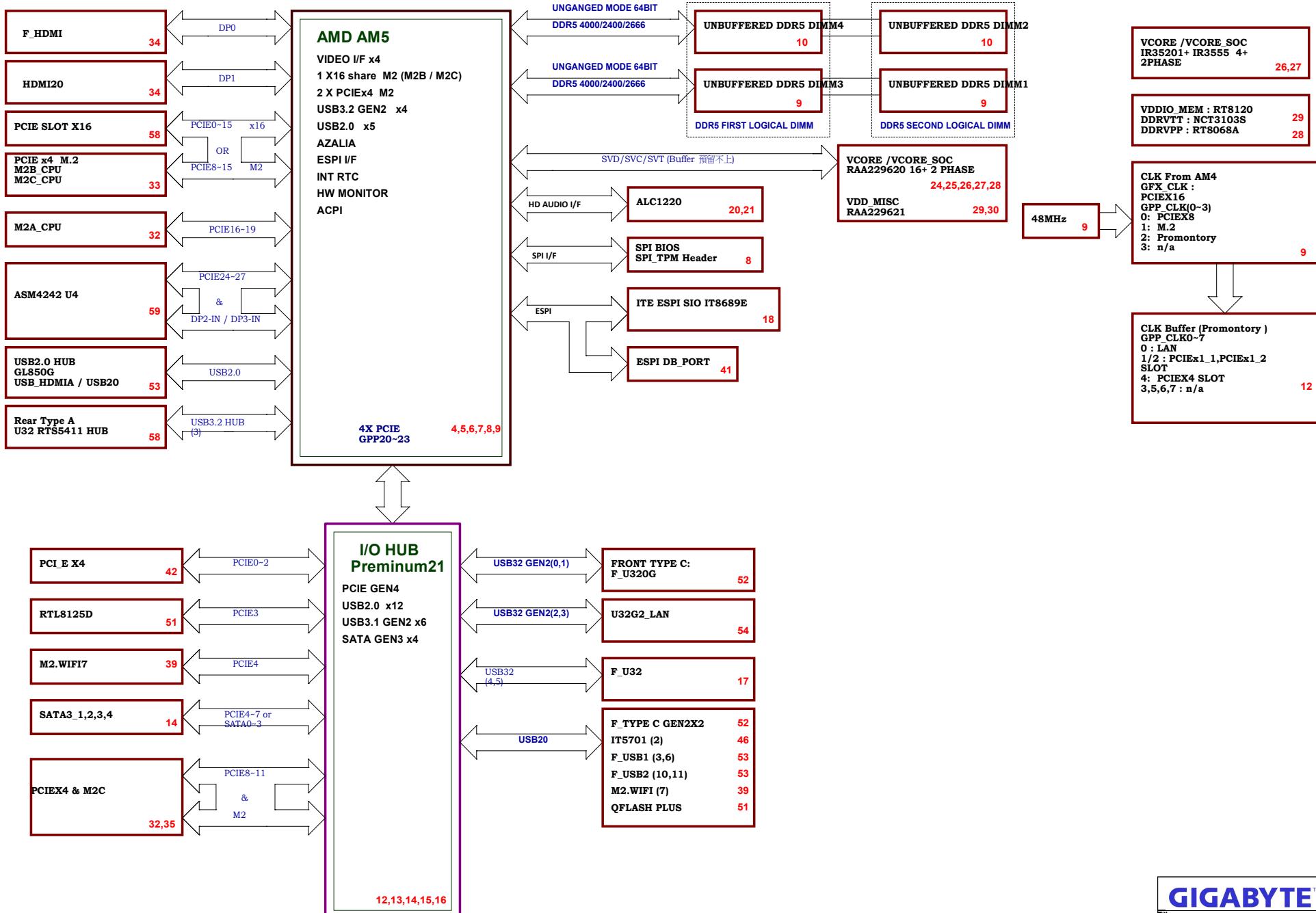
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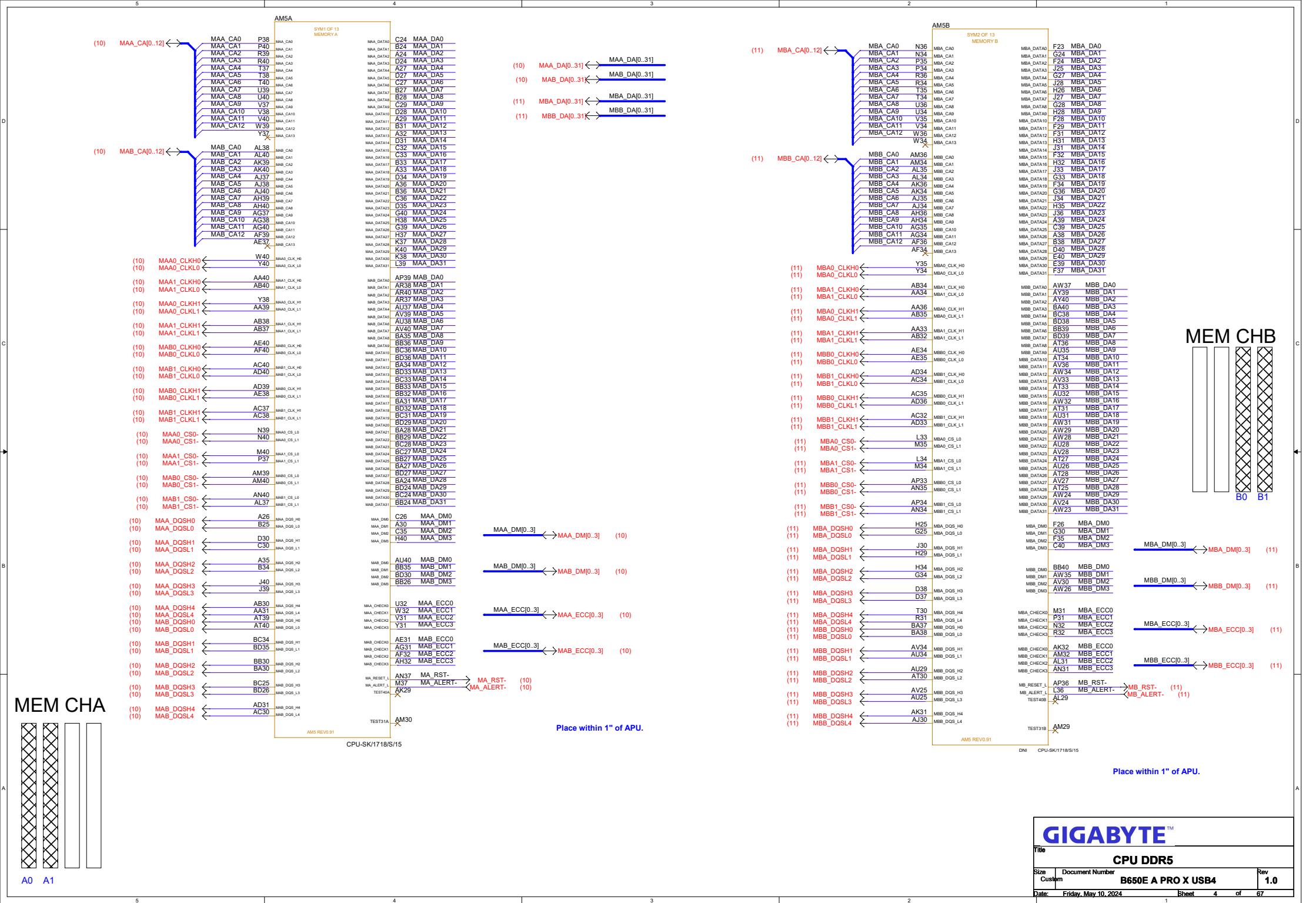
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P-Code: U98126-0

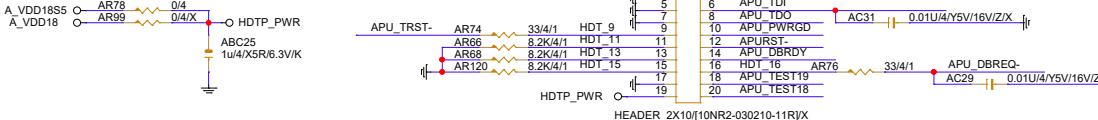
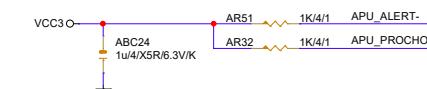
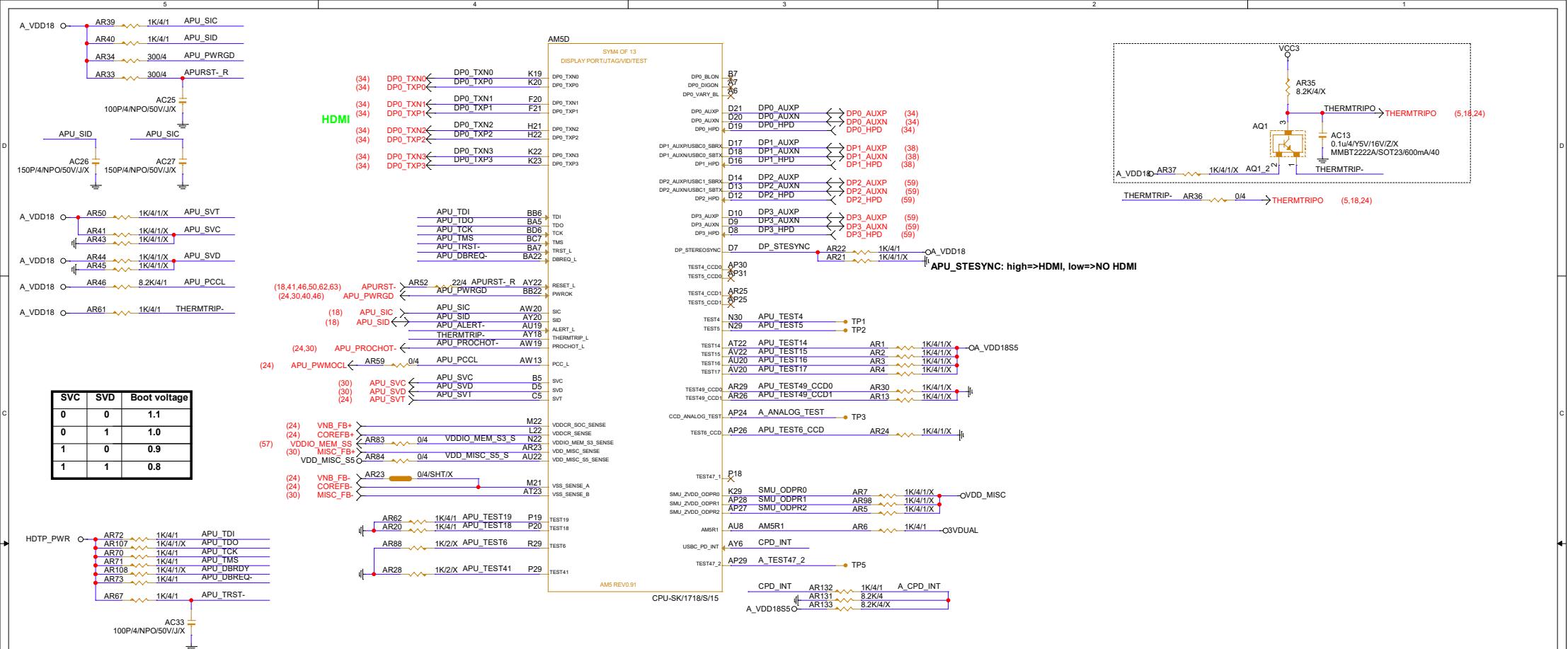
Date	Change Item	Reason
2022.08.25	F-BOM Release .	PCB: 1.0 1. BOM : 10D 2. Location : WIFI_COVER "11KWP-000001-31R"
2022.08.25	F-BOM Release .	PCB: 1.0 1. BOM : 10E 2. Location : RAR2 上件 3. Location : RQ2 NA (DATA BUFFER 單向,會有問題)
2022.09.15	F-BOM Release .	PCB: 1.0 1. BOM : 10F 2. Location : UAU3D1,UAU3D2,UAU3D4,UAU3D5 修改用料為 "10DE2-353124-10R" 3. Location : AR26 上件 pw_sw ac第一次開機"42"燈會滅問題
2022.10.14	F-BOM Release .	PCB: 1.0 1. BOM : 10F 2. ECN , 移除10HP4-112516-40R用料 CHIP LAN I225V B3 INTEL 搭配10HP4-112516-40R有LAN ID無法燒錄問題,移除10HP4-112516-40R,修改為10HP4-112516-50R用料
2023.01.04	A-BOM Release .	PCB: 1.0 BOM : 10G PCB1.0 (ABOM) 1. Location : MAC11_100p to 470p (for CHOKE noise issue) 2. Location : MCUR100 / MCUR19 NA 3. Location : MCUR155 / MCUR157 change to 300/6/ 4. PWM 料號 10TA1-629620-02R --> 10TA1-629620-04R (delay 1ms)
2023.03.27	F-BOM Release . 9MB65EMSR-00-10H	PCB: 1.0 BOM : 10H PCB1.0 (FBOM) 1. Location : DA1_DR3/DA2_DR3/DB1_DR3/DB2_DR3/DC1_DR3/DC2_DR3/DD2_DR3 /DD1_DR3/DE1_DR3/DE2_DR3/DF1_DR3/DF2_DR3/DG1_DR3/DG2_DR3 /DH1_DR3/DH2_DR3 2.2ohm to 4.7ohm 2. MCUR155,MCUR157 300ohm change to 200ohm
2023.03.28	A-BOM Release . 9MB65EMSR-00-10K	PCB: 1.01 1. SPS PIN 3 add 0.1u by on top layer & gen to pin2 2. SPS BOOT PIN 4.7ohm TO 2.2ohm
2023.05.11	P-BOM Release . 9MB65EMSR-00-10K	PCB: 1.01 1. 轉P-BOM,試產50PCS
2023.05.29	ECN Release . 9MB65EMSR-00-10K	PCB: 1.01 1. 0201 0.1u/X6S 新增替料(10CM9-3K1003-76R)
2023.07.14	A-BOM Release . 9MB65EMSR-00-10L	PCB: 1.01 1. RTS5411T -> RTS5411S(FW更新) 2. JY513008 -10R to -11R RQ1 NA, RAR1 0 ohm上件 3. DB_PORT Add 11DL1-020070-73R(耐高溫)
2023.09.21	F-BOM Release . 9MB65EMSR-00-10M	PCB: 1.01 AM5 model PHX CPU hang with Hardware Reset issue 1. FPR9 REMOVE 2. Mother board ID : OR14 change to OR26 3. FAN NCT3947->NCT3948 4. F*R2 & F*C1 NA
2023.12.25	F-BOM Release . 9MB65EMSR-00-10N	PCB: 1.01 Location : PEC1 330u to 470u
2023.12.25	E-BOM Release .	PCB: 0.2 1. U4_RST & U4_WAKE 接至CPU端(P.7) 2. M2A 與 ASM4242 位置對調
2024.04.15	P-BOM Release .	PCB: 1.0 1. Location : ECDR6 要上件,QFLASH PLUS FUNCTION 2. 8851G_INT 搬至agpio11 (ADS) 3. VDDIO_MEM add WBC192 POSCAP 4. DG_U1 VIN 改VCC 5. A_Q5 方向 6. LED_B_33 change to 470/8P4R6 7. MA_L1 0.22->0.15uH (MA_DR18 : 75K-> 69.8K)

## **Circuit or PCB layout change for next version**







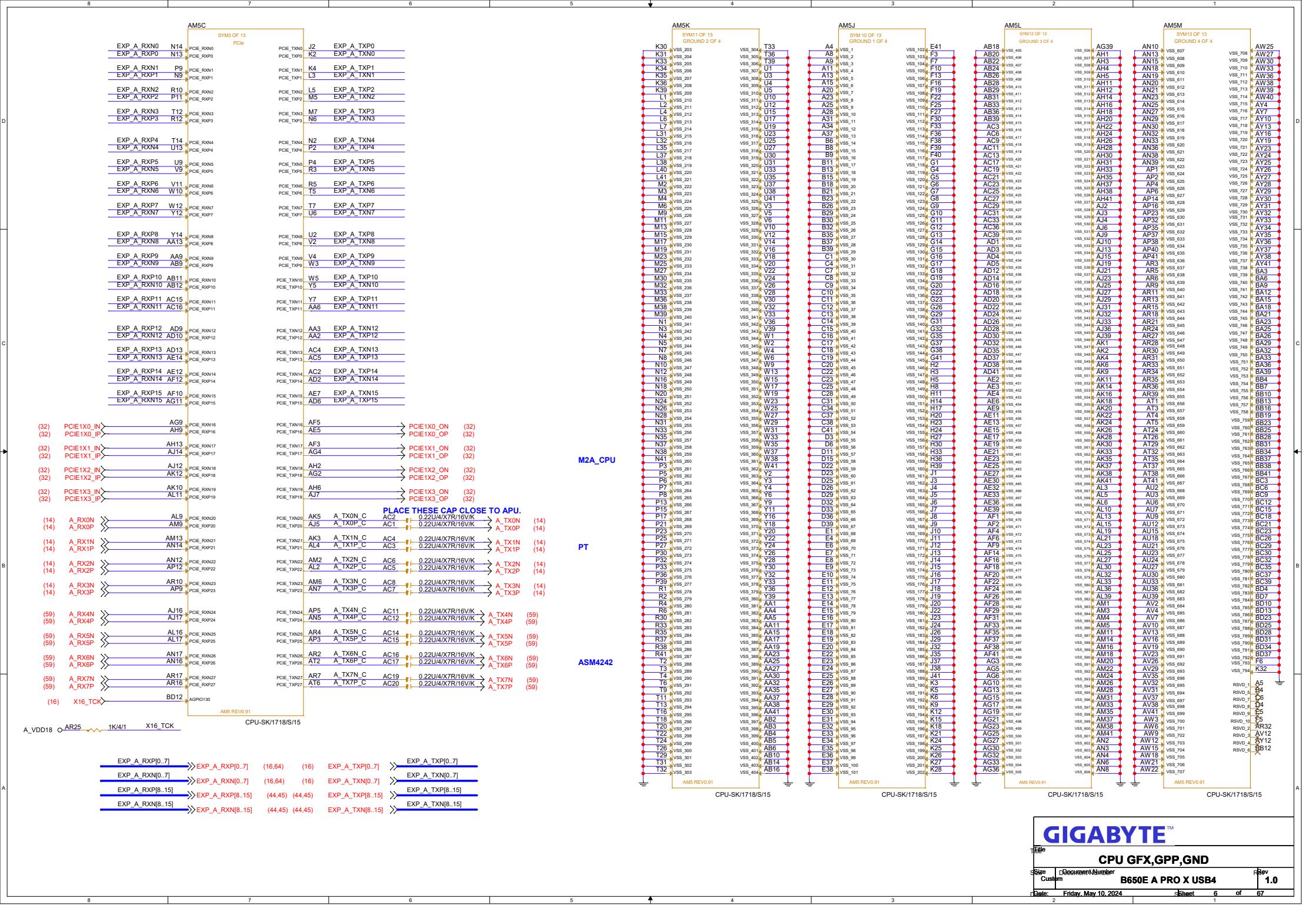


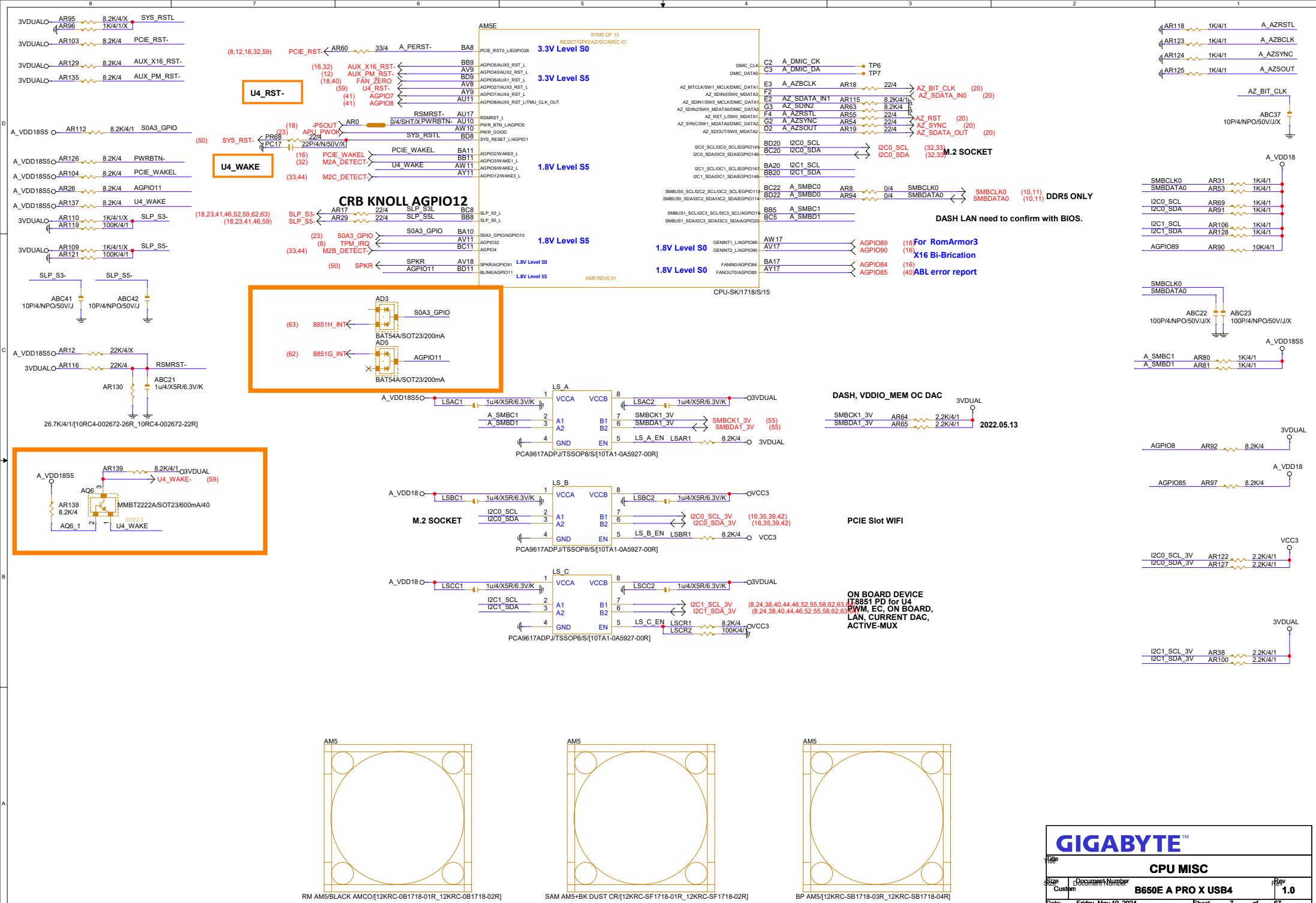
Socket AM5 Processor		
Family / Model	Numbers	AM5 APU TYPE
Family 19h, Model 40h, 4Fh		TYPE 1
Family 19h, Model 60h, 6Fh		TYPE 2
Family 19h, Model 70h, 7Fh		TYPE 3

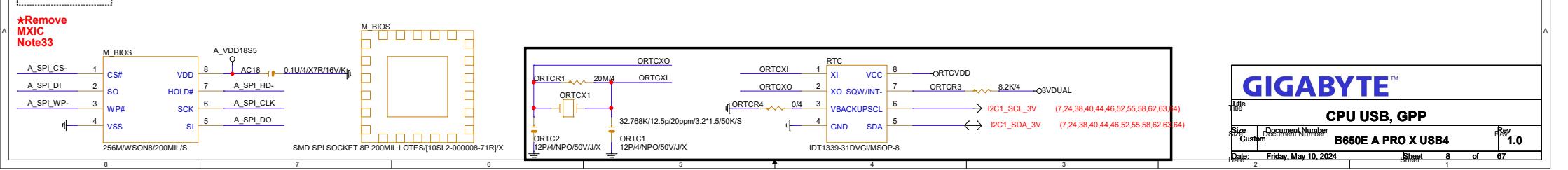
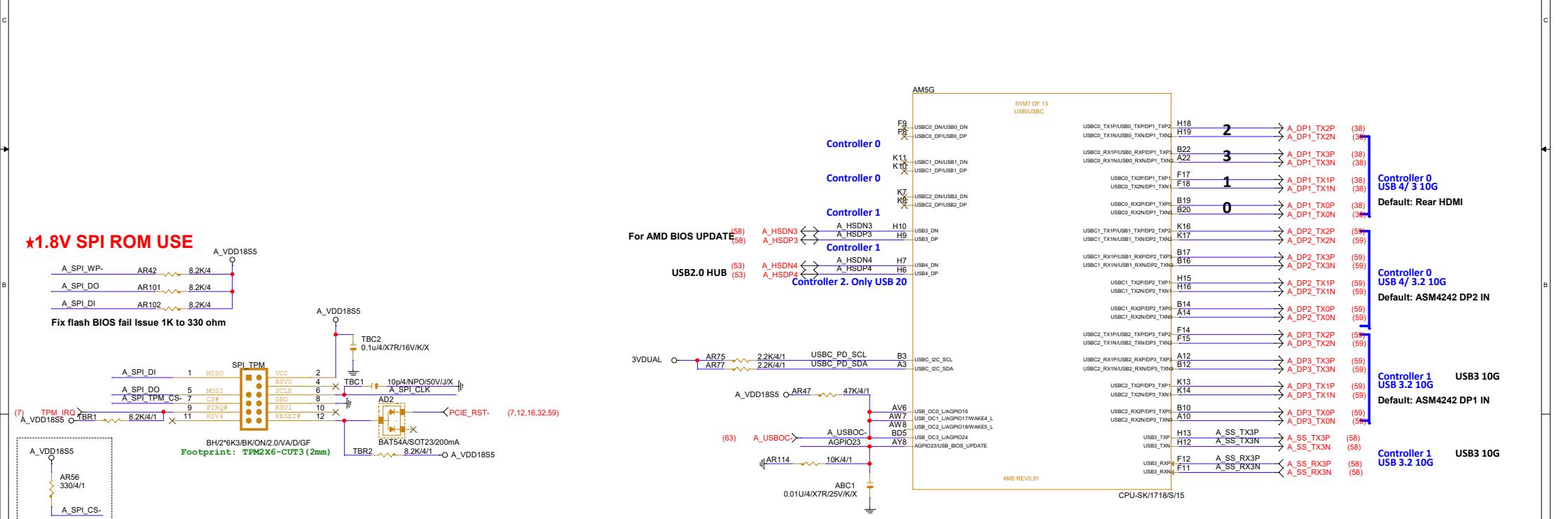
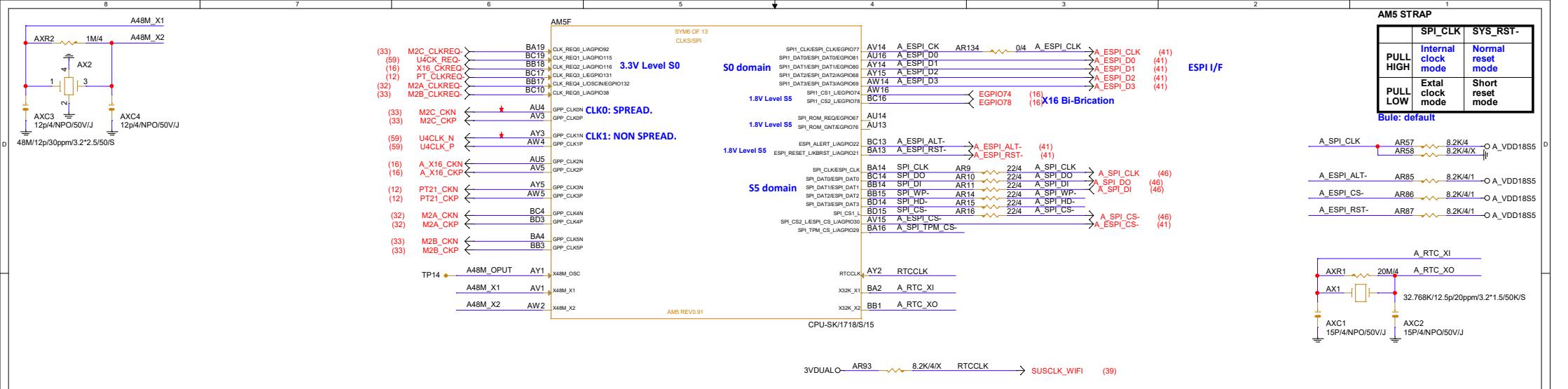
**GIGABYTE**™

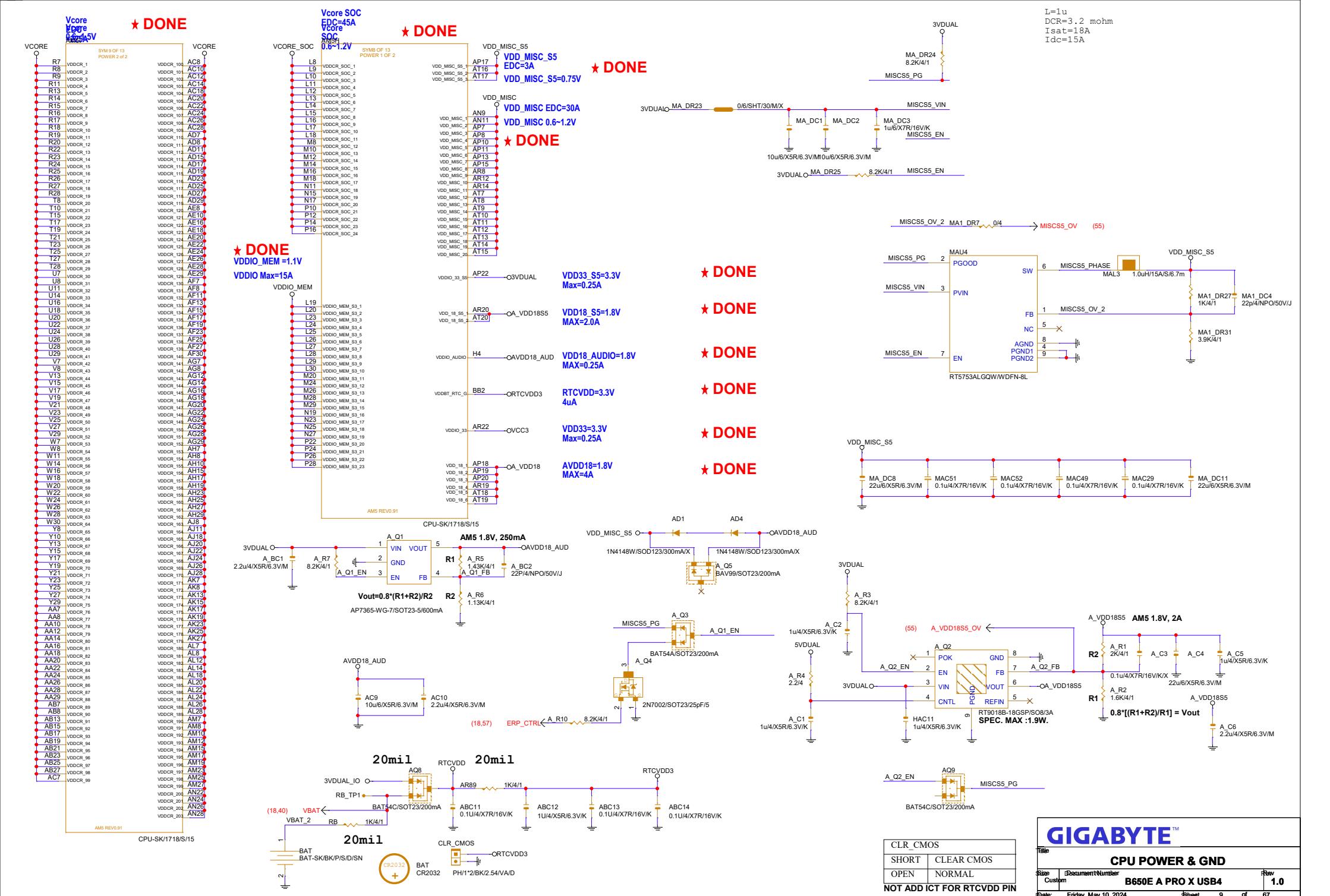
## CPU CONTROL

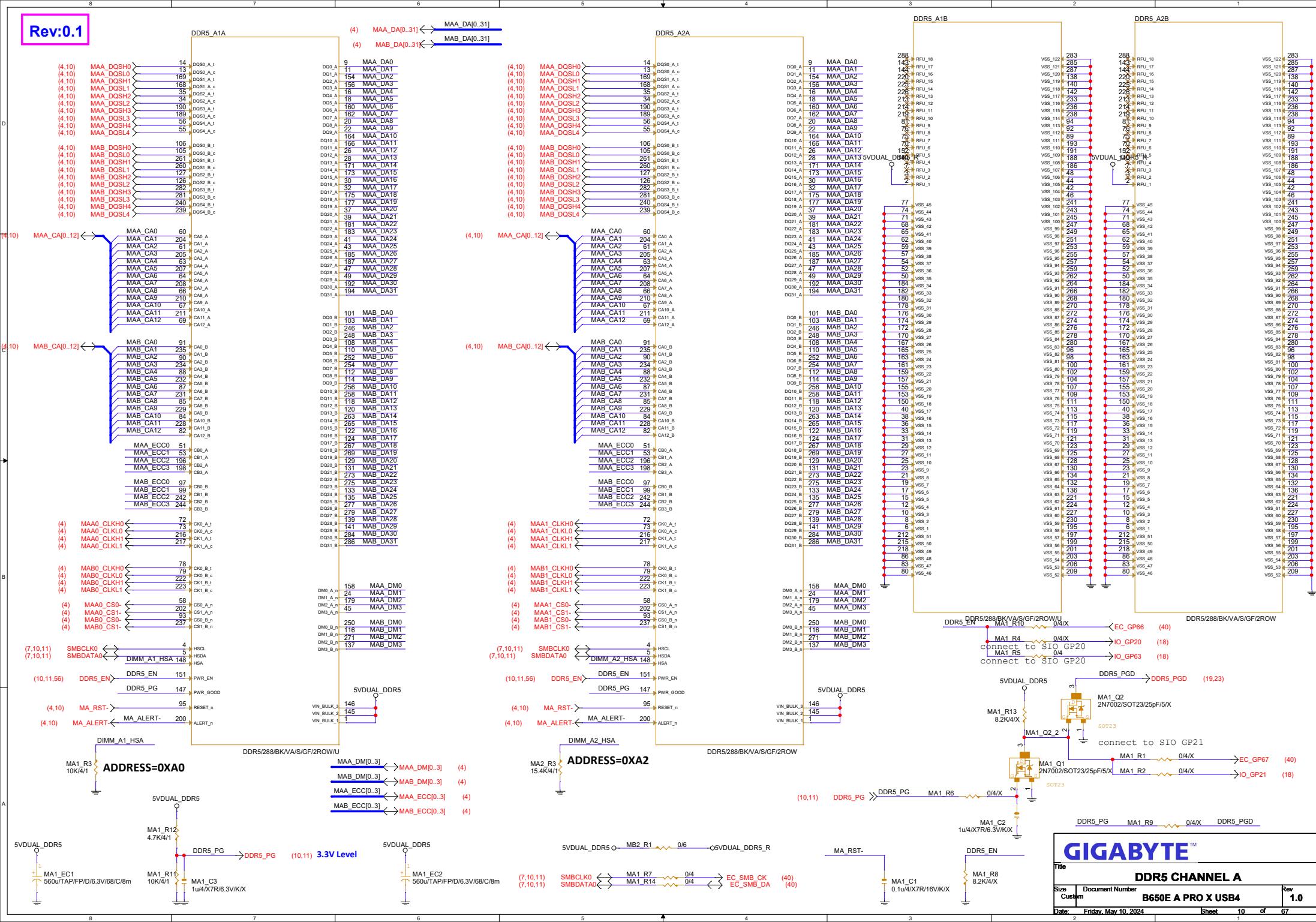
Document Number Custom	Rev 1.0
B650E A PRO X USB4	
Date: Friday, May 10, 2024	Sheet 1 of 67

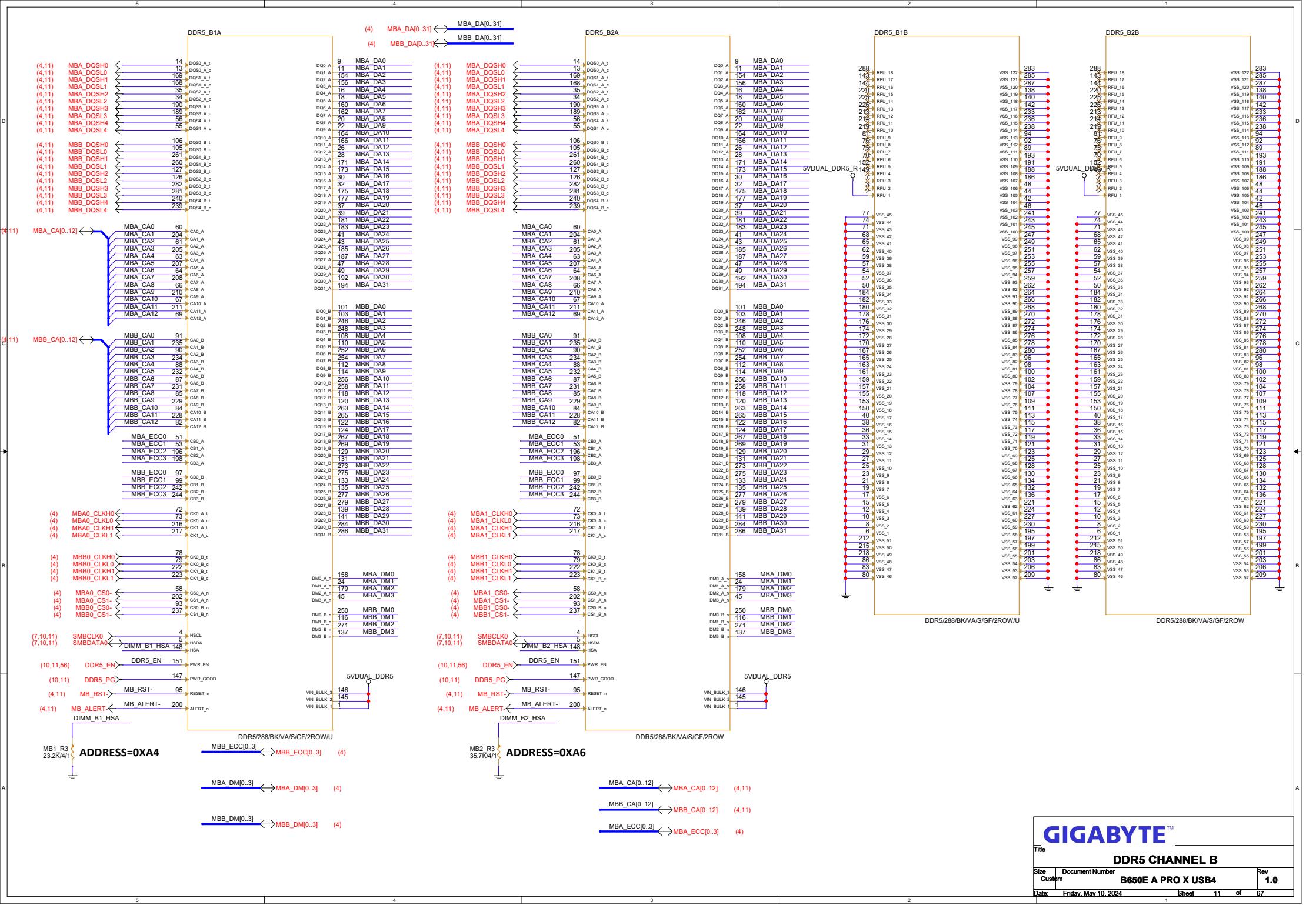












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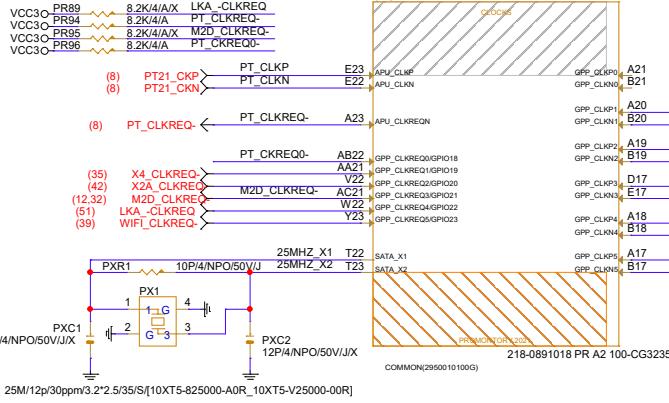
## DDR5 CHANNEL B

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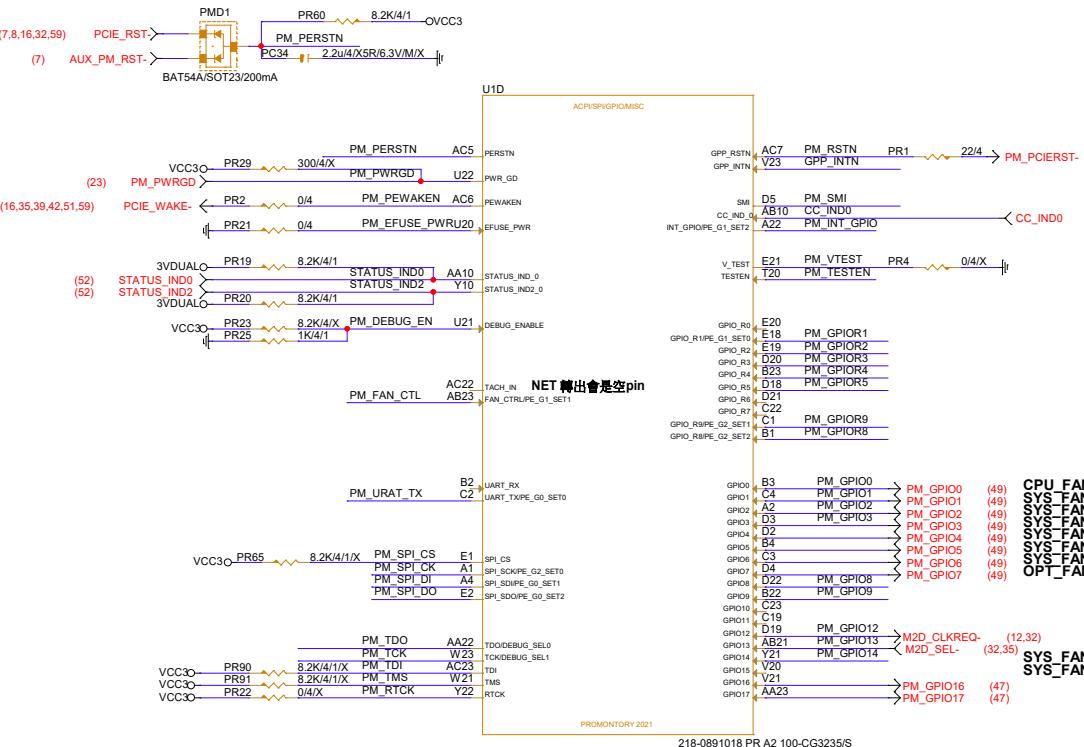
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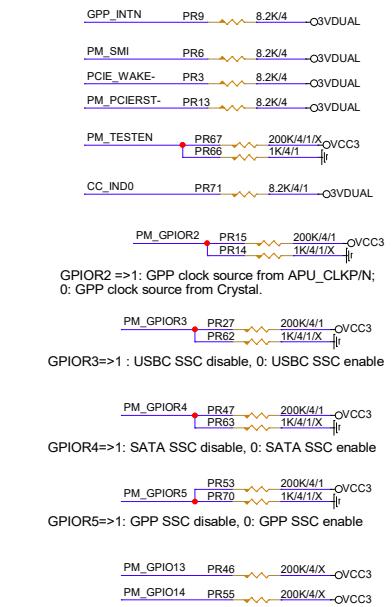
VCC <sub>Q</sub>	PR35 PR36	8.2K4/1/X 1K4/1	PM_INT	GPIO
VCC <sub>Q</sub>	PR39 PR40	200K4/1/X 1K4/1	PM_FAN	CTL
VCC <sub>Q</sub>	PR37 PR38	200K4/1/X 1K4/1	PM_GPIOR1	
			Bit 0	Bit 1
Bit 2	Bit 1	Bit 0	GPP Group 1	5 6 7
1	1	1	X4	
0	1	1	X2 ---	X2 ---
0	0	1	X2 ---	X1 X1
0	1	0	X1 X1	X2 ---
0	0	0	X1 X1 X1 X1	
Others: Reserved				

The diagram illustrates three parallel connections from the VCC3.3 rail to the PM GPIO pins. Each connection includes a resistor (either 200K/4/1 or 1K4/1X), a pull-up pin (PR41, PR42, PR50, PR51, PR48, PR49), and a ground connection (GND). The connections are labeled Bit 2, Bit 1, and Bit 0.



**Table 34. Type-C Status Function Table**

<b>STATUS_IND_0</b>	<b>STATUS_IND2_0</b>	<b>Function</b>
0	1	Device attached with host 3A output capable
1	0	Device attached with host 1.5A output capable
1	1	Device attached with host 900mA output capable
0	0	Device detached
<b>CC_IND_0</b>		<b>Function</b>
0		Configuration channel on CC1
1		Configuration channel on CC2

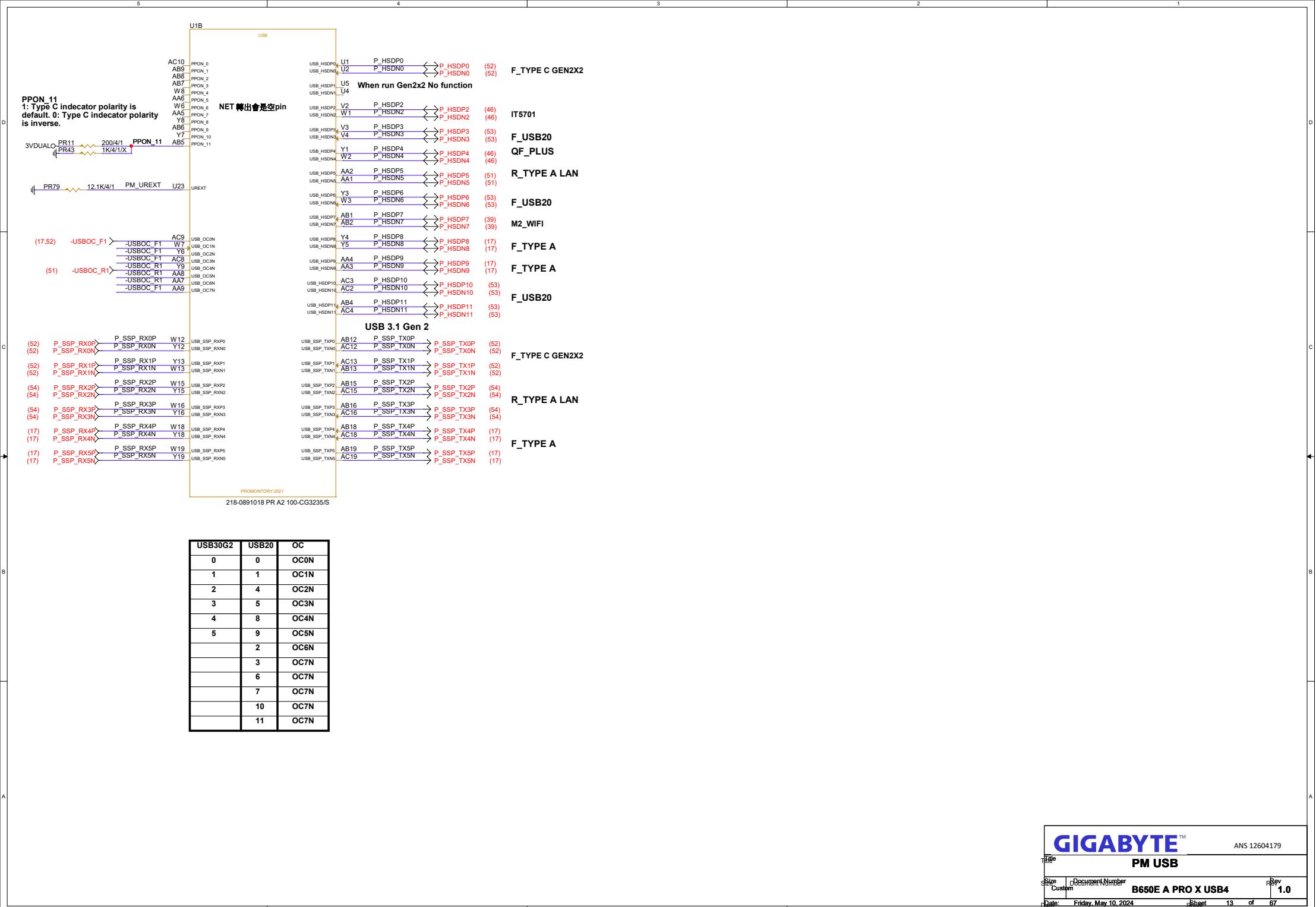


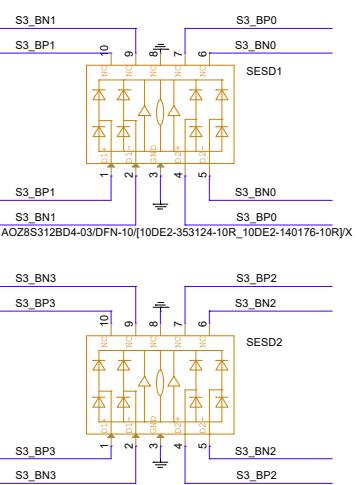
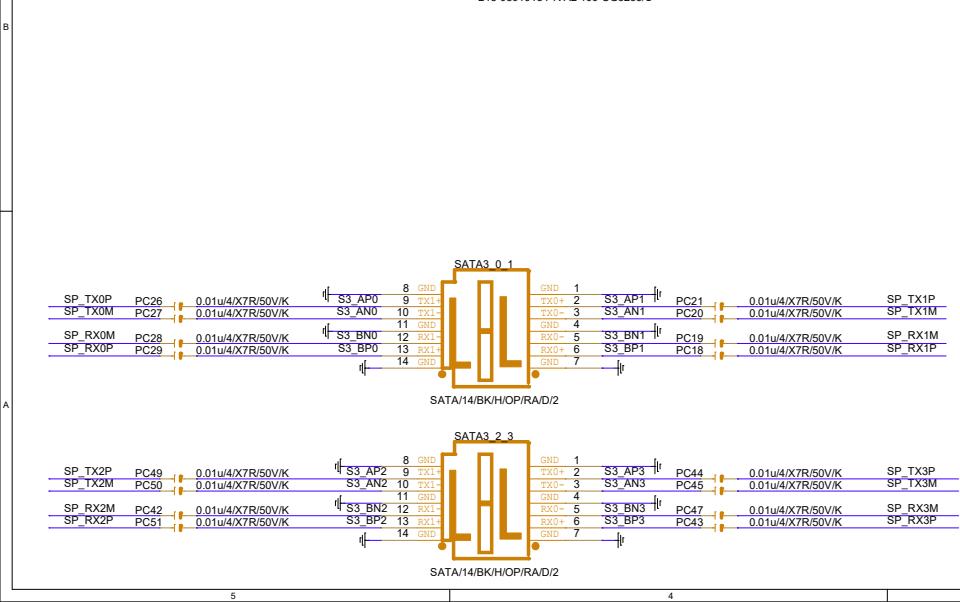
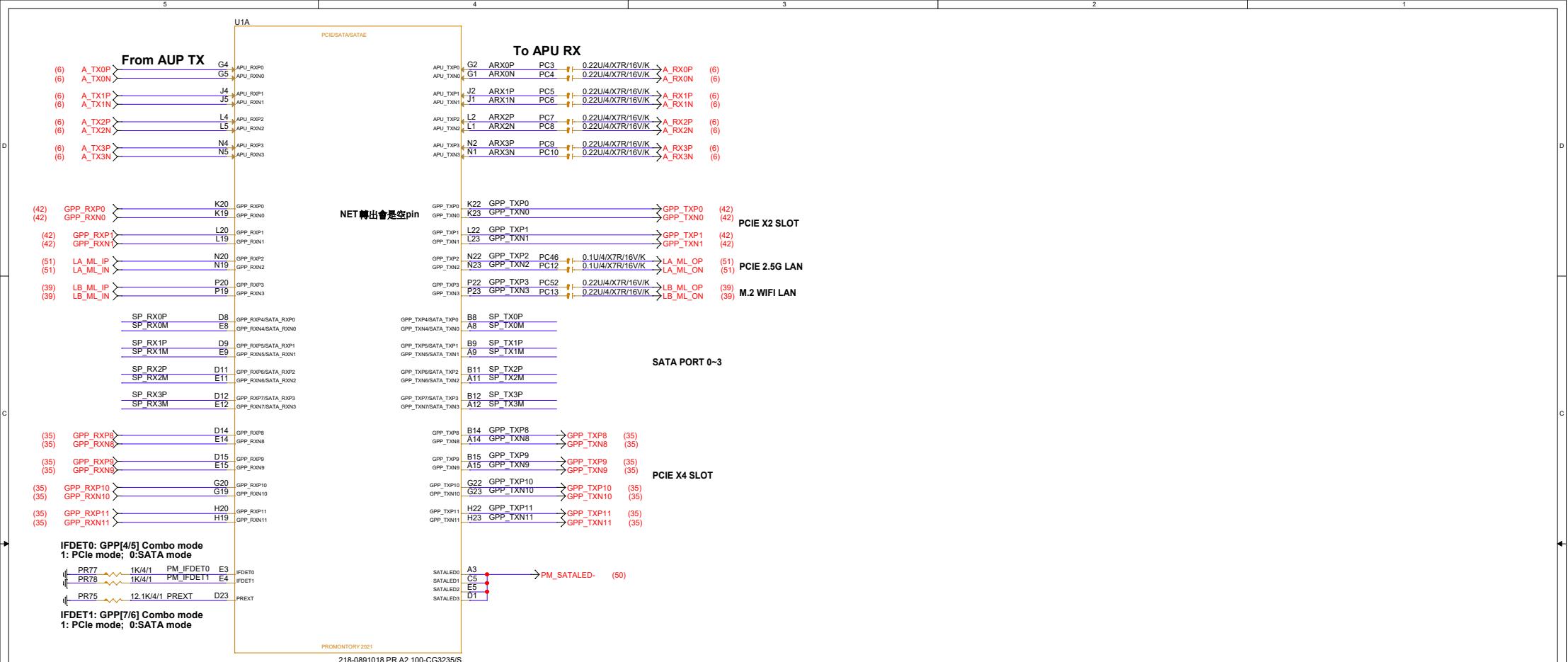
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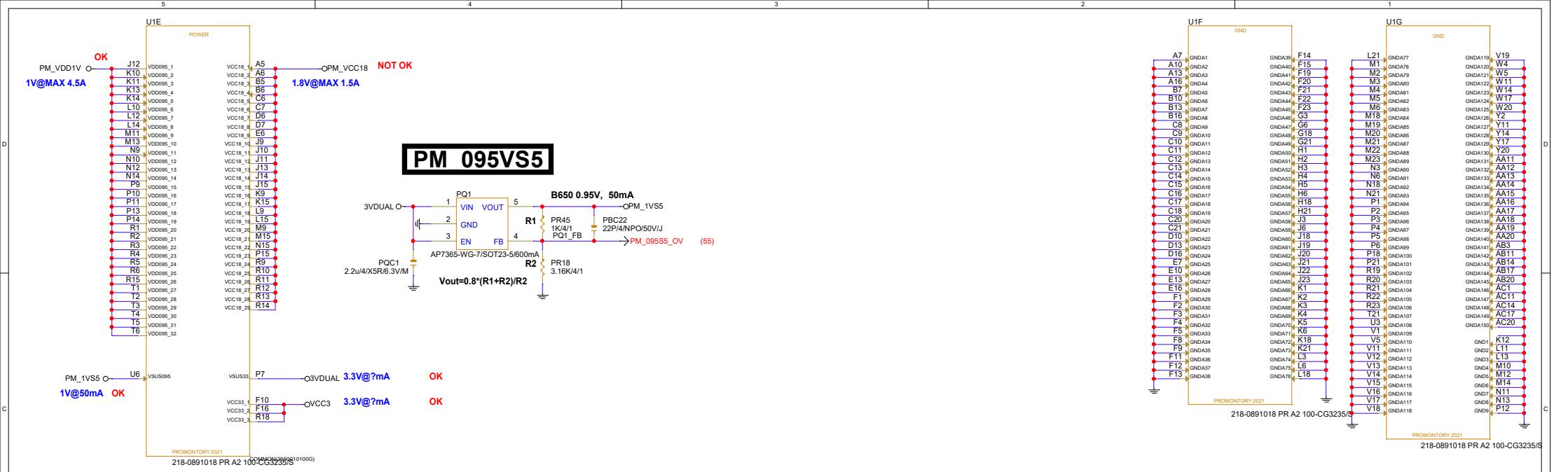
ANS 12604179

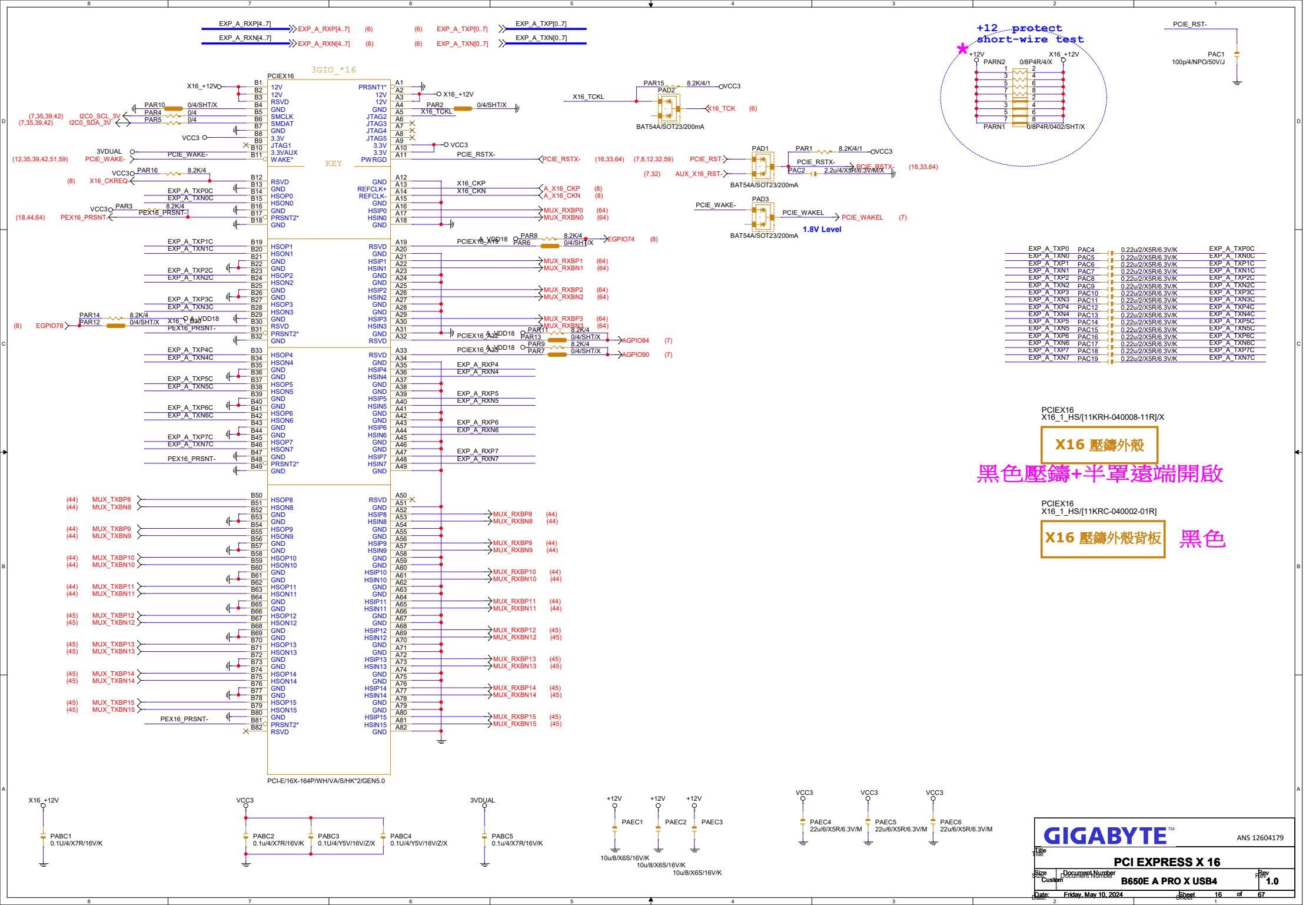
## **PM CLK/SPI/MISC**

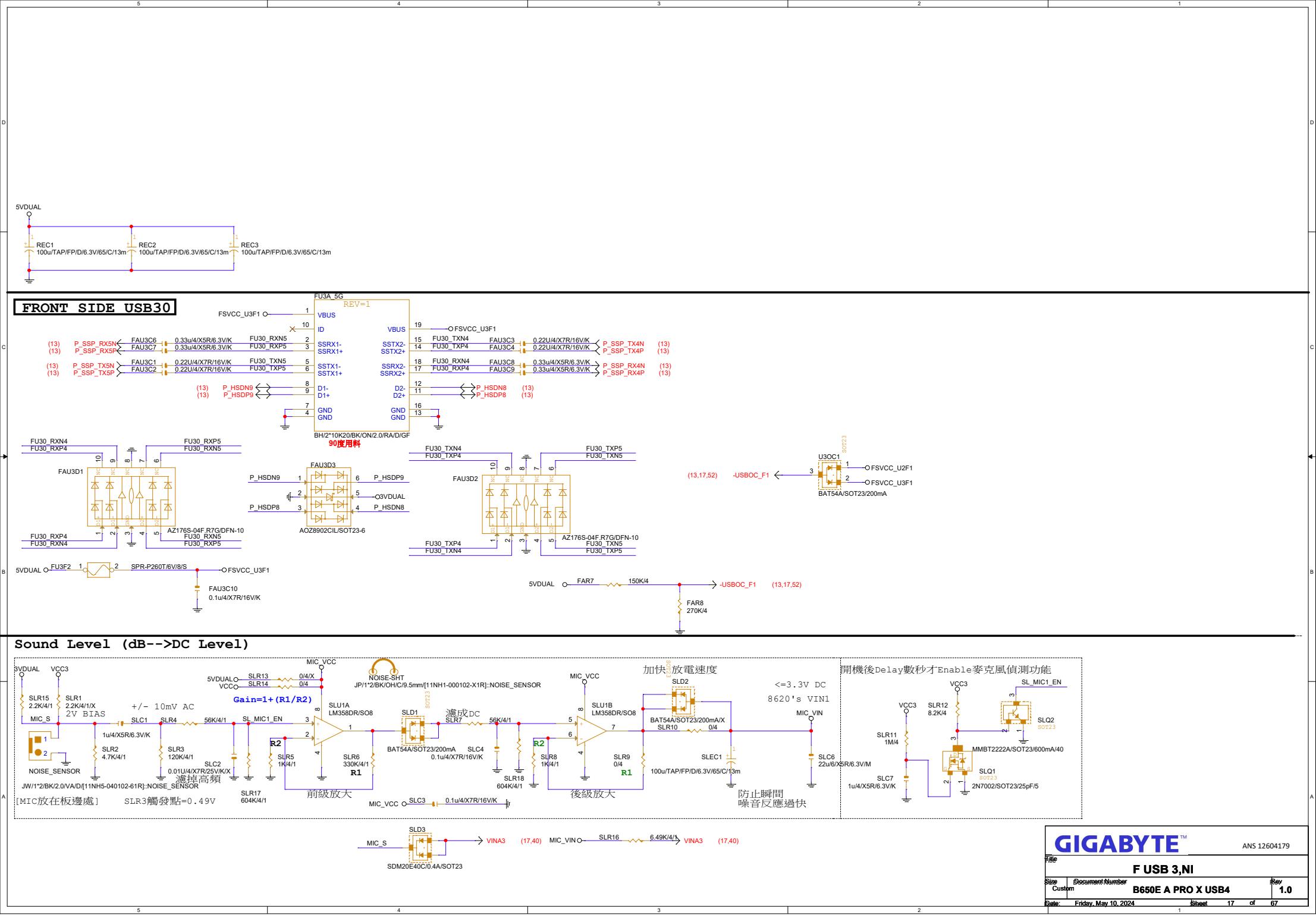
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ANS 12604179

F USB 3.NI

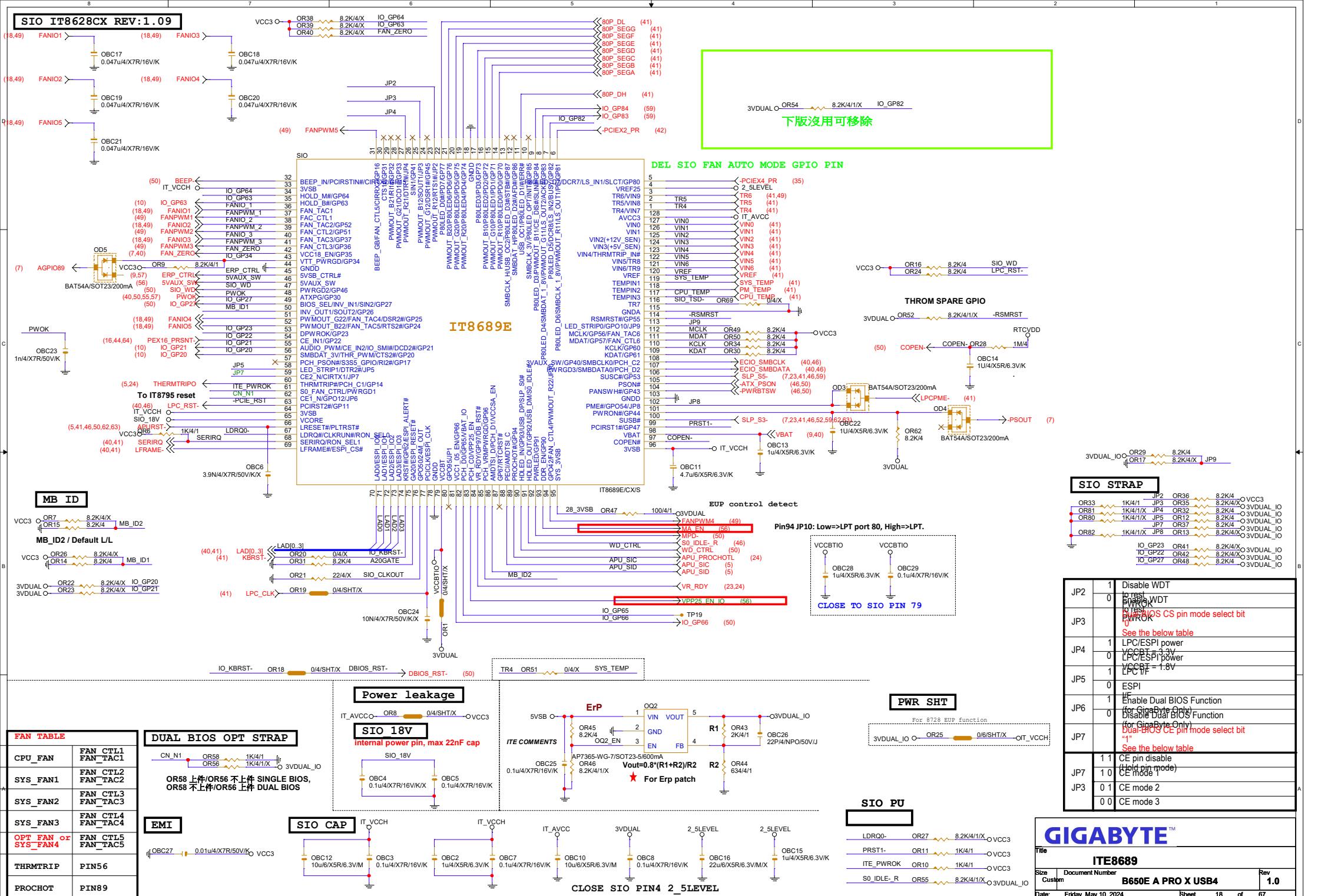
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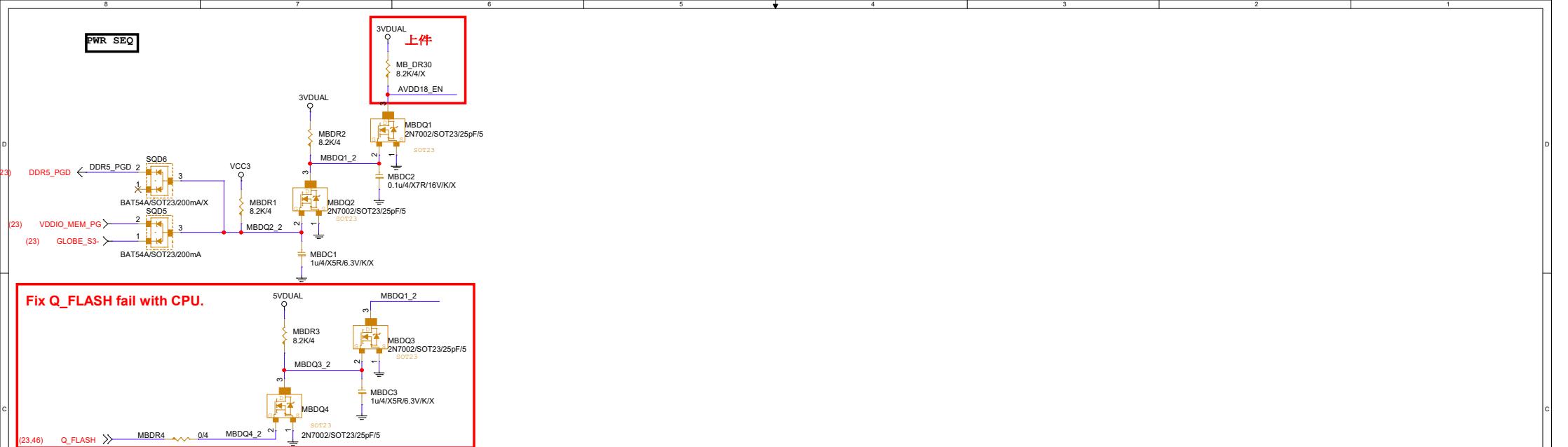
B650E A PRO X USB4

Rev 1.0

Date: Friday, May 10, 2024

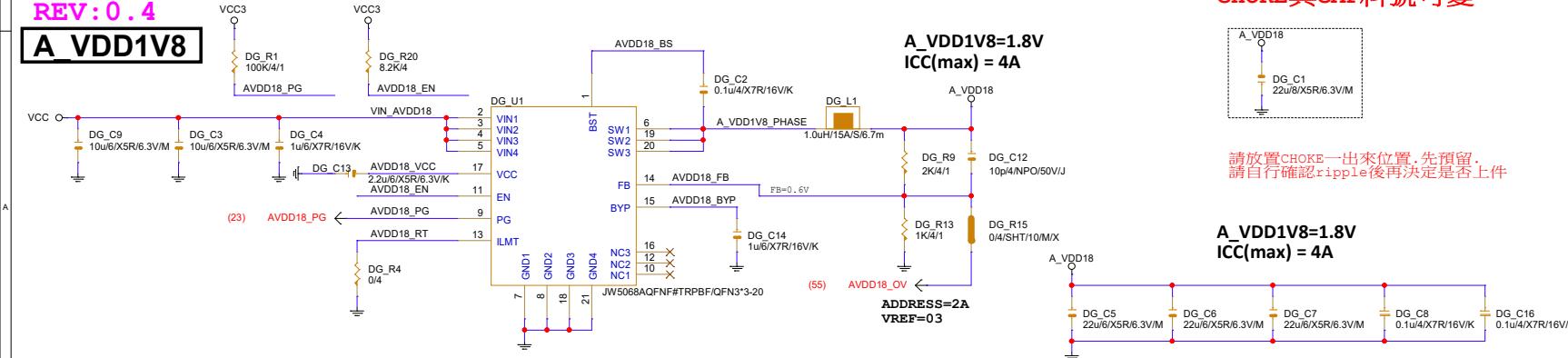
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REV: 0.4

A\_VDD1V8



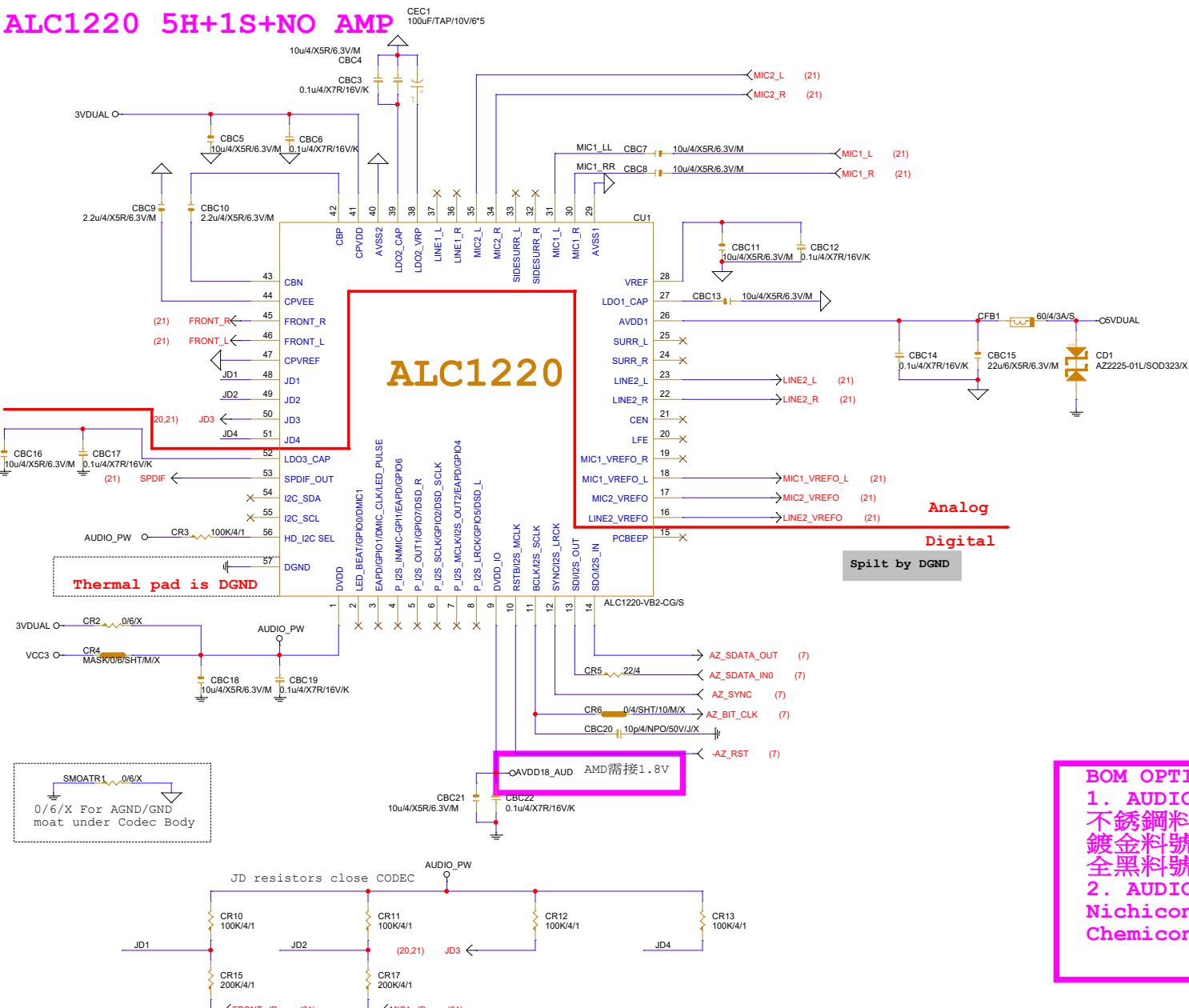
A\_VDD18

請放置CHOKE一出來位置.先預留.  
請自行確認ripple後再決定是否上件

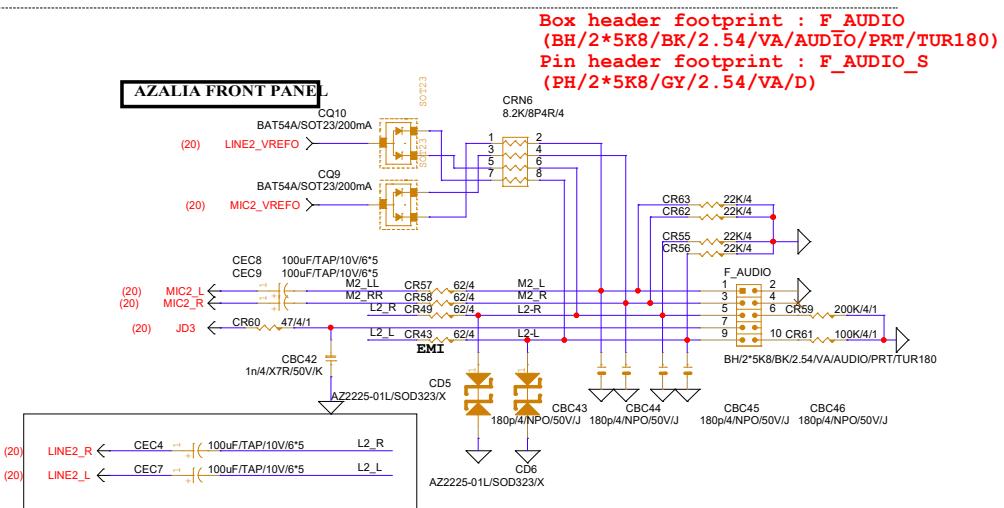
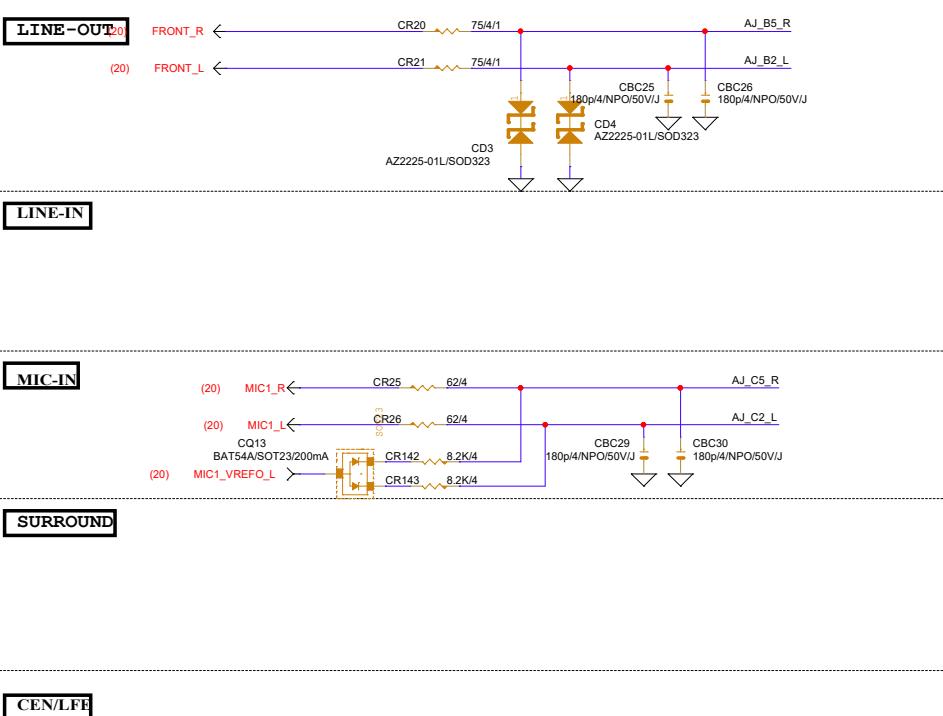
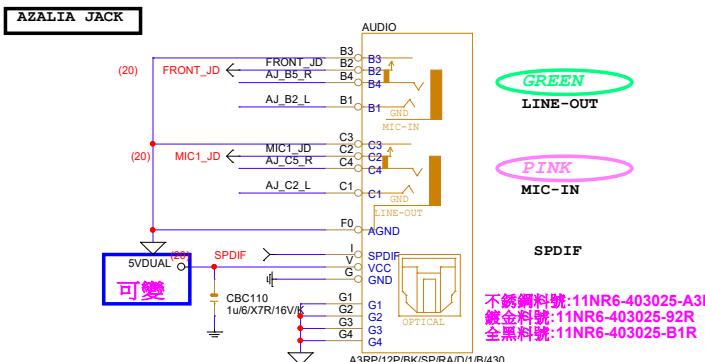
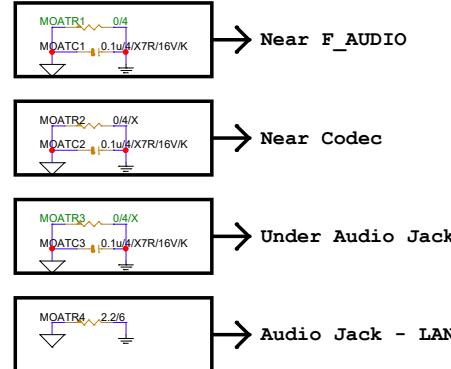
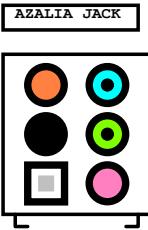
A\_VDD1V8=1.8V  
ICC(max) = 4A



## ALC1220 5H+1S+NO AMP



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AUDIO JACK

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B650E A PR

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D

D

c

c

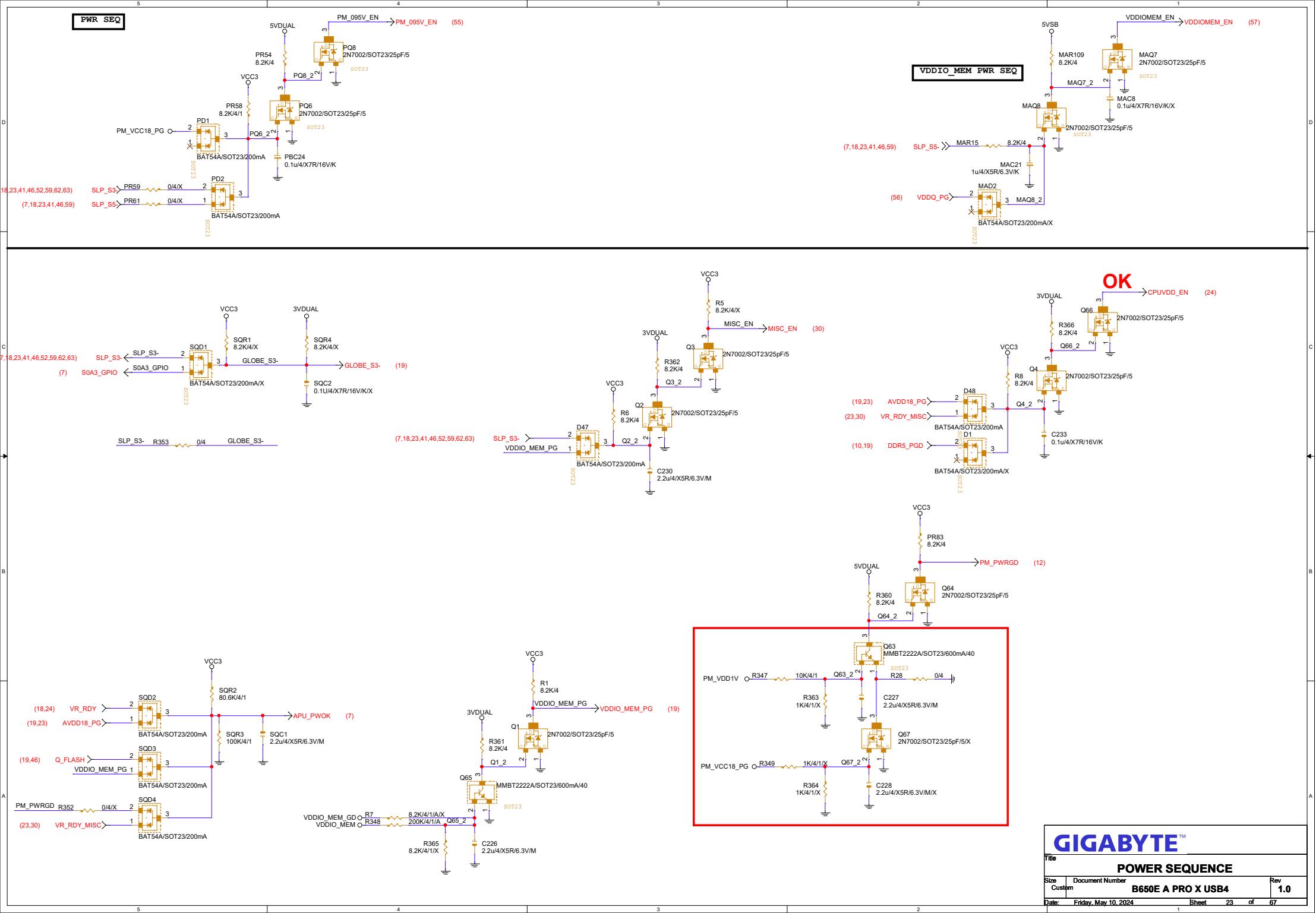
B

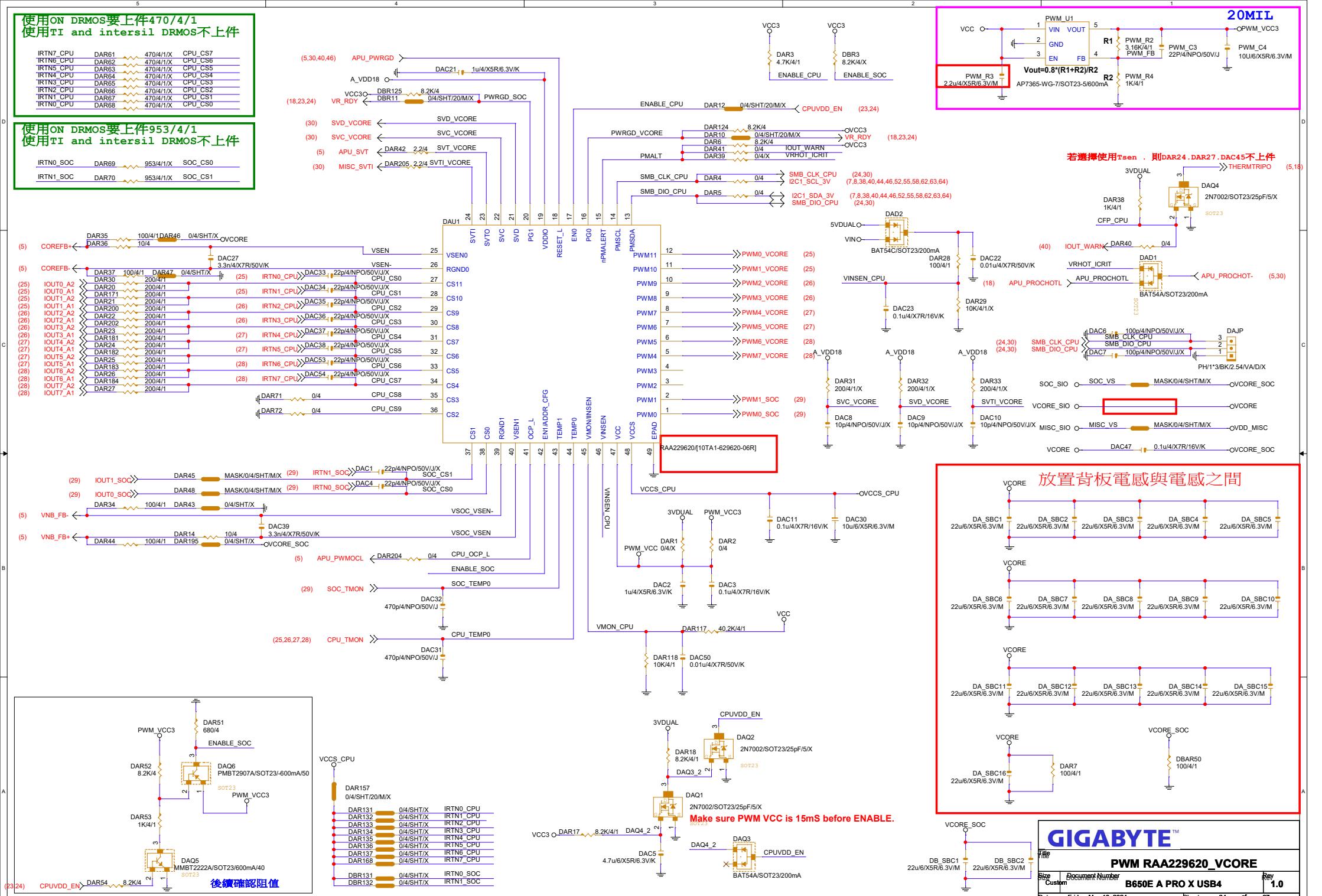
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A

A

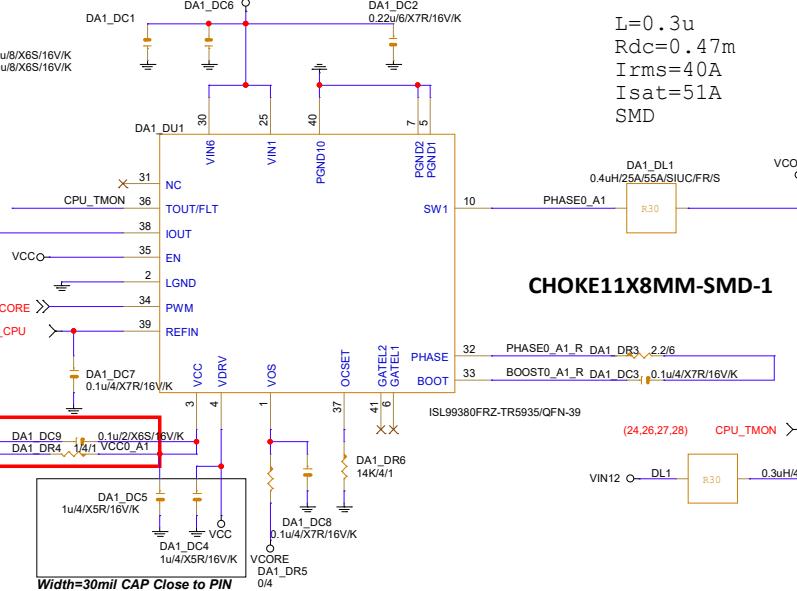
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<b>Size</b>	<b>Document Number</b>
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	<b>Rev</b>
	1.0
<b>Date:</b>	Friday, May 10, 2024
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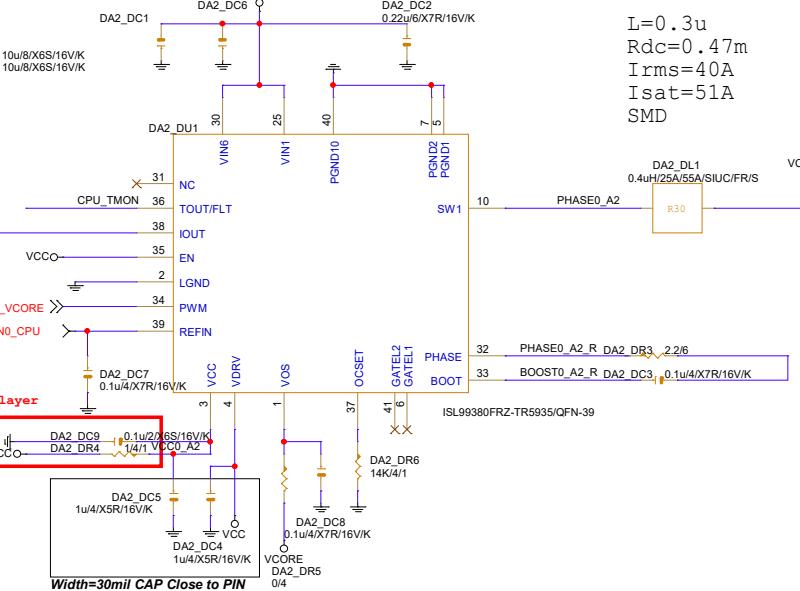


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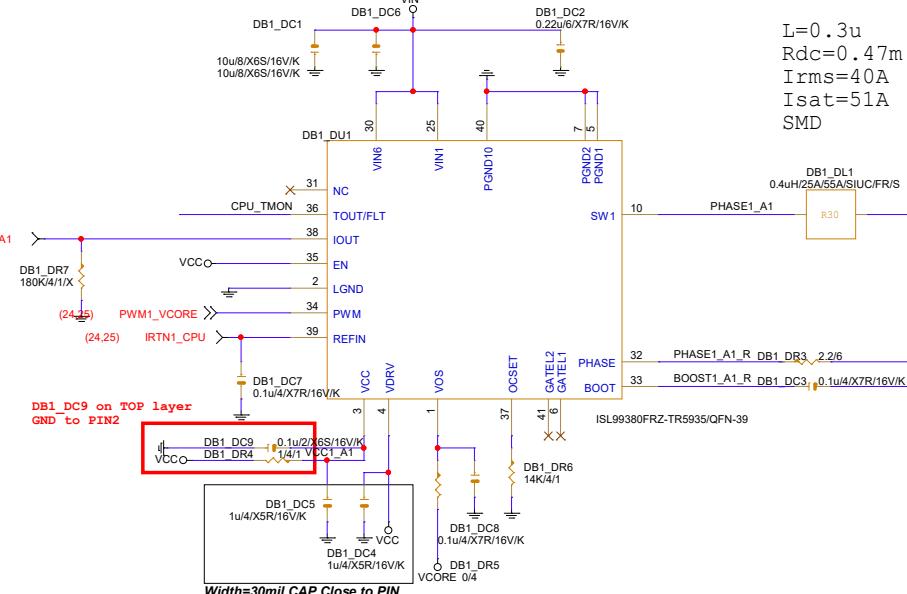
## VCORE PHASE1\_1



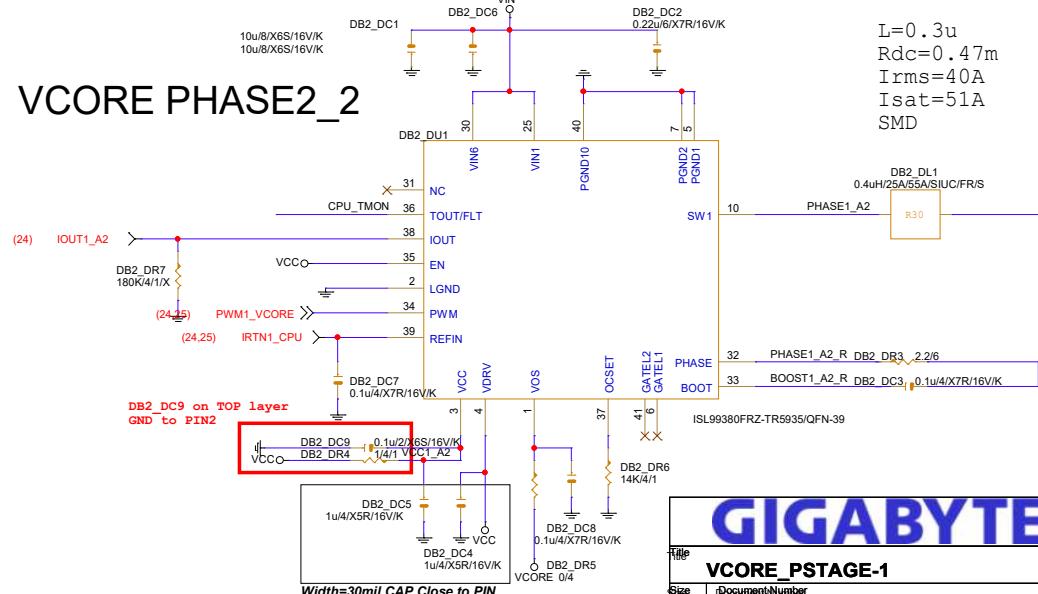
## VCORE PHASE1\_2



## VCORE PHASE2\_1

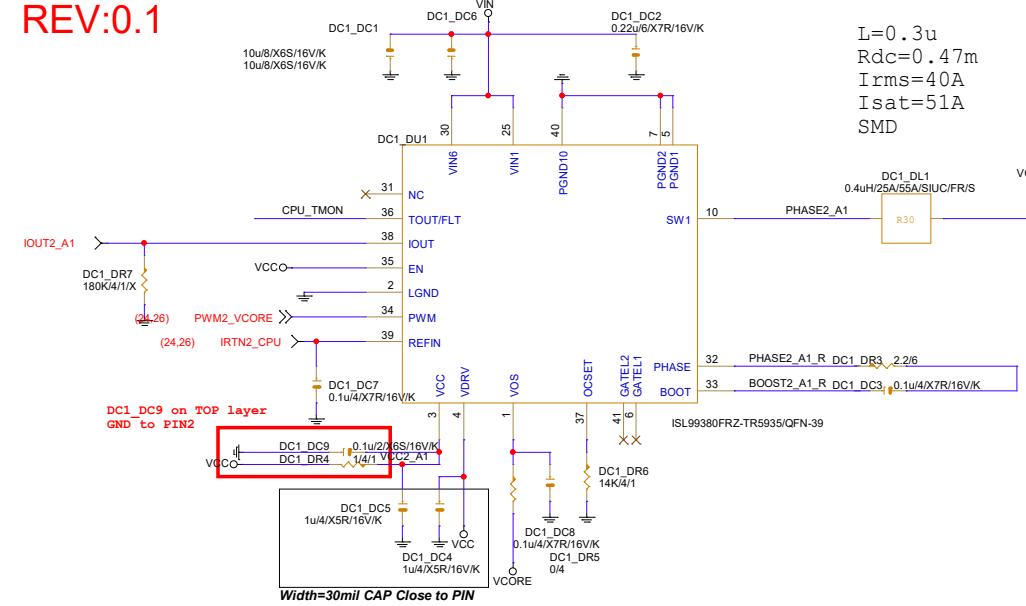


## VCORE PHASE2\_2



## VCORE PHASE3\_1

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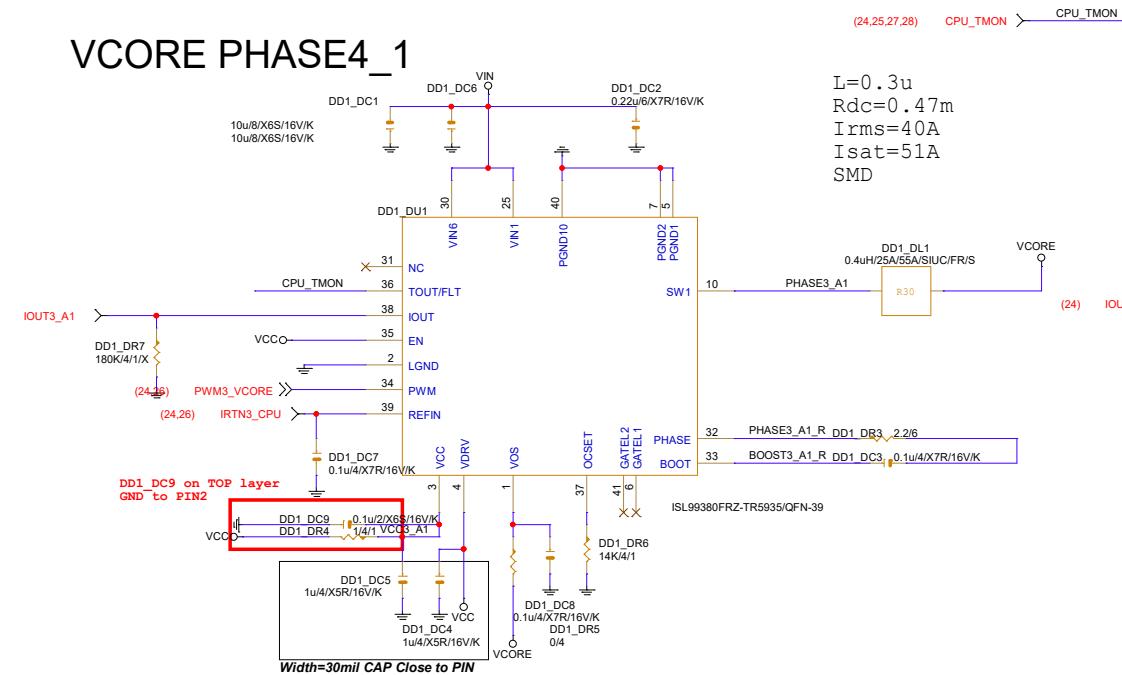


L=0.3u  
Rdc=0.47m  
Irms=40A  
Isat=51A  
SMD



L=0.3u  
Rdc=0.47m  
Irms=40A  
Isat=51A  
SMD

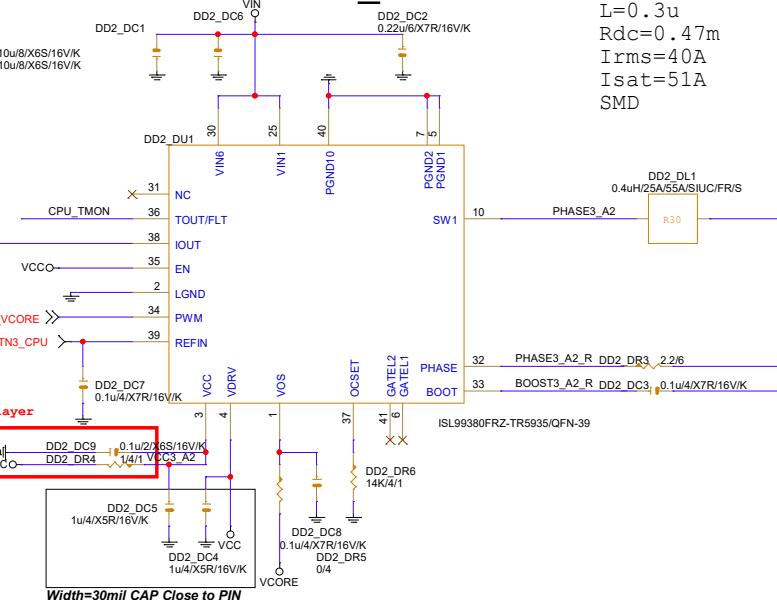
VCORE PHASE4\_1



L=0.3u  
Rdc=0.47m  
Irms=40A  
Isat=51A  
SMD



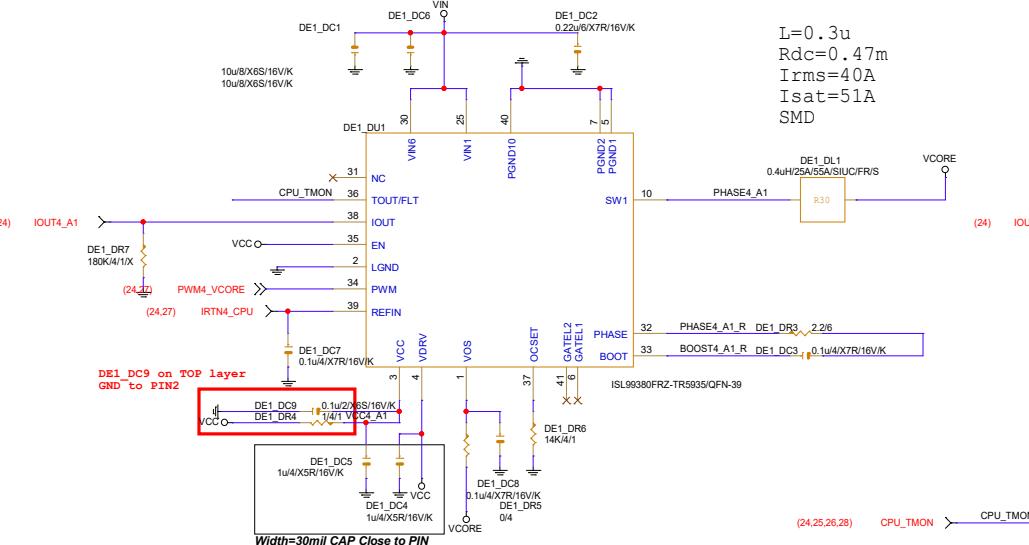
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Rdc=0.47m  
Irms=40A  
Isat=51A  
SMD



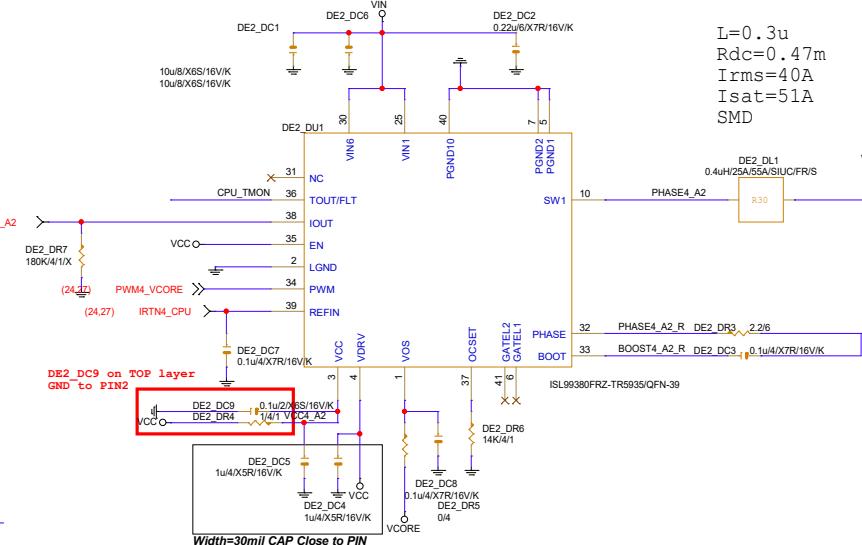
*Width=30 mil CAP Close to PIN*

REV:0.1

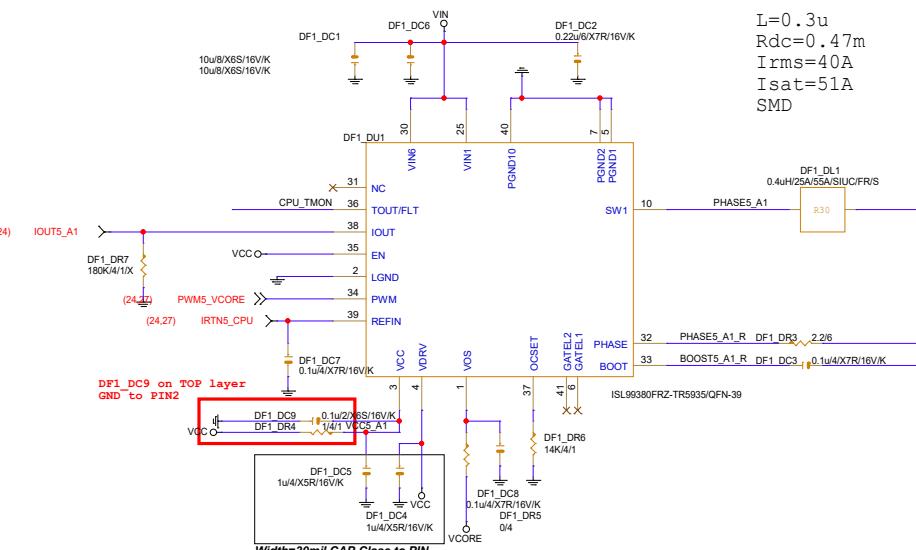
## VCORE PHASE 5\_1



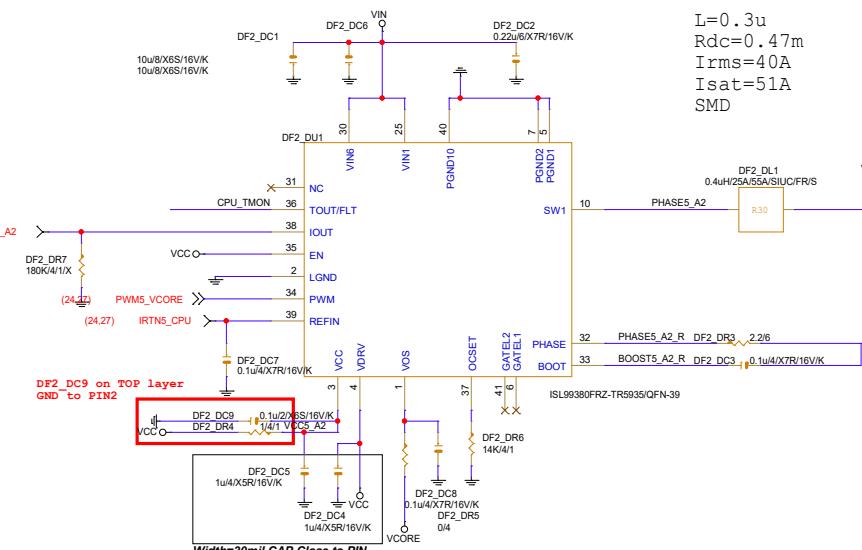
## VCORE PHASE 5\_2



## VCORE PHASE 6\_1

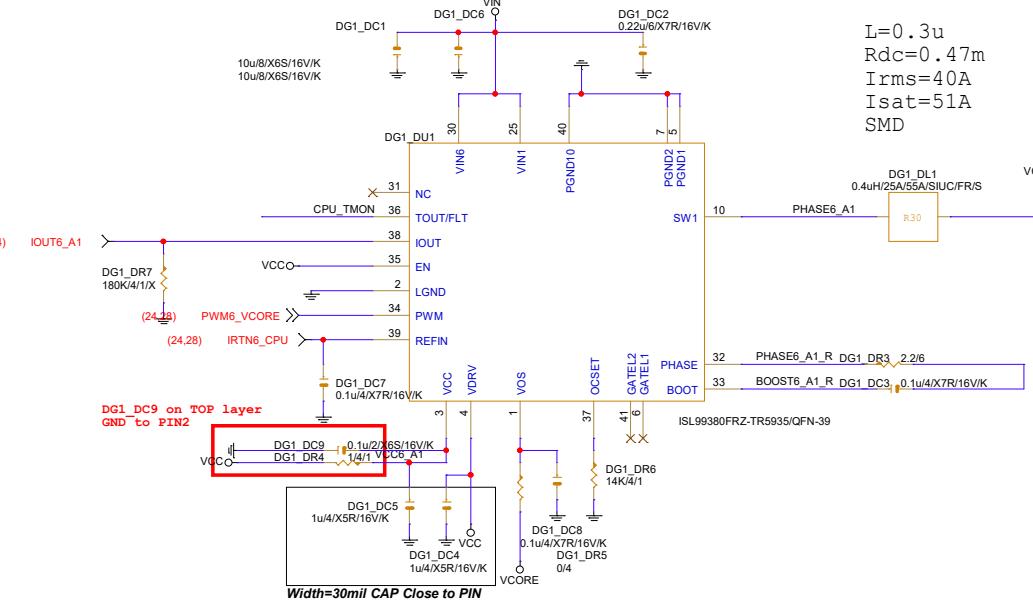


## VCORE PHASE 6\_2



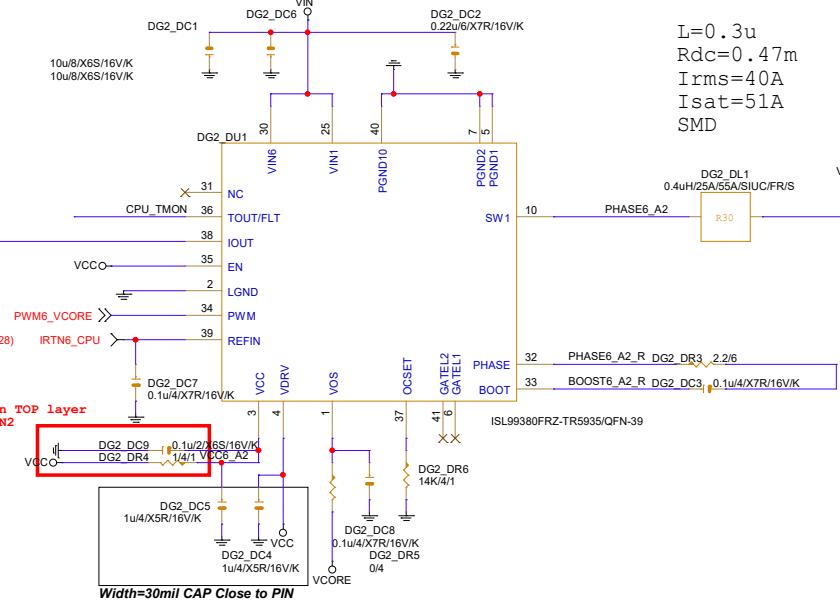
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# VCORE PHASE 7\_1



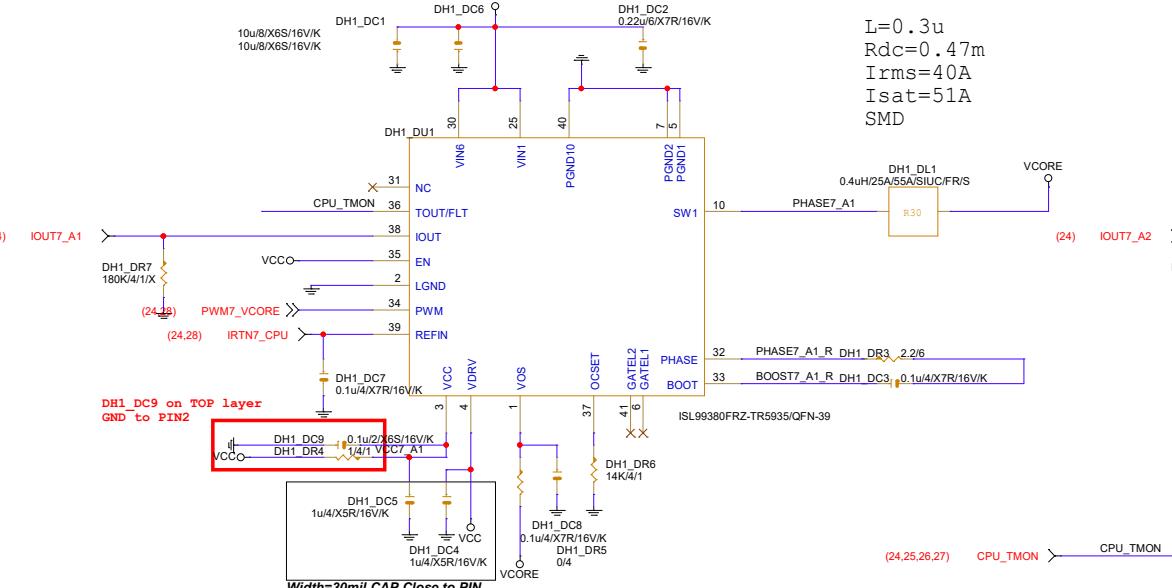
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 $Rdc=0.47m$   
 $Irms=40A$   
 $Isat=51A$   
SMD

# VCORE PHASE 7\_2



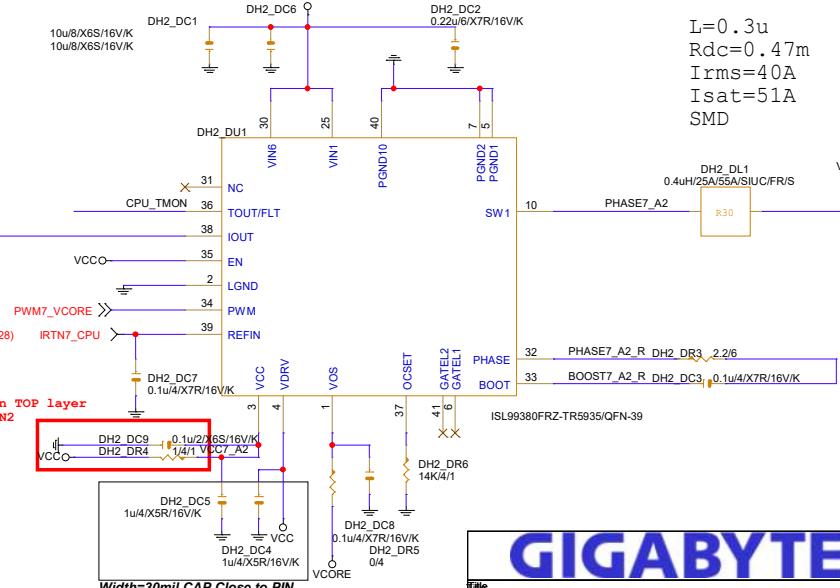
$L=0.3\mu$   
 $Rdc=0.47m$   
 $Irms=40A$   
 $Isat=51A$   
SMD

# VCORE PHASE 8\_1



$L=0.3\mu$   
 $Rdc=0.47m$   
 $Irms=40A$   
 $Isat=51A$   
SMD

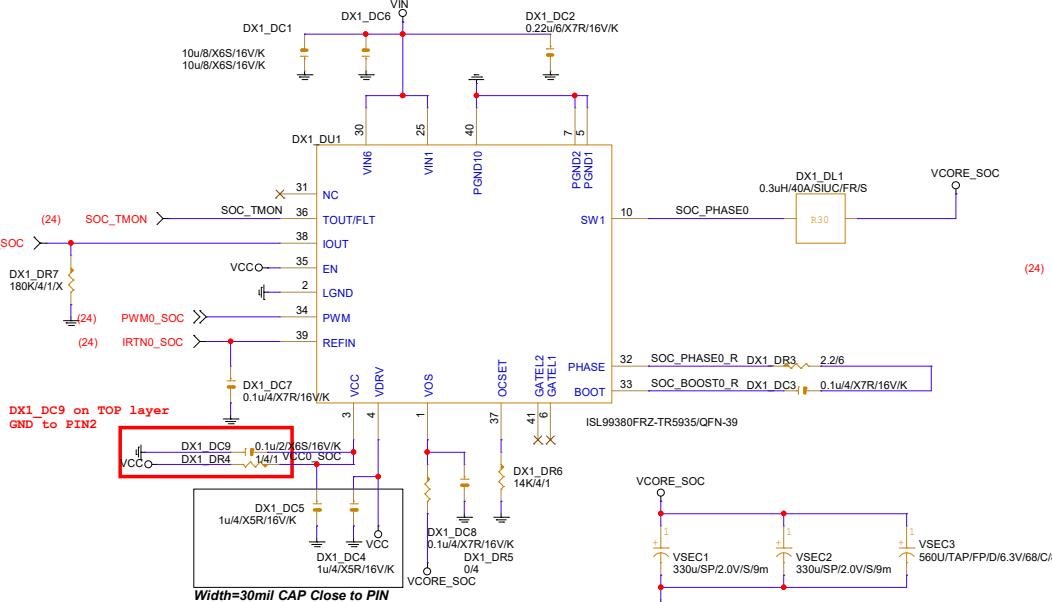
# VCORE PHASE 8\_2



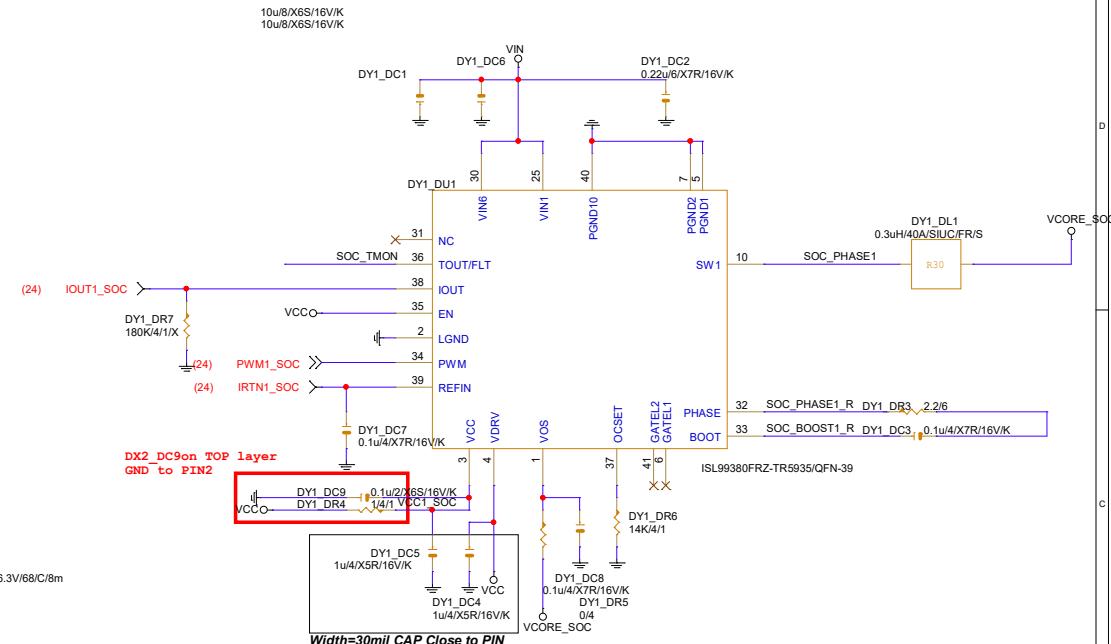
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 $Irms=40A$   
 $Isat=51A$   
SMD

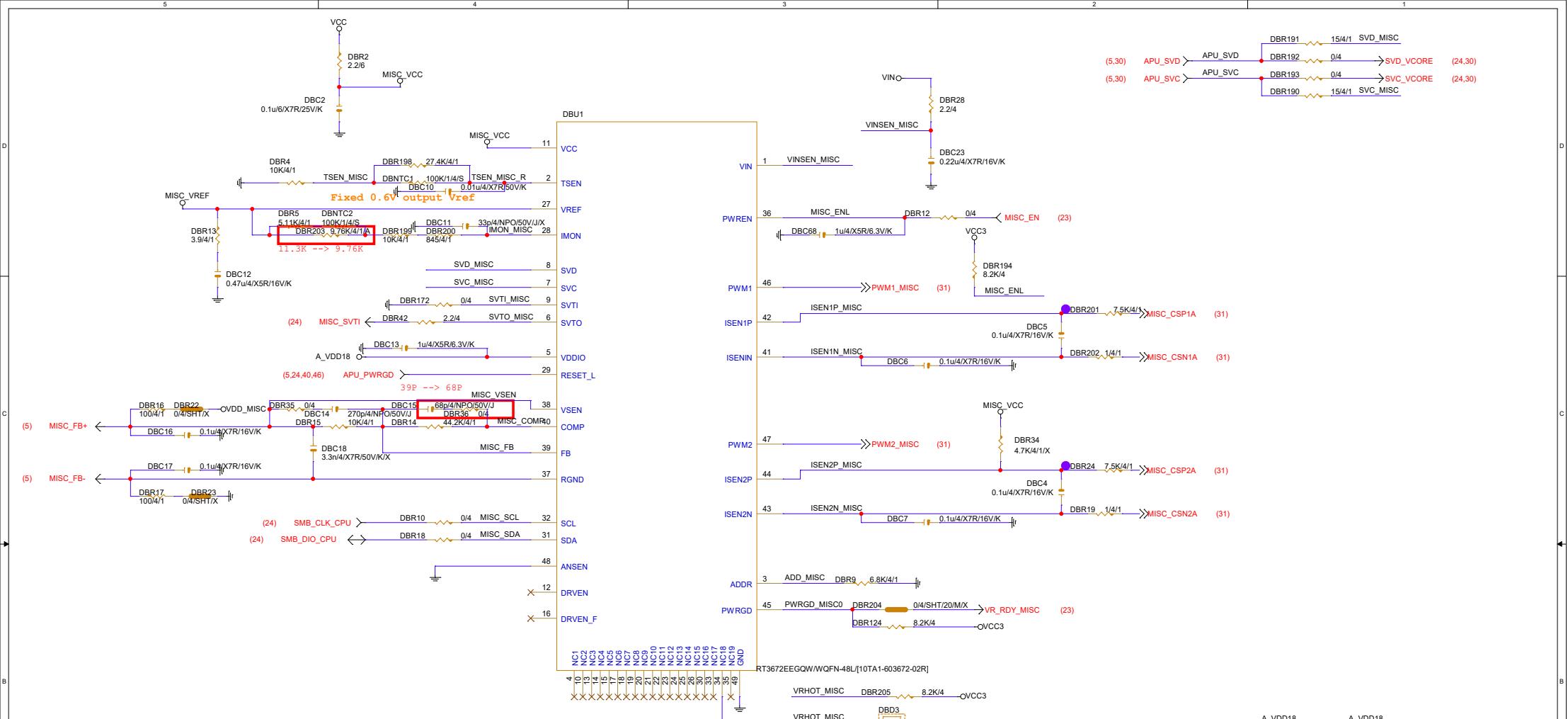
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## VCORE\_SOC PHASE1



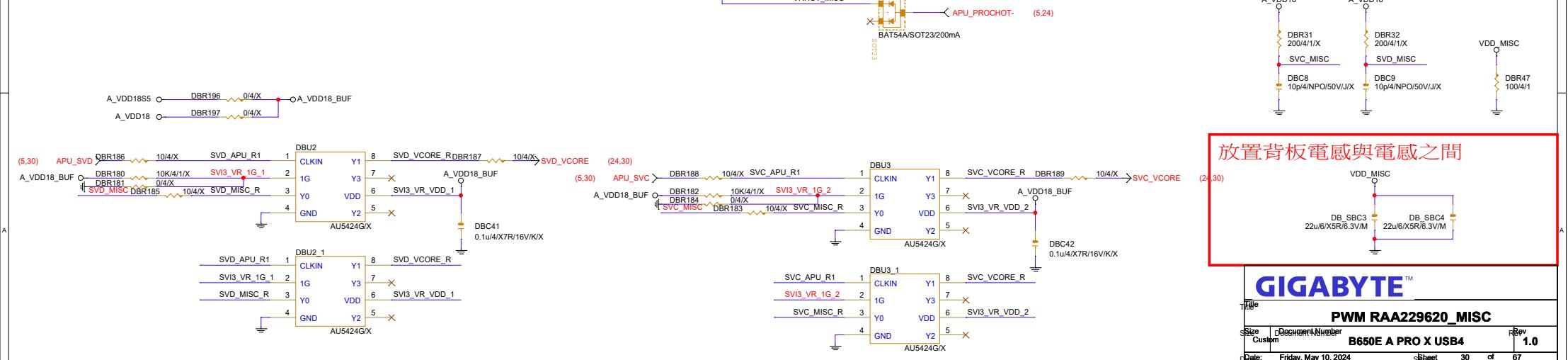
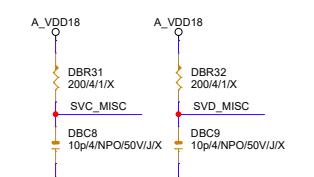
## VCORE\_SOC PHASE2



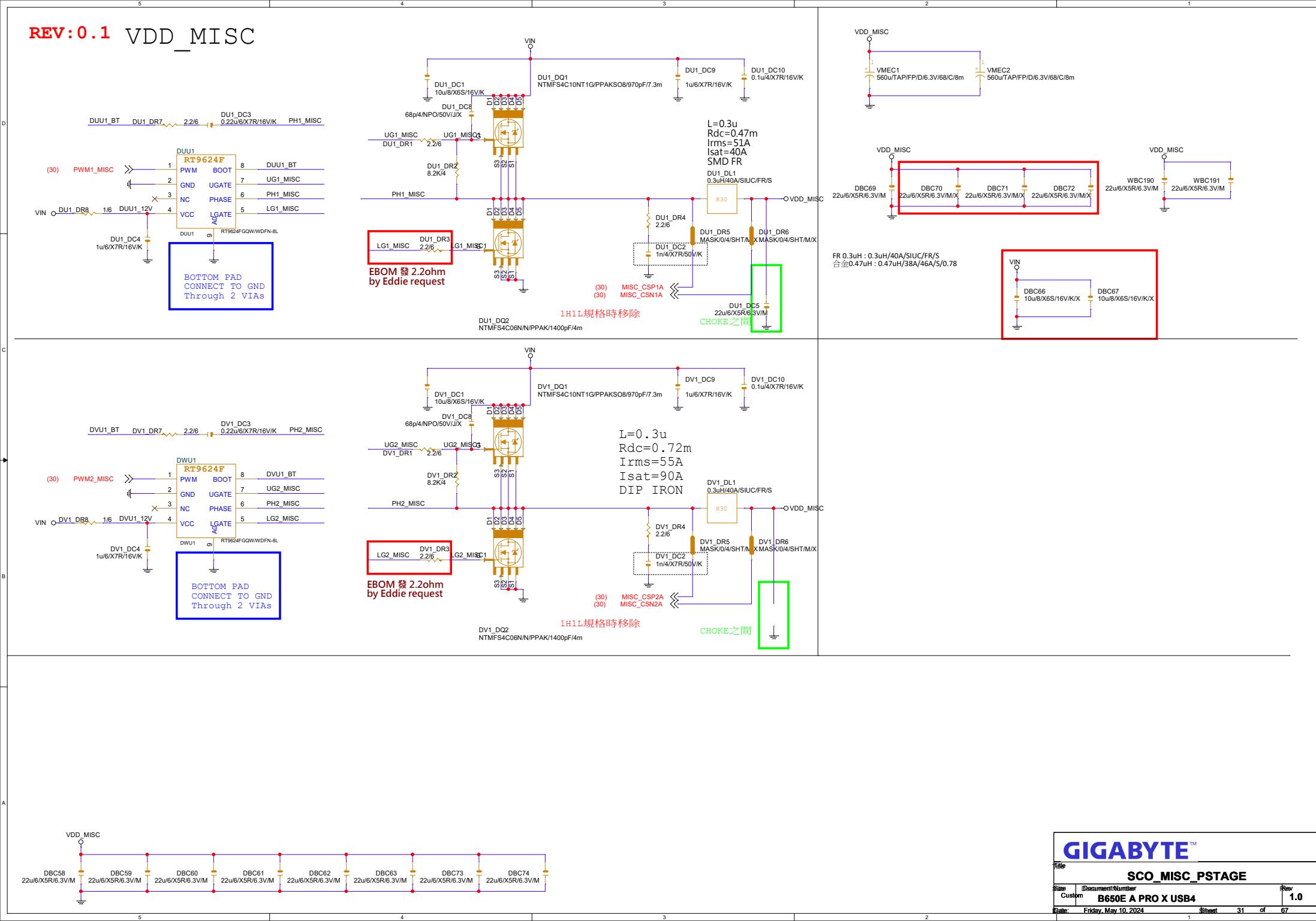


放置背板電感與電感之間

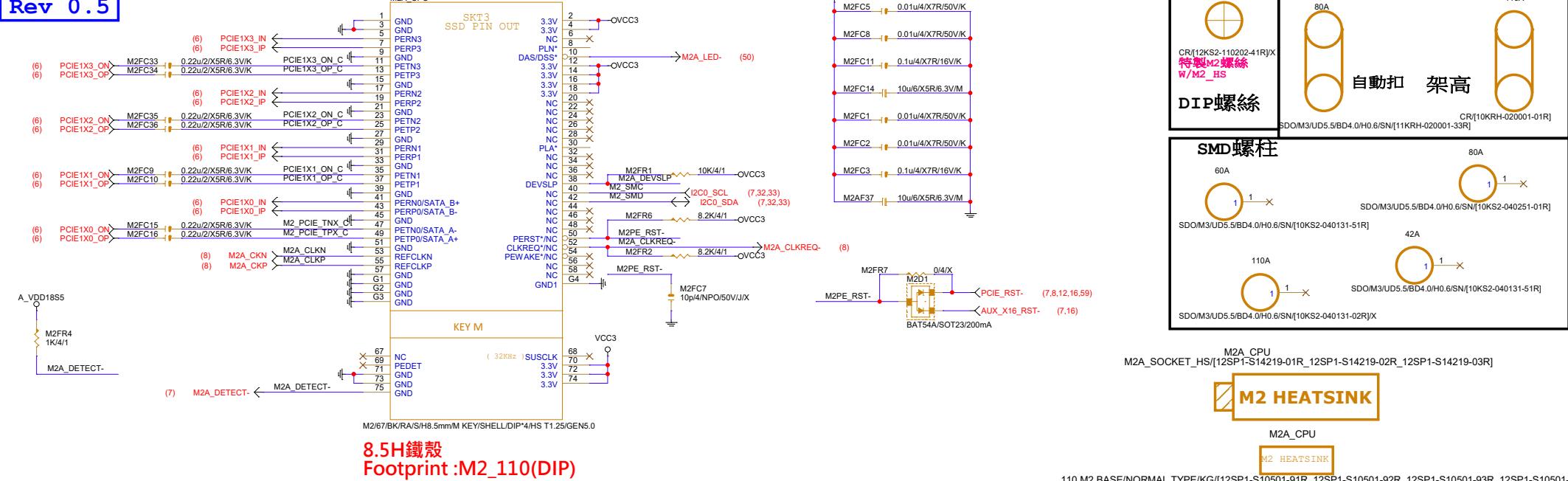
**GIGABYTE™**  
Part Number: B650E A PRO X USB4  
Size: Custom  
Revision: 1.0  
Date: Friday, May 10, 2024  
Sheet 30 of 67



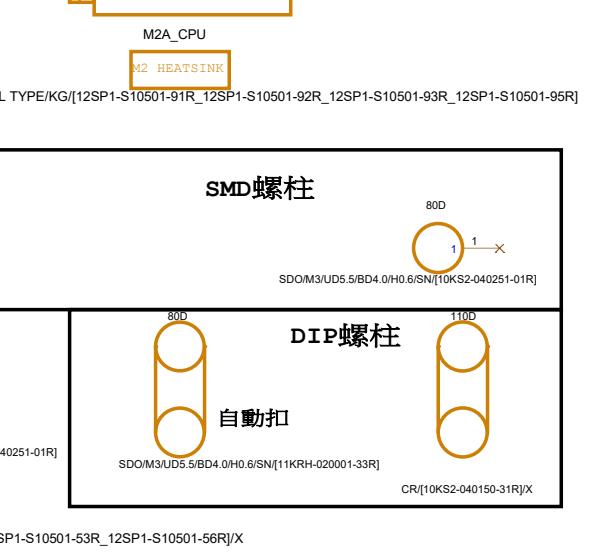
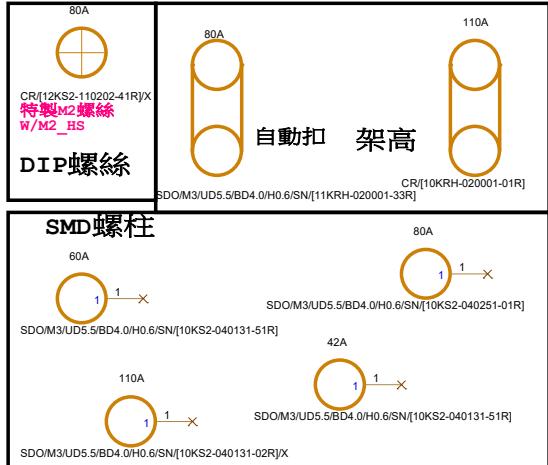
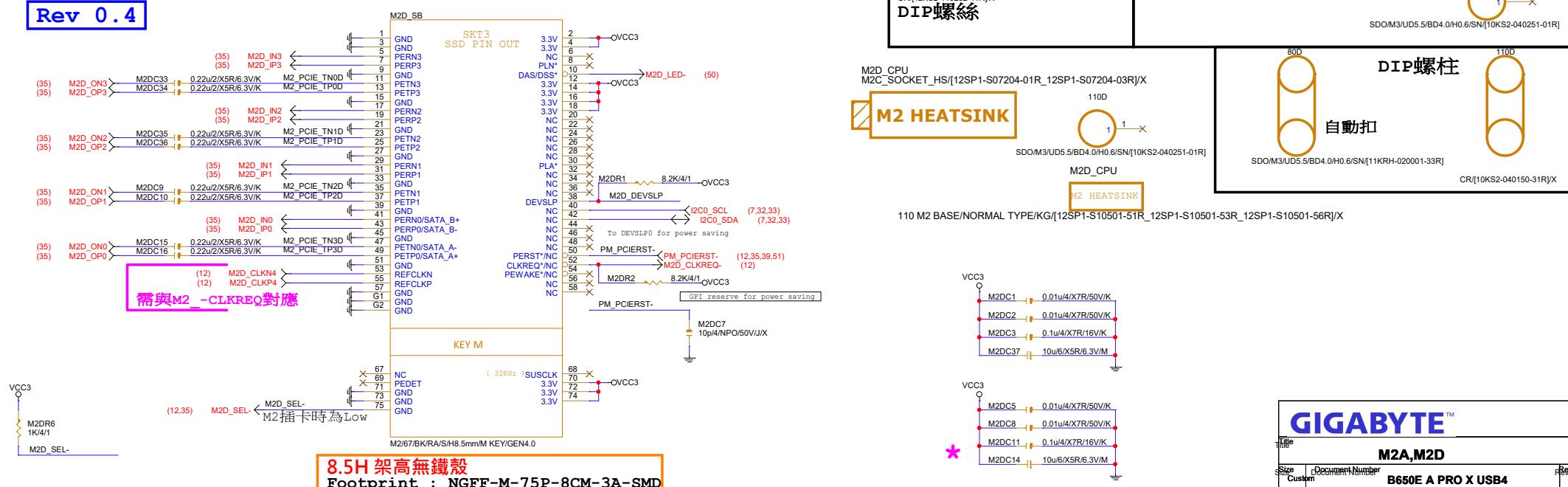
# REV: 0.1 VDD\_MISC

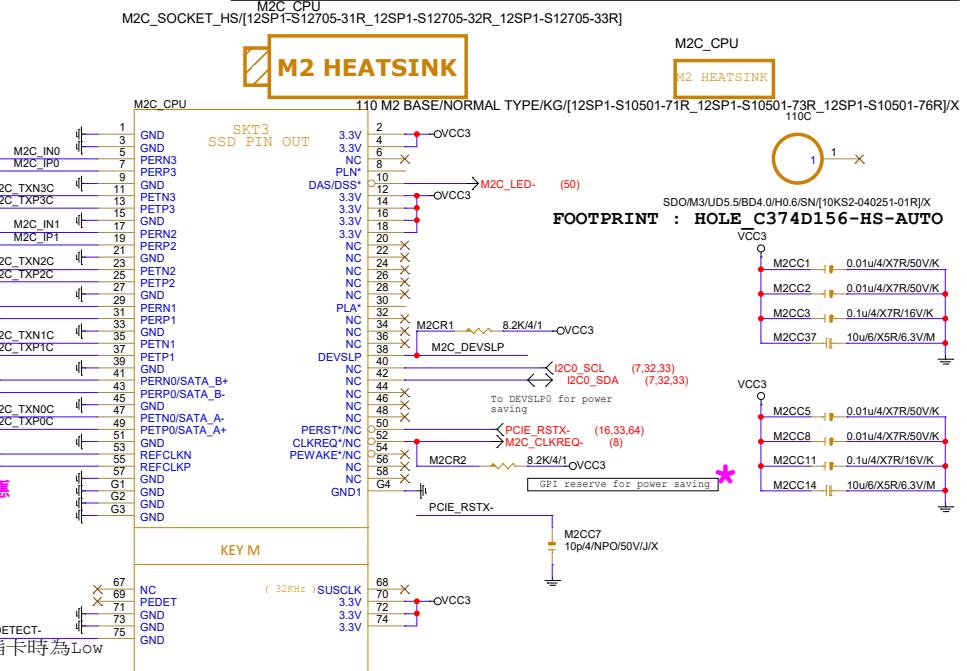
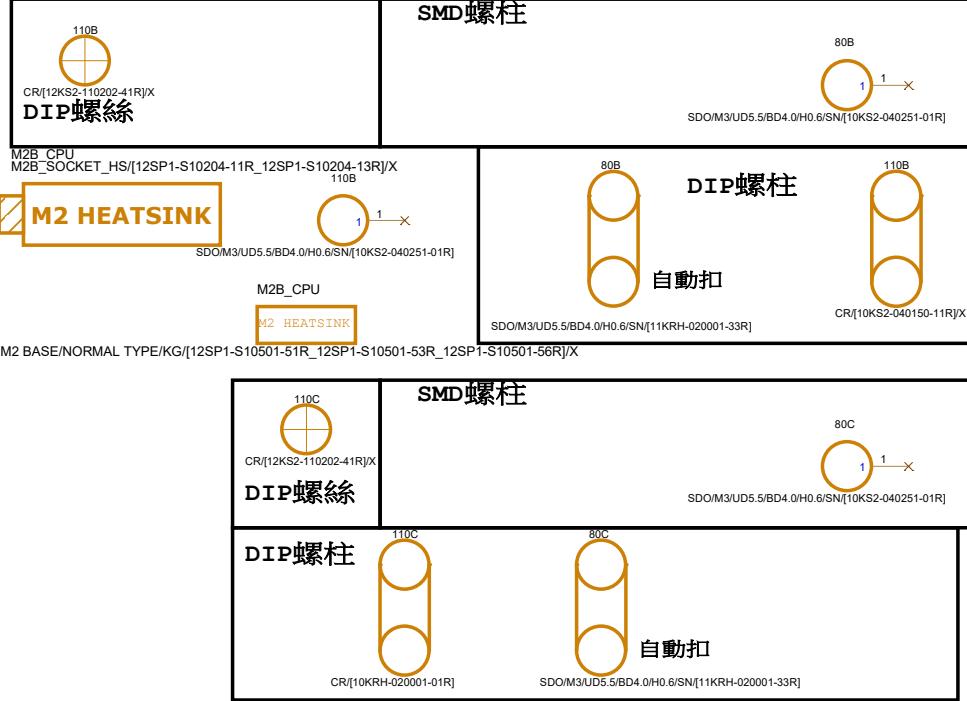
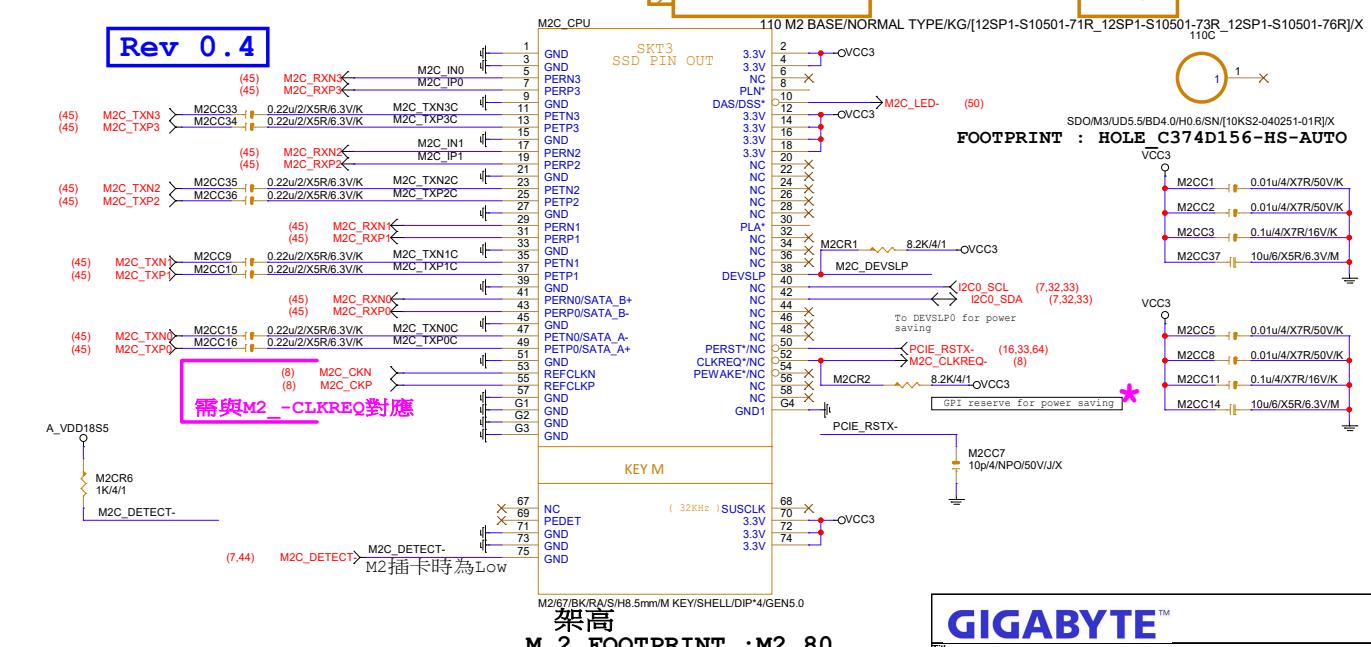
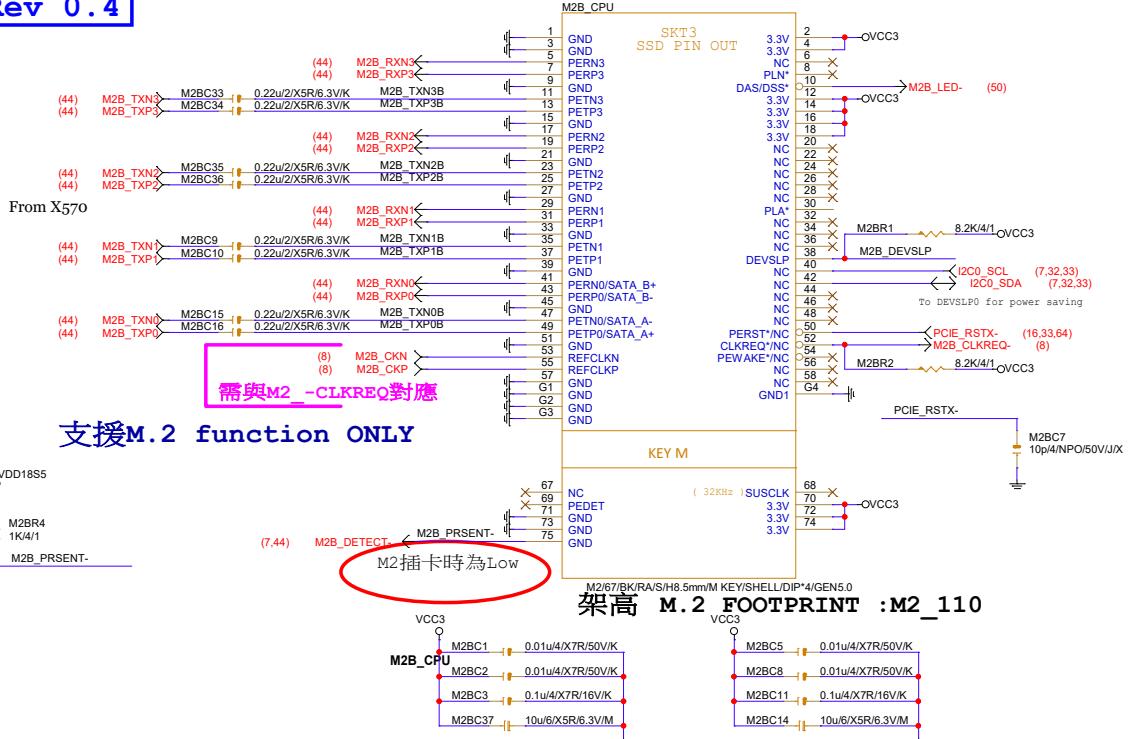


Rev 0.5

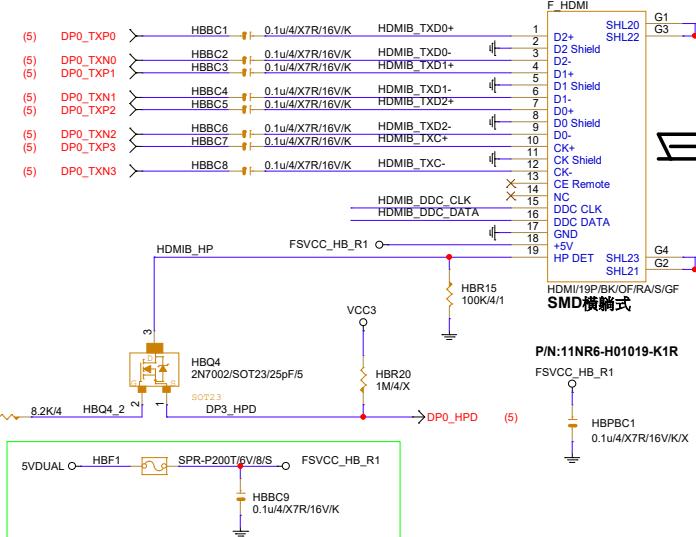
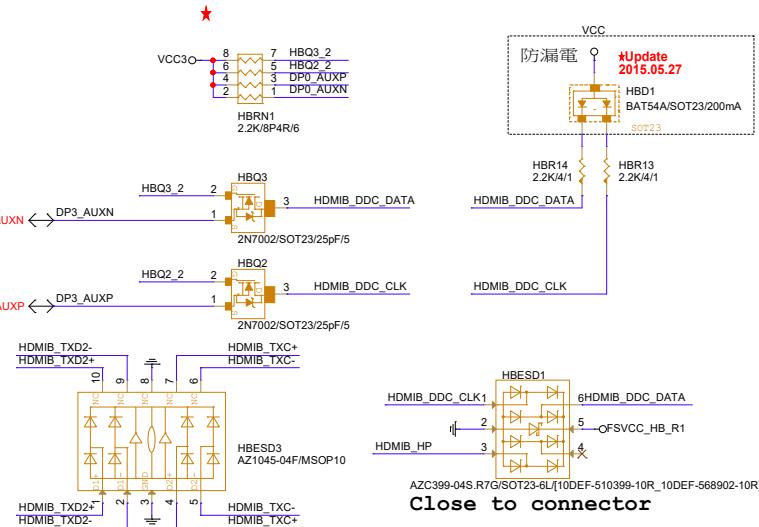
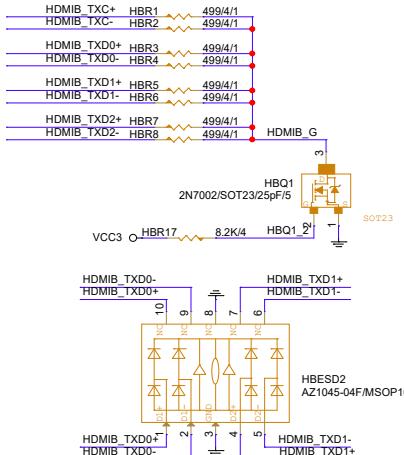


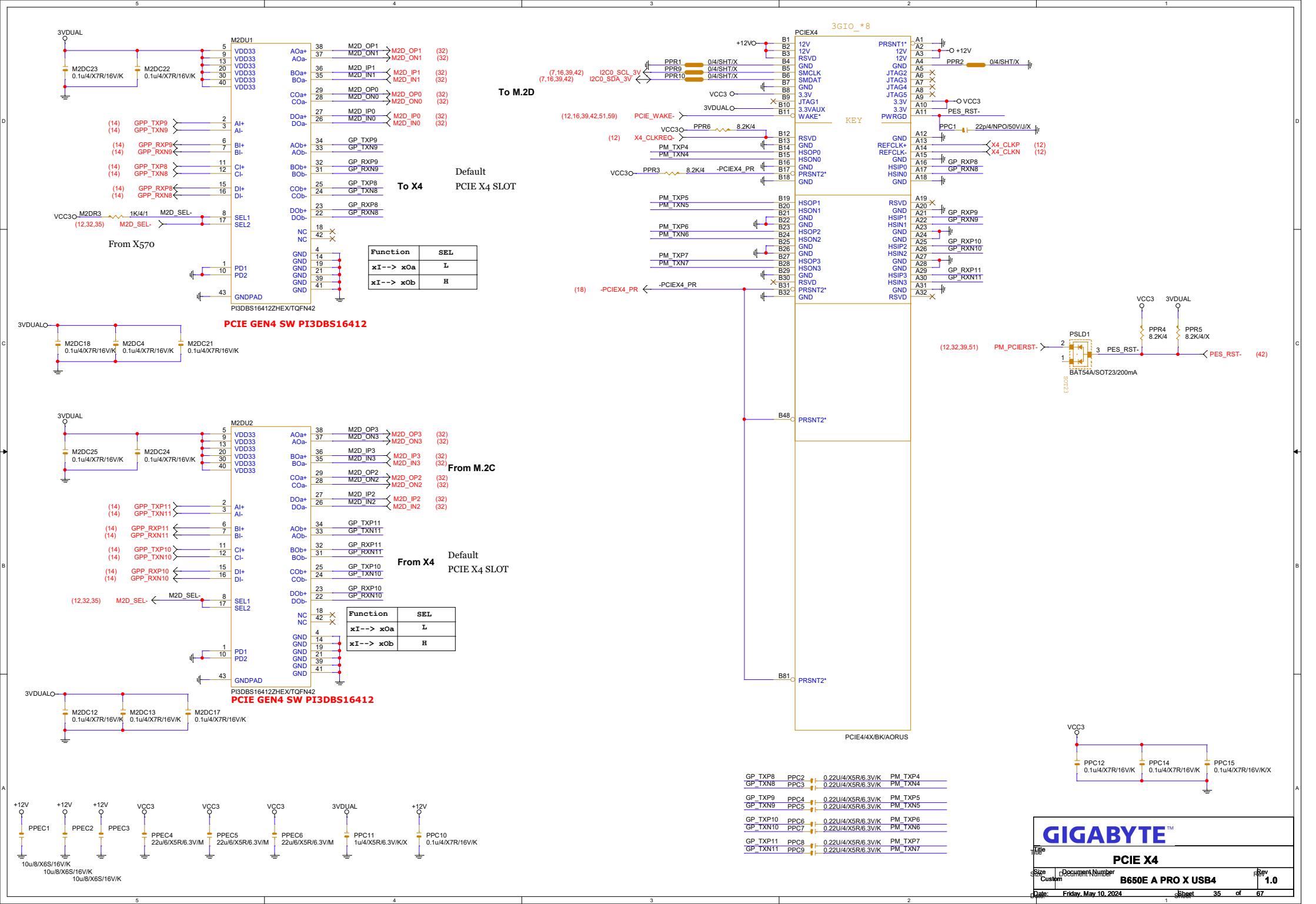
Rev 0.4

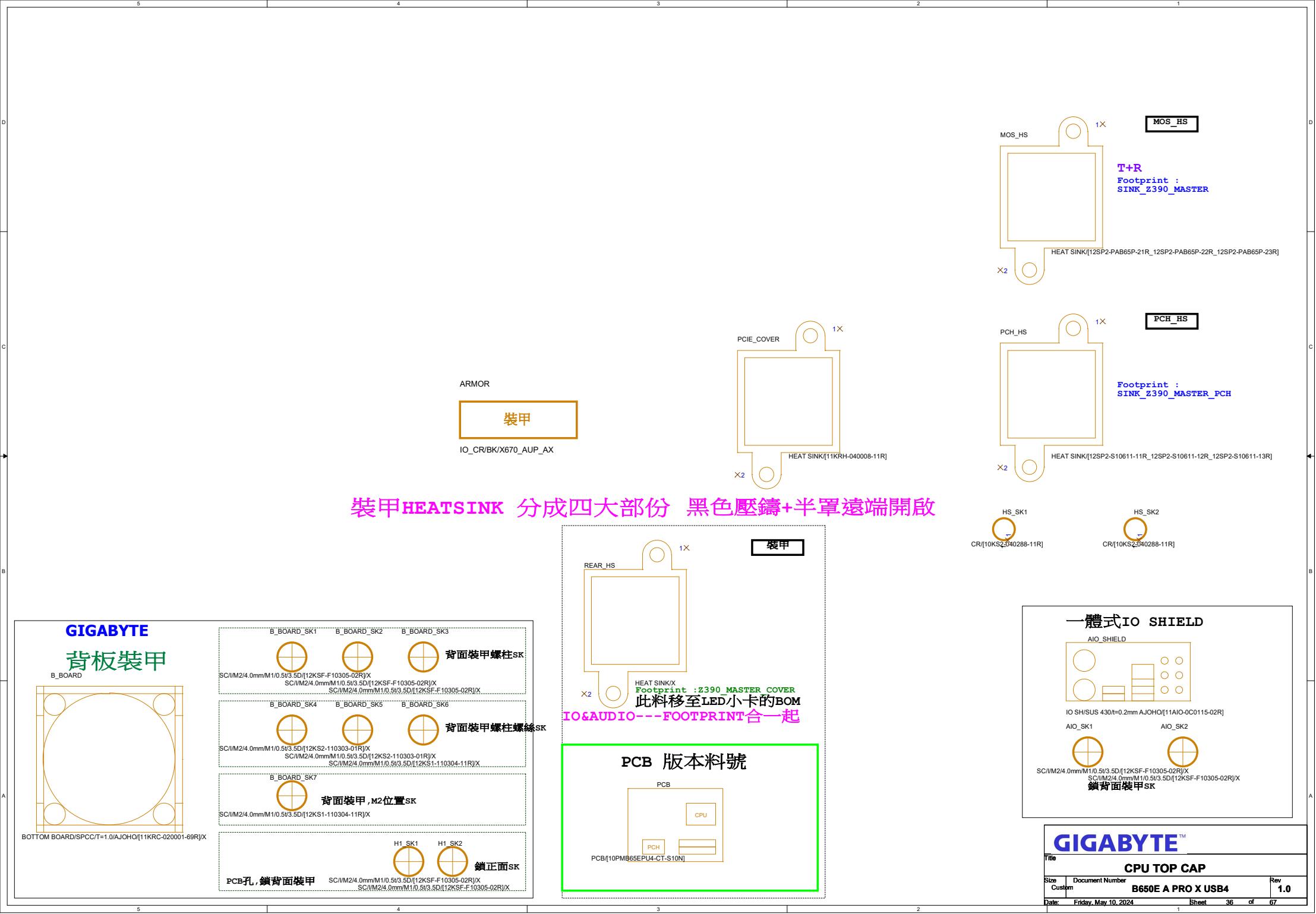




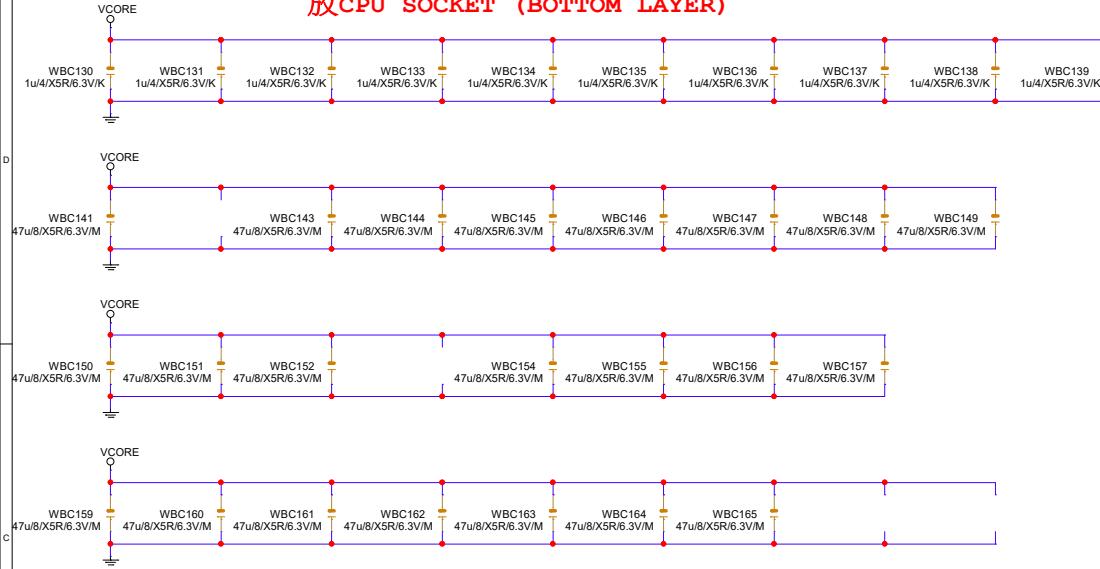
## FRONT HDMI



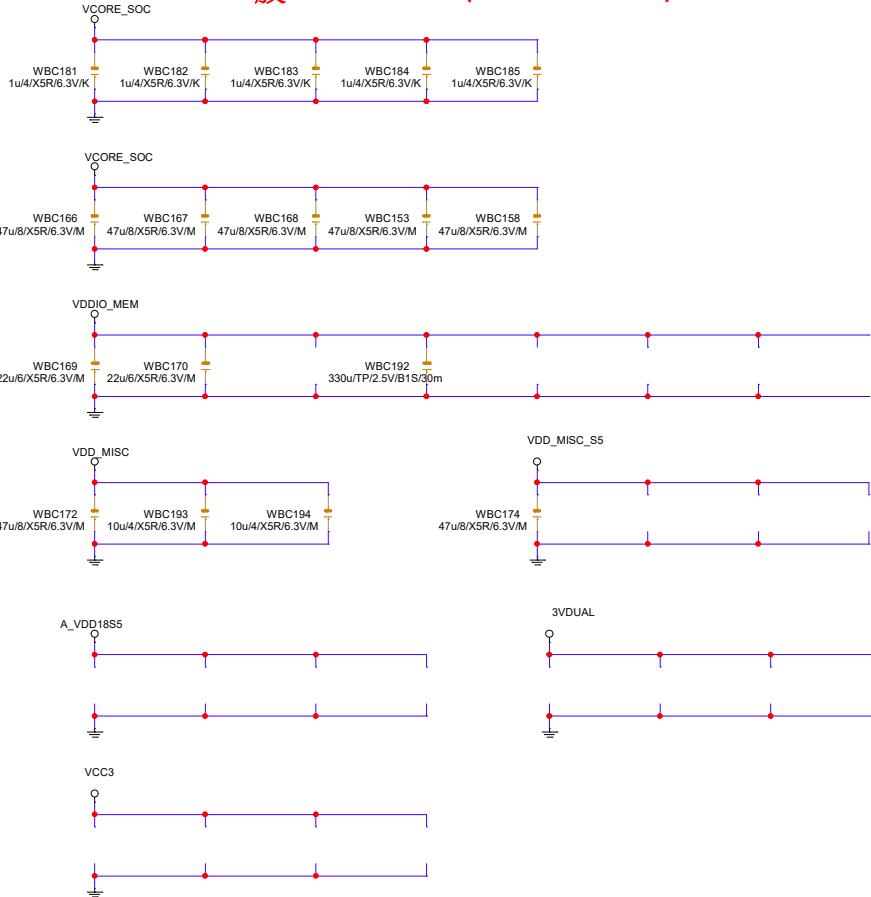




### 放CPU SOCKET (BOTTOM LAYER)



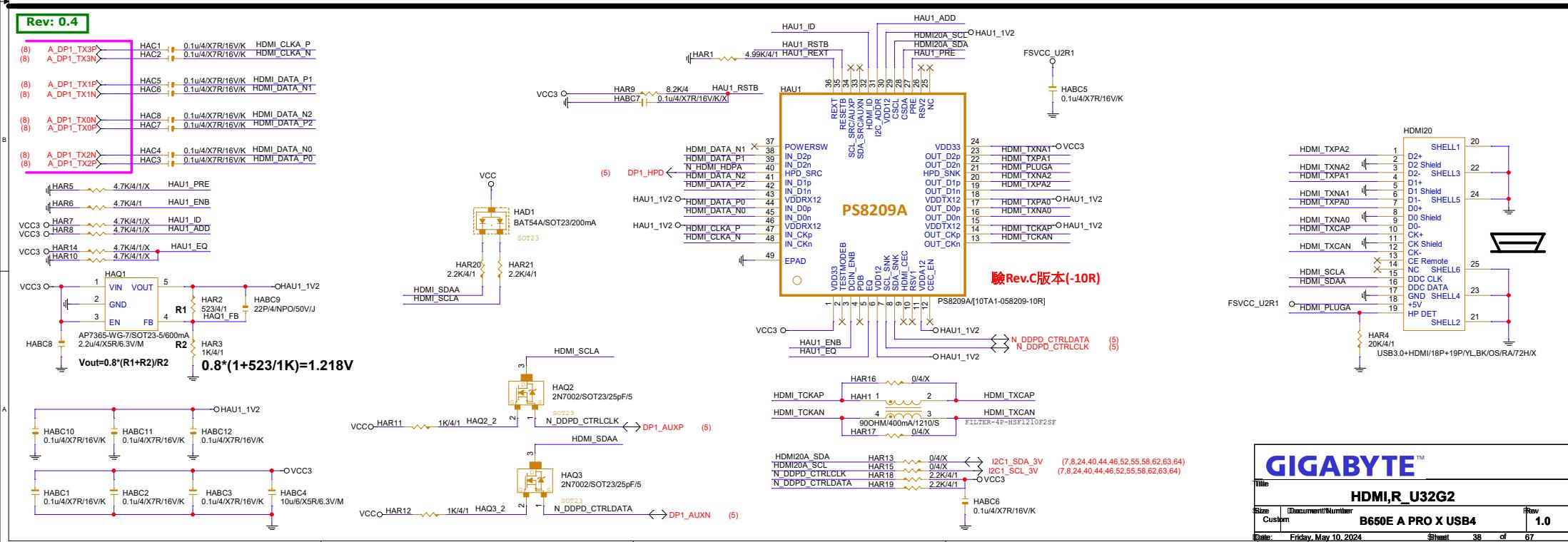
### 放CPU SOCKET (BOTTOM LAYER)



**GIGABYTE™**

CPU BOTTOM CAP

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請選擇適用的USBport :  
SOC/UD7/UD5/G1/G7 : USB4  
;UD3/G5:USB6

## NET 可變

(13) P\_HSDP7  
(13) P\_HSDN7

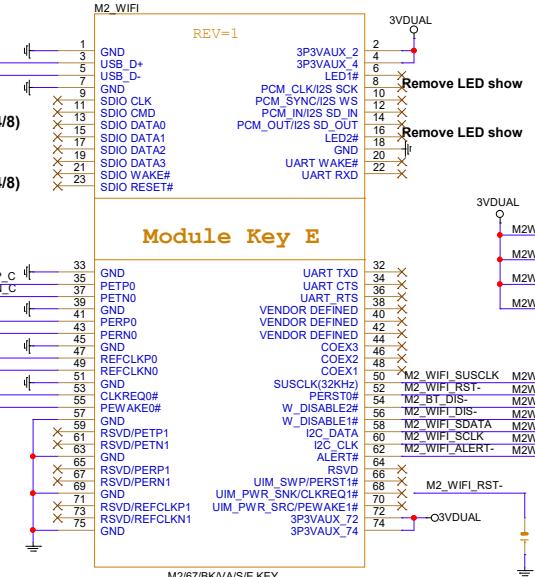
PCIE:15/4/4/15(breakout min 8/4/4/8)  
外層Impedance=85 ± 17.5%

PCIE:15/4/4/15(breakout min 8/4/4/8)  
內層 Impedance=85 ± 12%

## NET 可變

WIFI use PCIE port4 in X99

(14) LB\_ML\_OP M2WC4 0/4/SHT/M/X  
(14) LB\_ML\_OH M2WC5 0/4/SHT/M/X  
(14) LB\_ML\_IP M2WC1 0/4/SHT/M/X  
(14) LB\_ML\_IN M2WC2 0/4/SHT/M/X  
(12) CK\_WIFI\_100M\_DP M2WR4 22/4 WIFI\_CLKREQ-  
(12) CK\_WIFI\_100M\_DN M2WR6 0/4/SHT/20/X WIFI\_WAKE-  
WIFI\_CLKREQ connect to relative pin.  
3VDUAL M2WR1 8.2K4 WIFI\_CLKREQ-



## Footprint Notice.

\*Update  
2015-07-22  
\*Footprint  
for 立式  
SMD:  
WIFI-EKEY

## Footprint Notice.

\*Update  
2015-07-22  
\*Footprint for  
橫躺式SMD: NGFF-E-75P-2

## FOR M.2 WIFI MODULE @ REAR PANEL

\*Update  
2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線



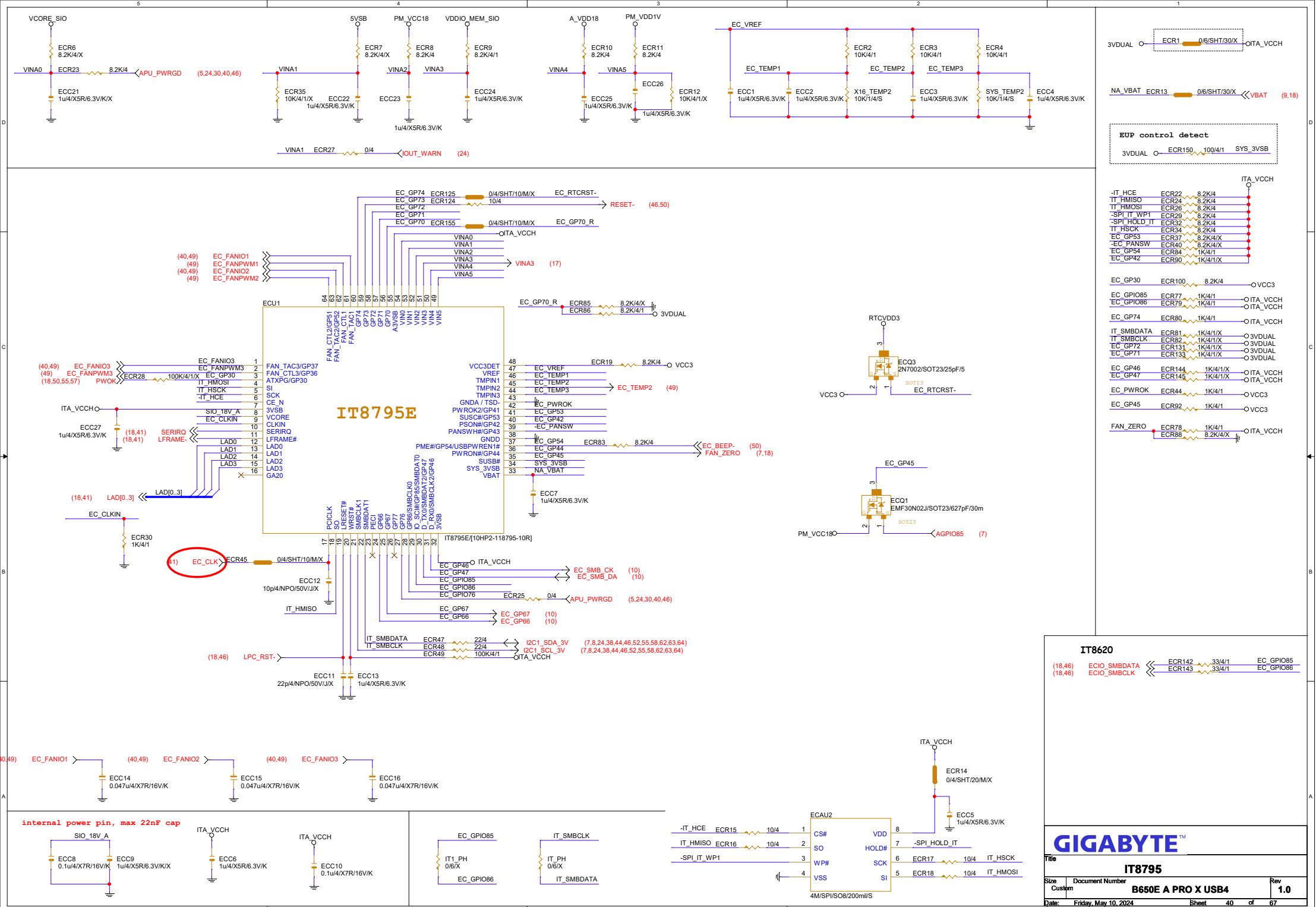
**GIGABYTE™**

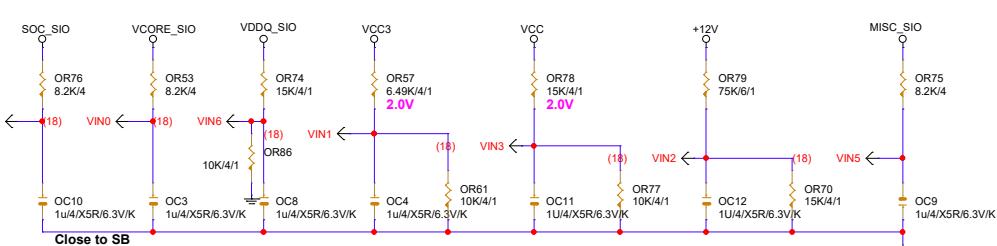
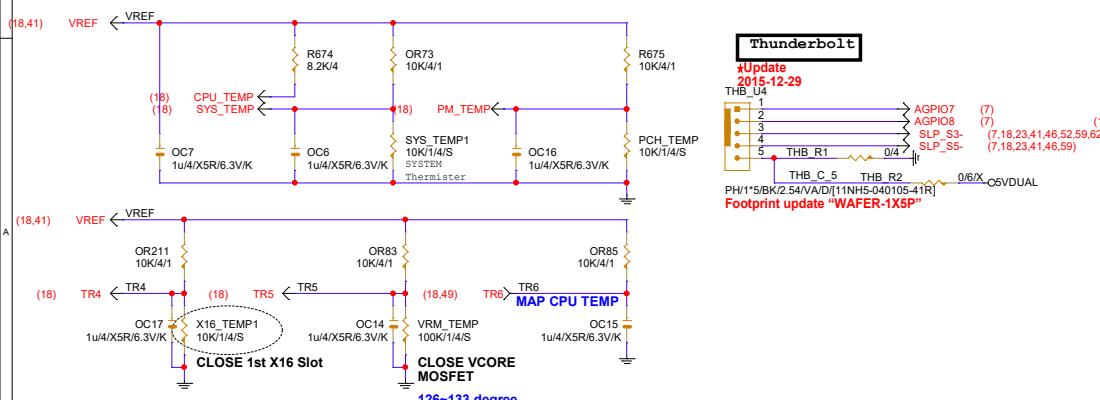
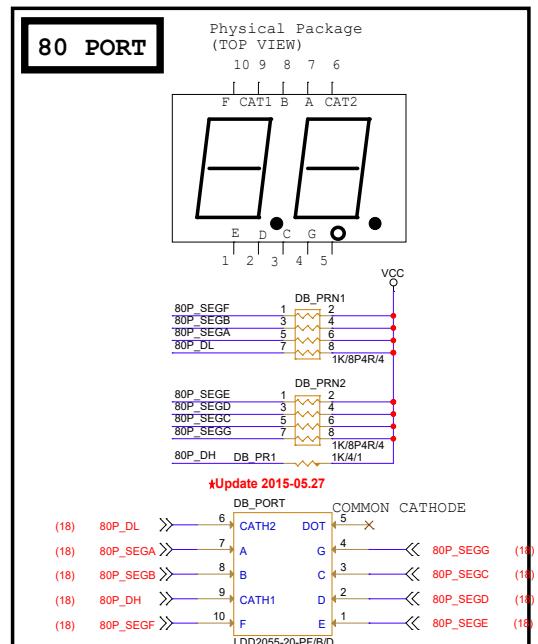
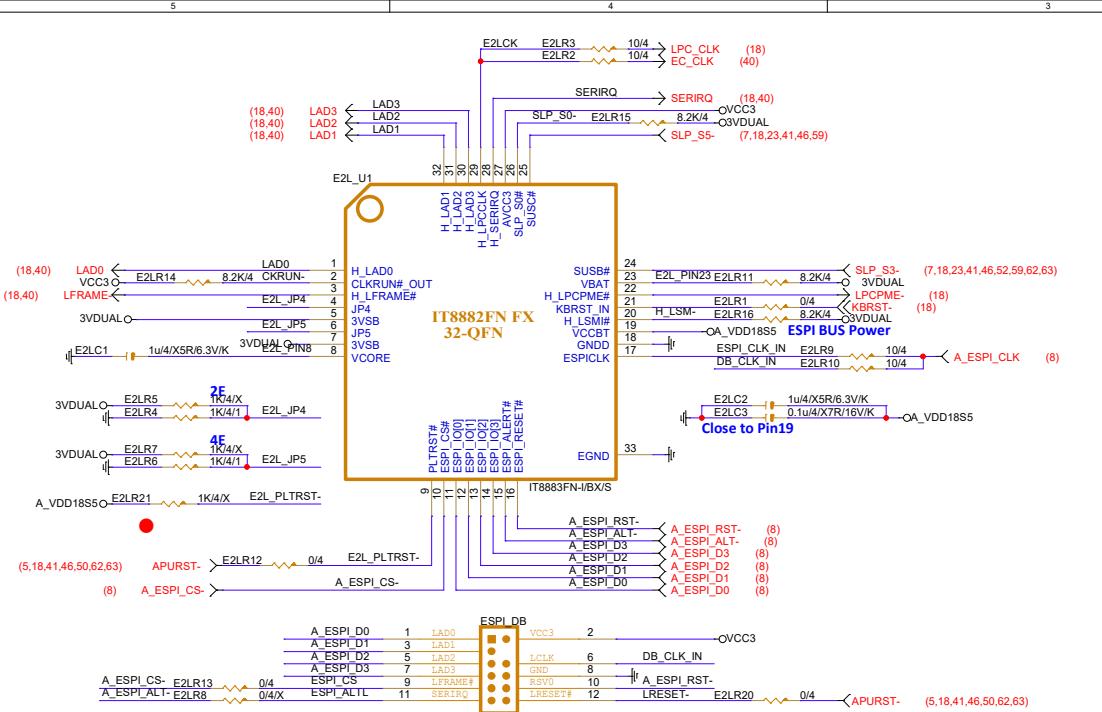
M2WIFI

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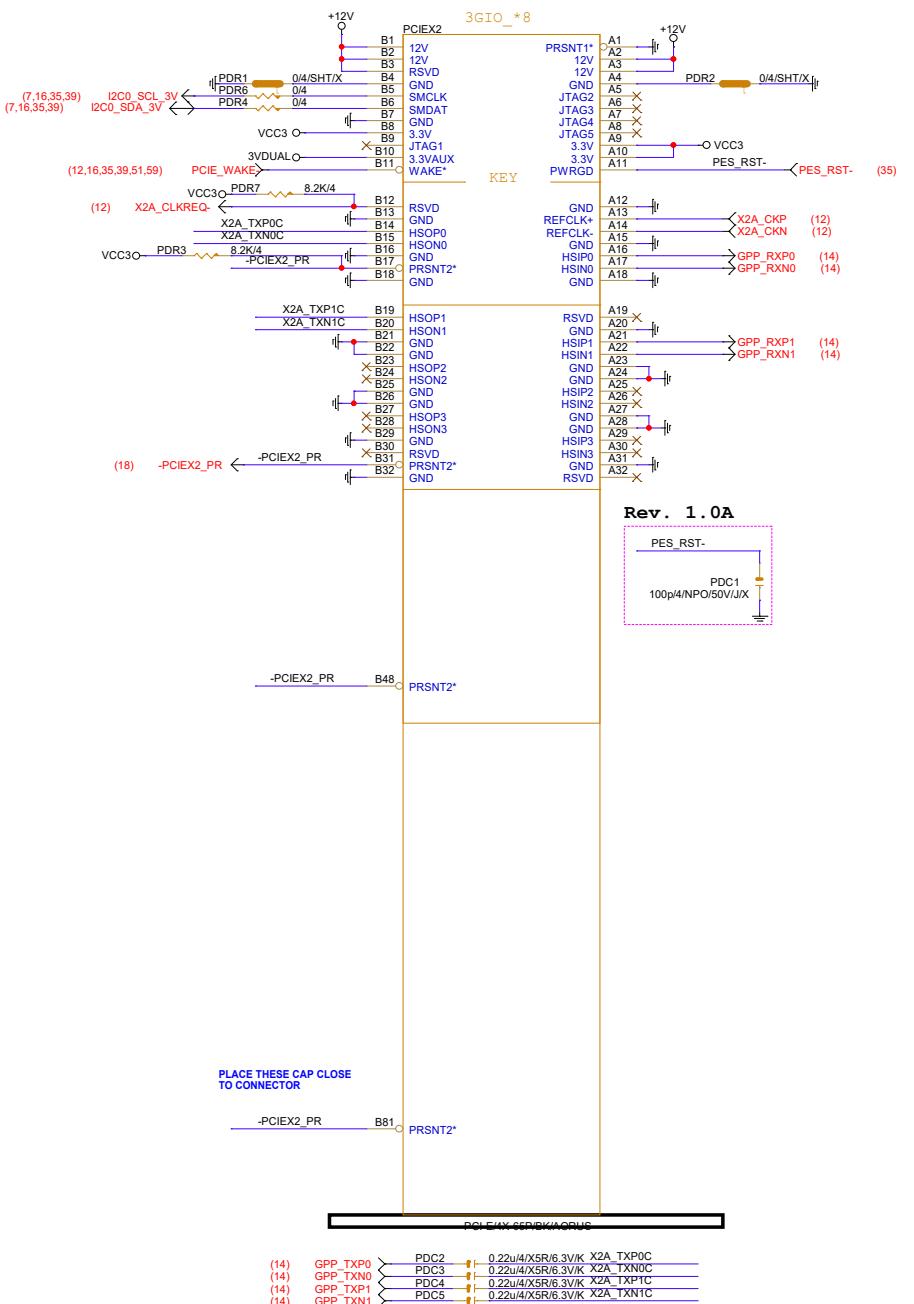


GIGABYTE™

IT8883 80 PORT

Document Number  
P050E A PRO X US

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D

D

c

c

B

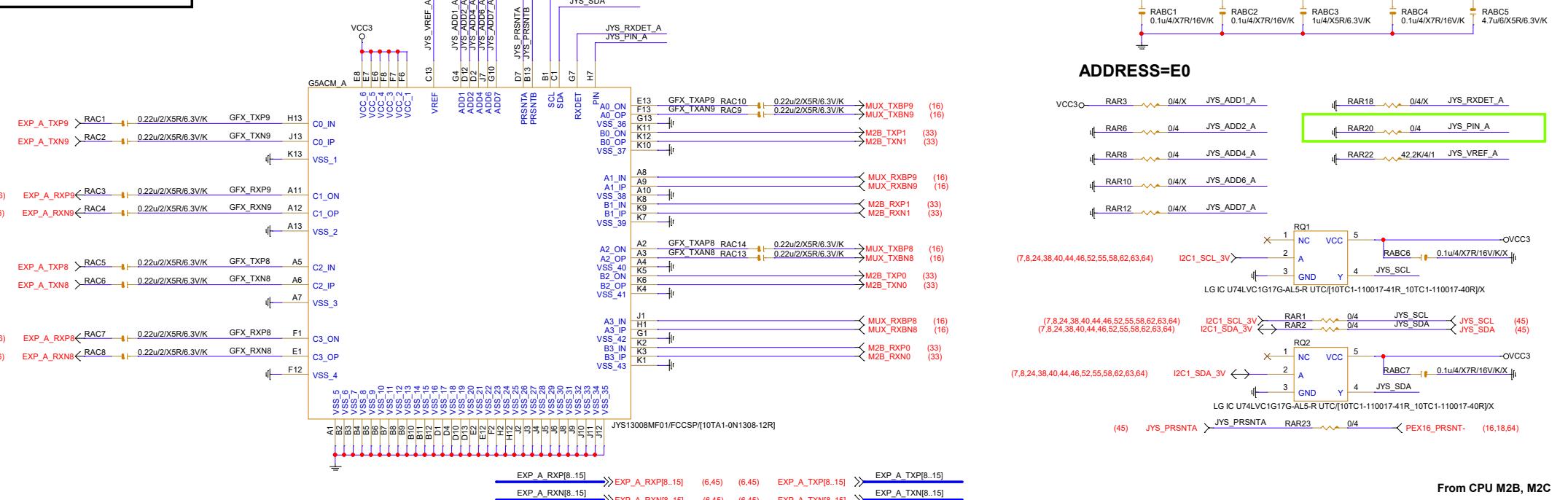
B

A

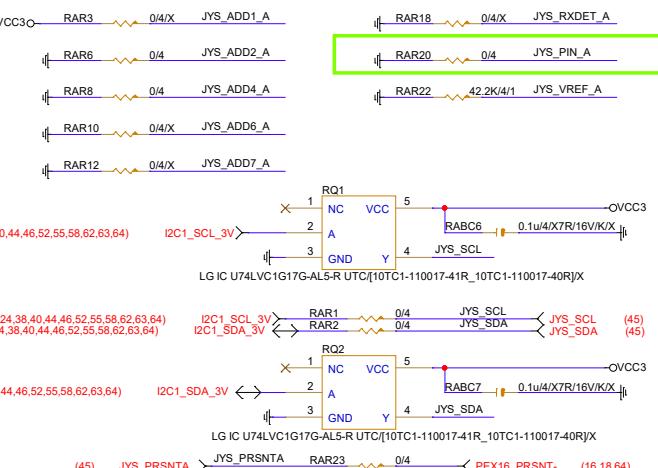
A

<b>GIGABYTE™</b>		
Title <b>CKG, HWM, TPM, THB</b>		
Size Custom	Document Number <b>B650E A PRO X USB4</b>	Rev 1.0
Date Friday, May 10, 2024	Sheet 43	of 67

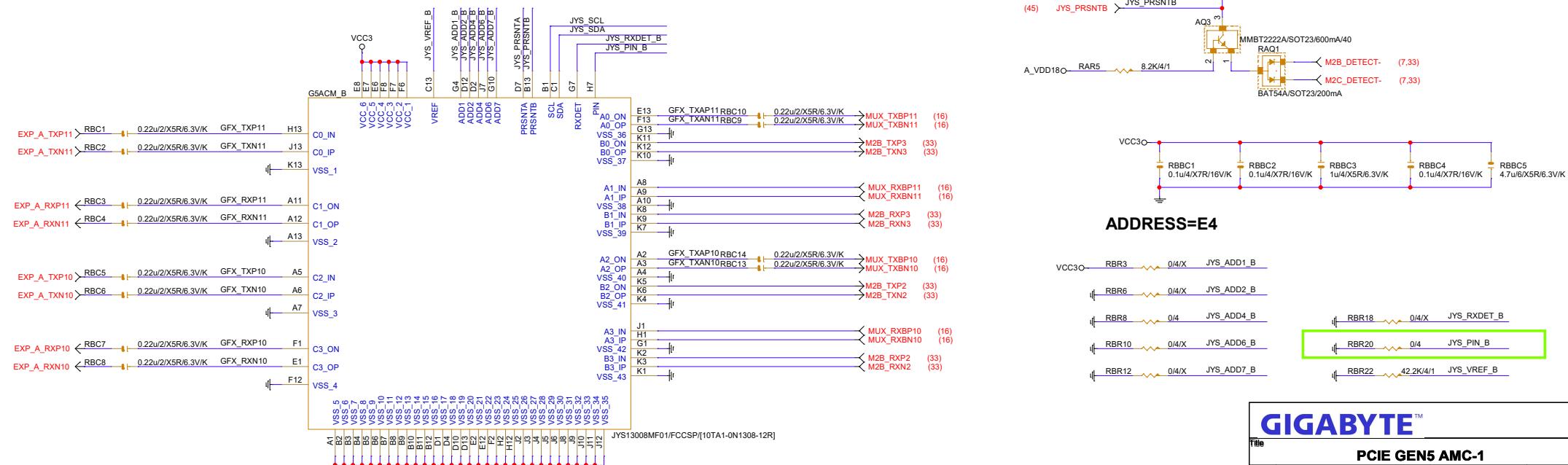
# PCIE GEN 5 ACTIV MUX



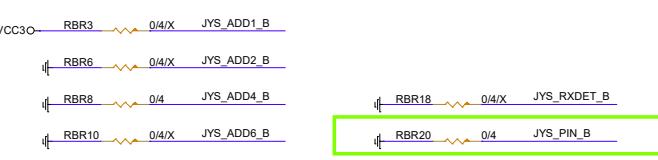
ADDRESS=E0



From CPU M2B, M2C



ADDRESS=E4

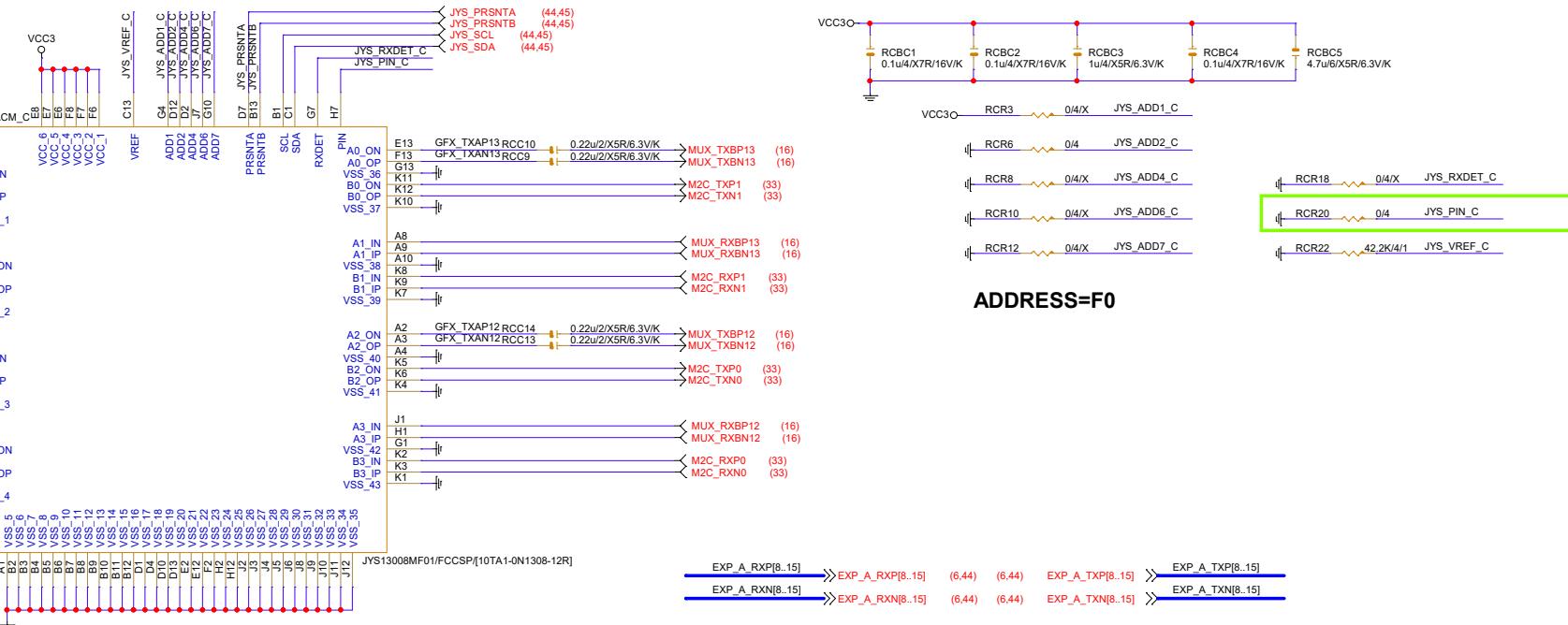


**GIGABYTE™**

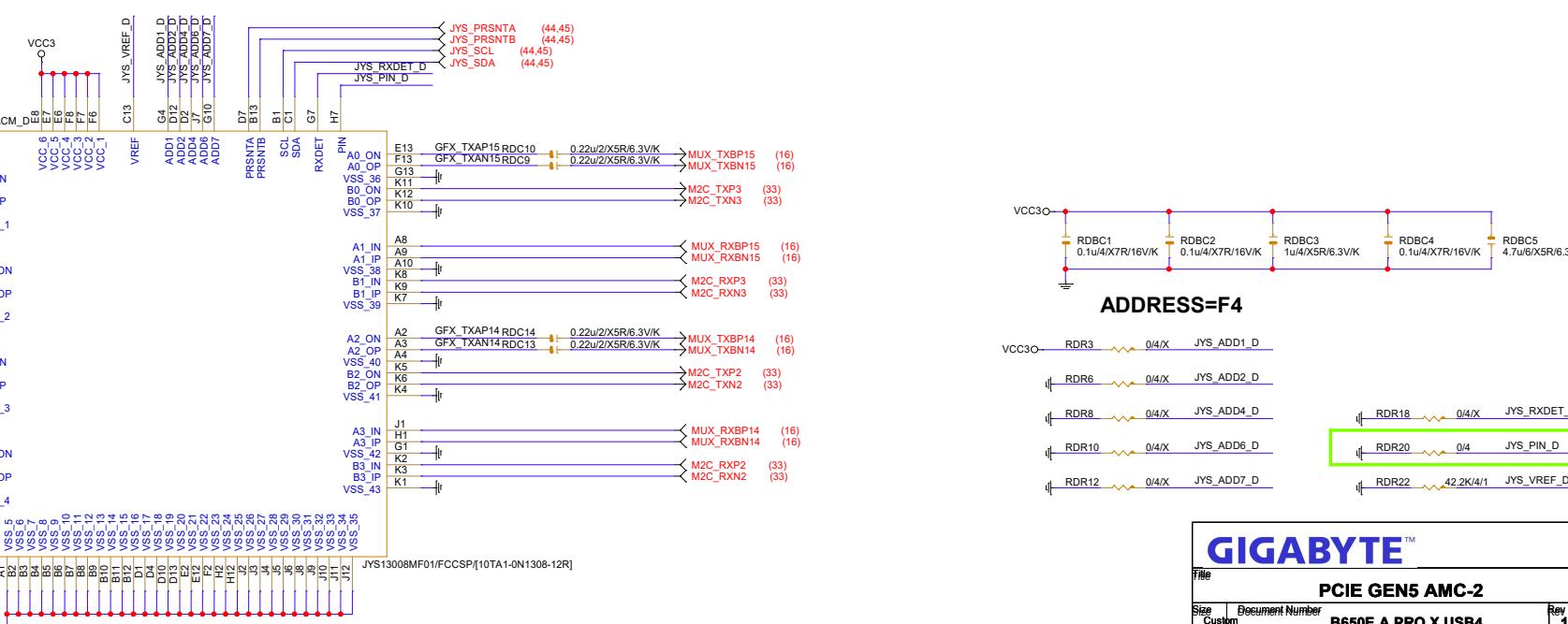
PCIE GEN5 AMC-1

Sheet	Document Number	Rev
Custom	B650E A PRO X USB4	1.0

## PCIE GEN 5 ACTITV MUX

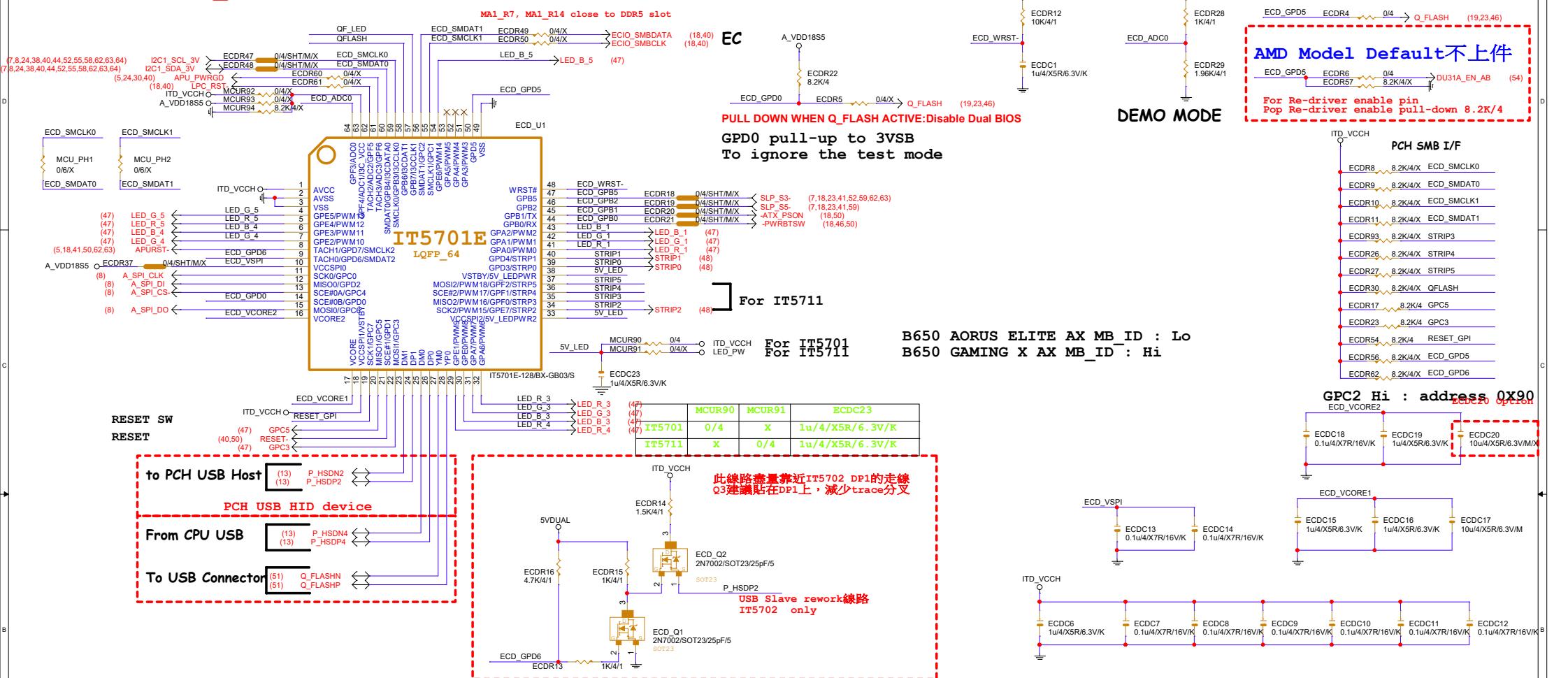


**ADDRESS=F0**

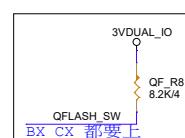
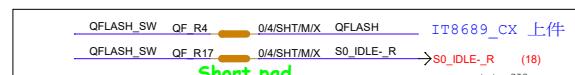


ADDRESS=

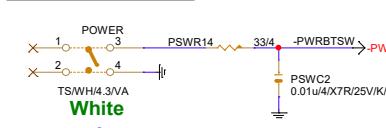
**ECD\_U1** 請放在PCH到BIOS路徑上. 避免線過長



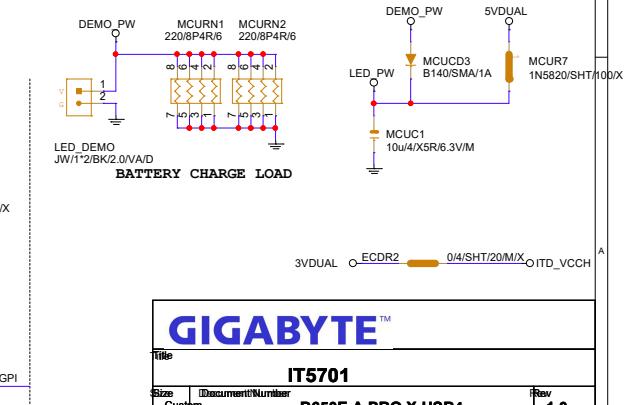
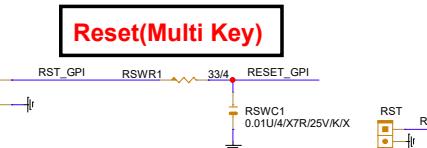
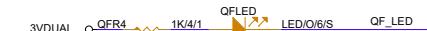
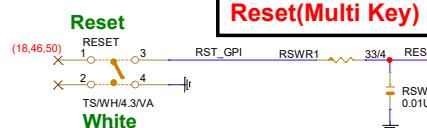
For IT8689 CX ERP QFLASH PLUS



## Power Button

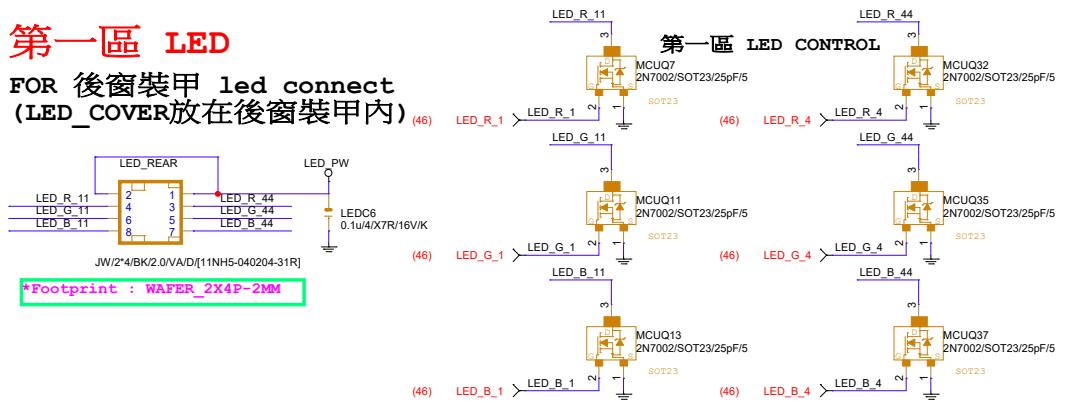


Footprint: TACT SW-POWER

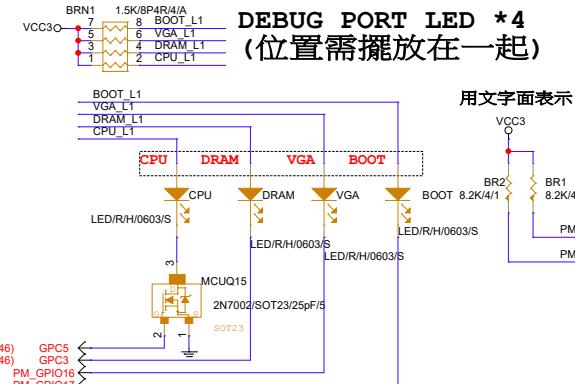


## 第一區 LED

FOR 後窗裝甲 led connect  
(LED\_COVER放在後窗裝甲內)



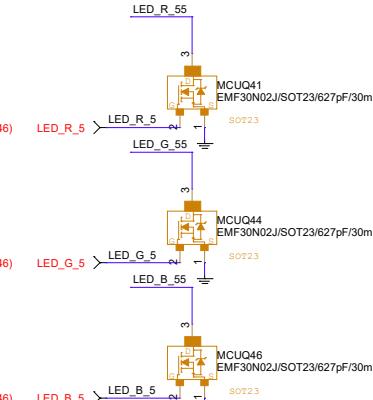
**DEBUG PORT LED \*4**  
(位置需擺放在一起)



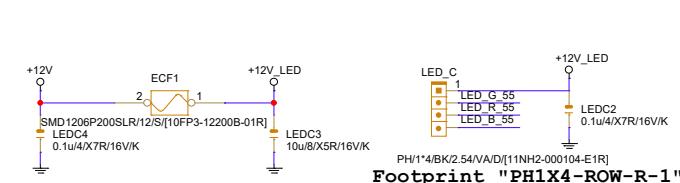
## 第三區 LED

## 第五區 LED

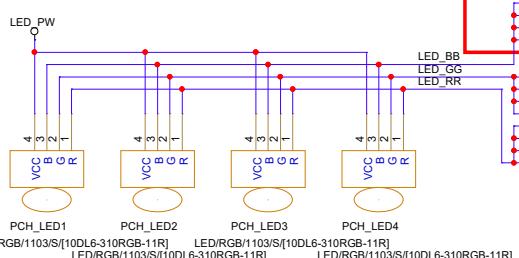
### 第五區 LED CONTROL



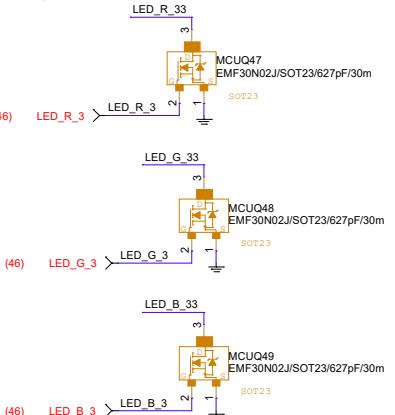
燈條 LED (LED\_C放在PCB左邊板邊位置)



## 第三區 LED



### 第三區 LED CONTROL

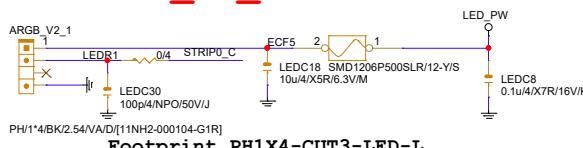


**GIGABYTE™**

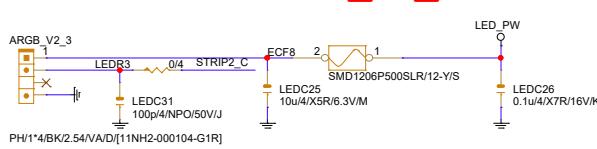
**MODEL / PCB /AUDIO/PCIe LED**

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Custom		1.0
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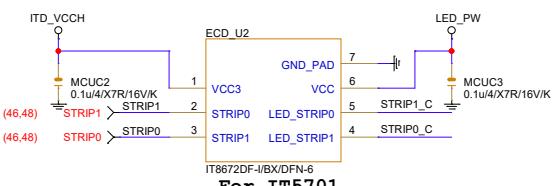
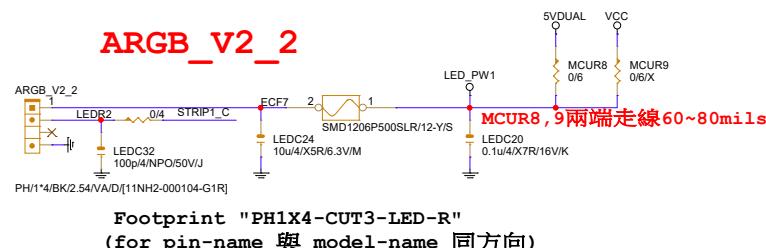
## 第六區 LED (靠近左上板邊位置)

**ARGB\_V2\_1****ARGB\_V2\_3**

位置須和ARGB\_V2\_1放在一起



## 第七區(靠近右下CPU板邊位置)

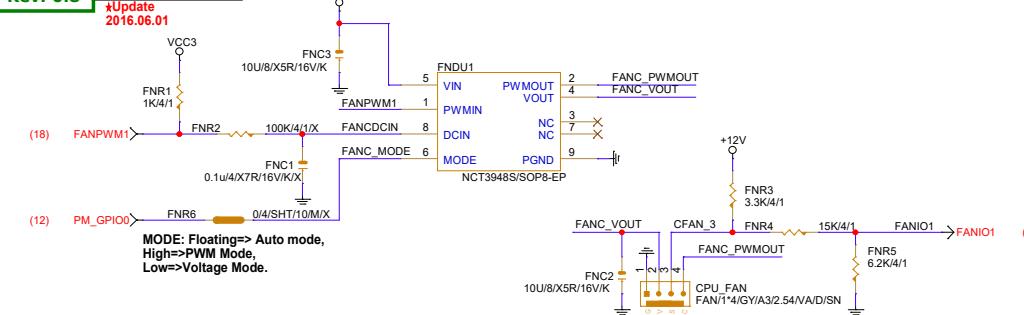
**ARGB\_V2\_2**

(46,48) STRIP0 > MCUR85 ~0/4/X STRIP0\_C For IT5711  
 (46,48) STRIP1 > MCUR86 ~0/4/X STRIP1\_C For IT5711  
 (46) STRIP2 > MCUR87 ~0/4/X STRIP2\_C For IT5711  
 STRIP0\_C MCUR88 ~0/4 STRIP2\_C For IT5701

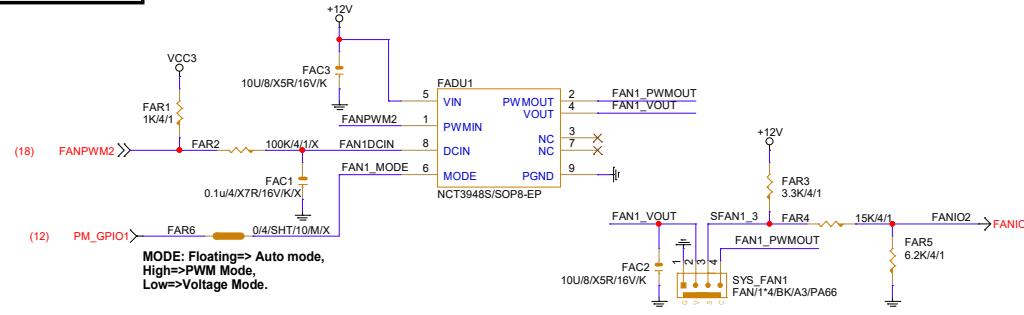
	ECD_U2	MCUR88	MCUR85	MCUR86	MCUR87	MCUC2	MCUC3
IT5701	0/4	0/4	X	X	X	0.1u/4	0.1u/4
IT5711	X	X	0/4	0/4	0/4	X	X

**GIGABYTE™**
**D\_LED,FAN,8**
**B650E A PRO X USB4**
**1.0**
**Date: Friday, May 10, 2024**
**Sheet 48 of 67**

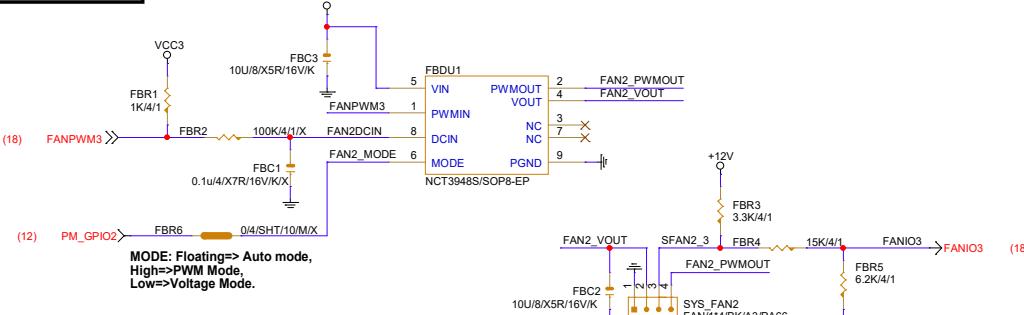
**CPU SMART FAN**



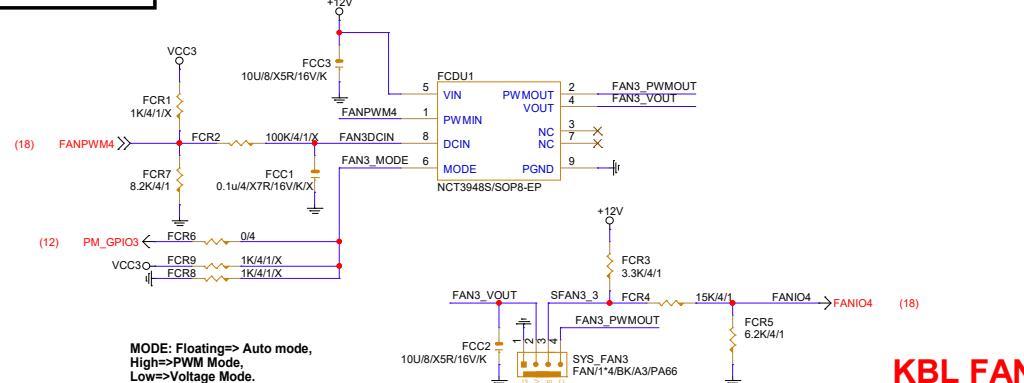
**SYSTEM FAN1**



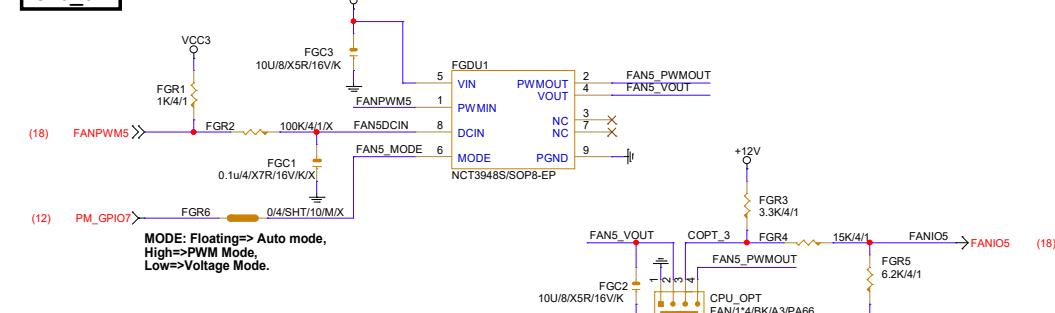
**SYSTEM FAN2**



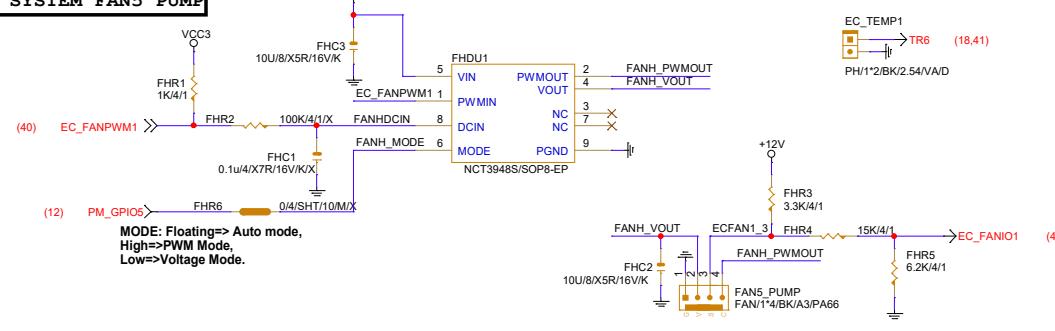
**SYSTEM FAN3**



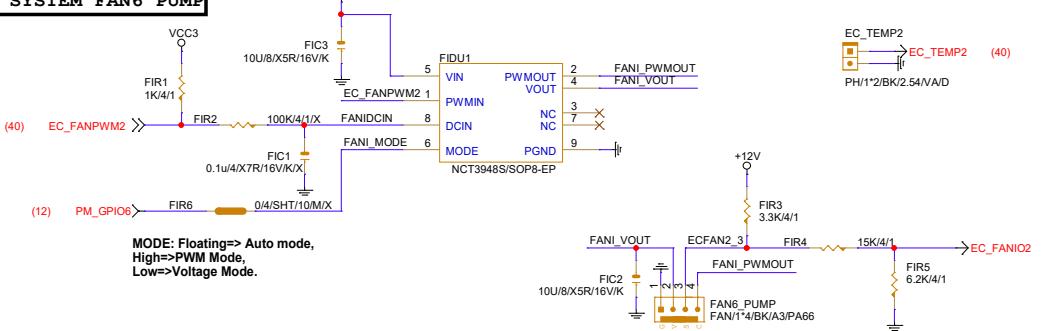
**CPU\_OPT**



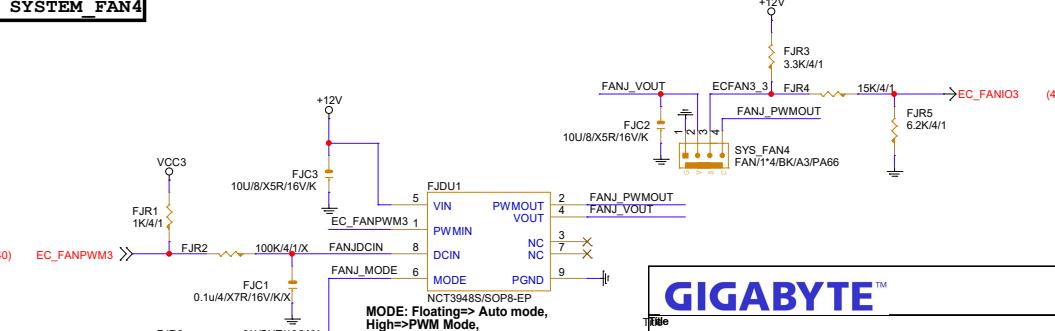
**SYSTEM FAN5 PUMP**



**SYSTEM FAN6 PUMP**



**SYSTEM\_FAN4**



**GIGABYTE™**

**FAN**

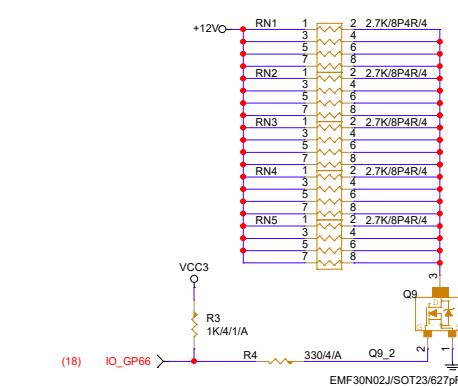
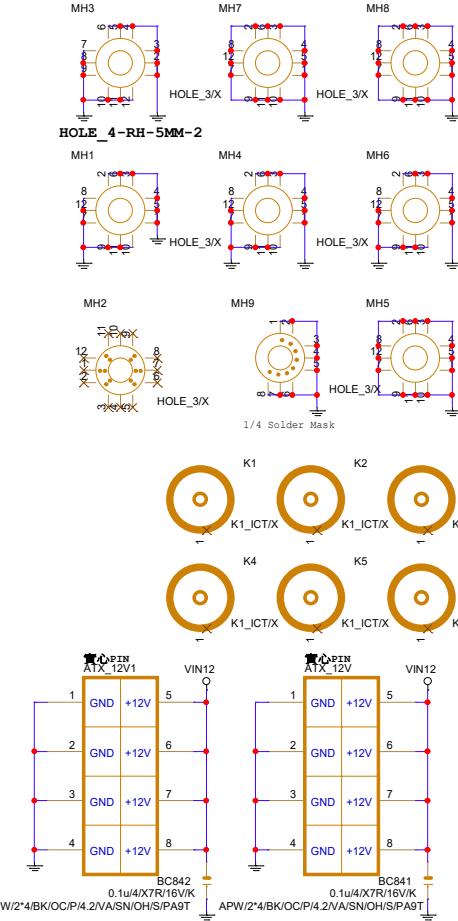
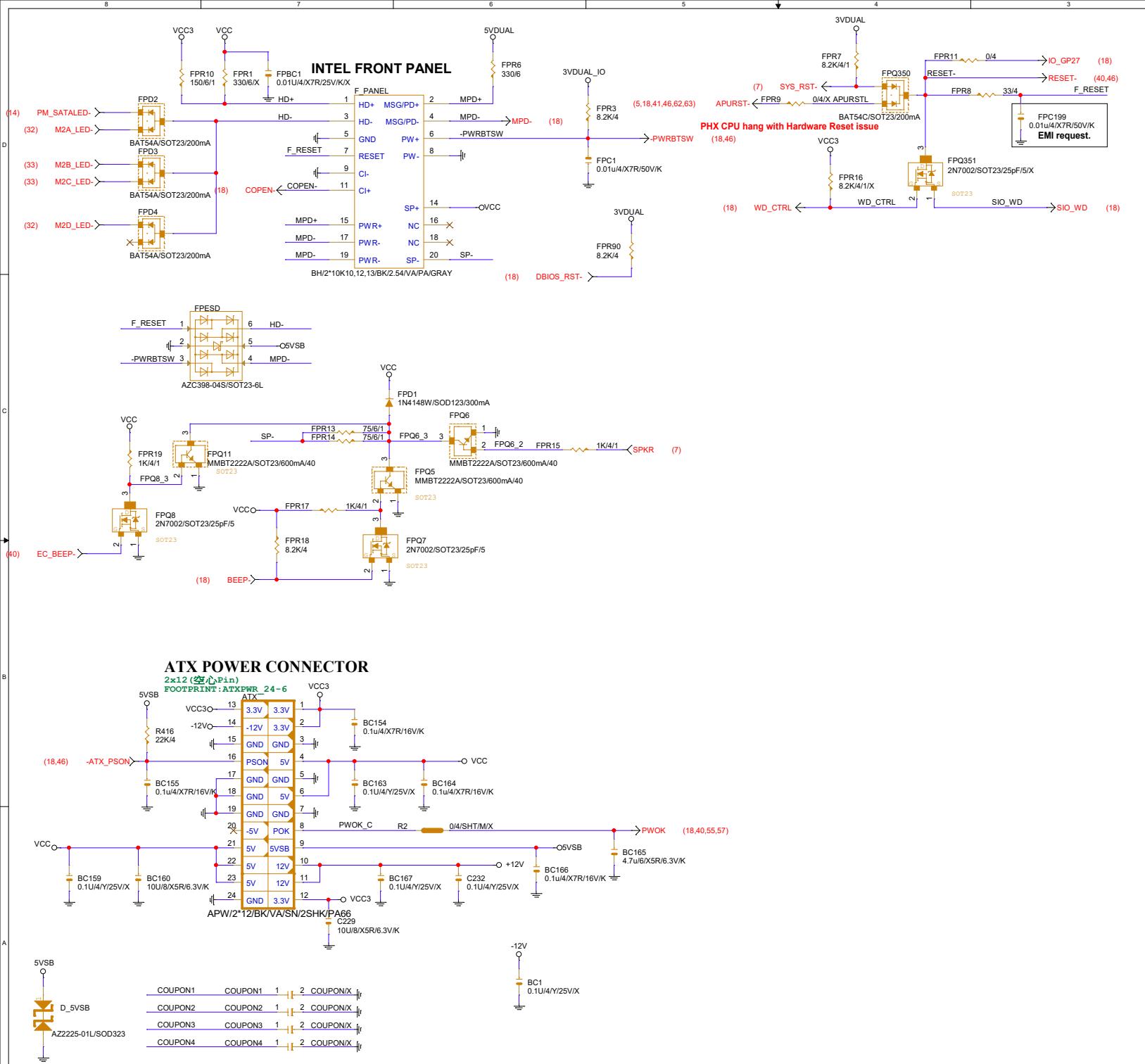
**B650E A PRO X USB4**

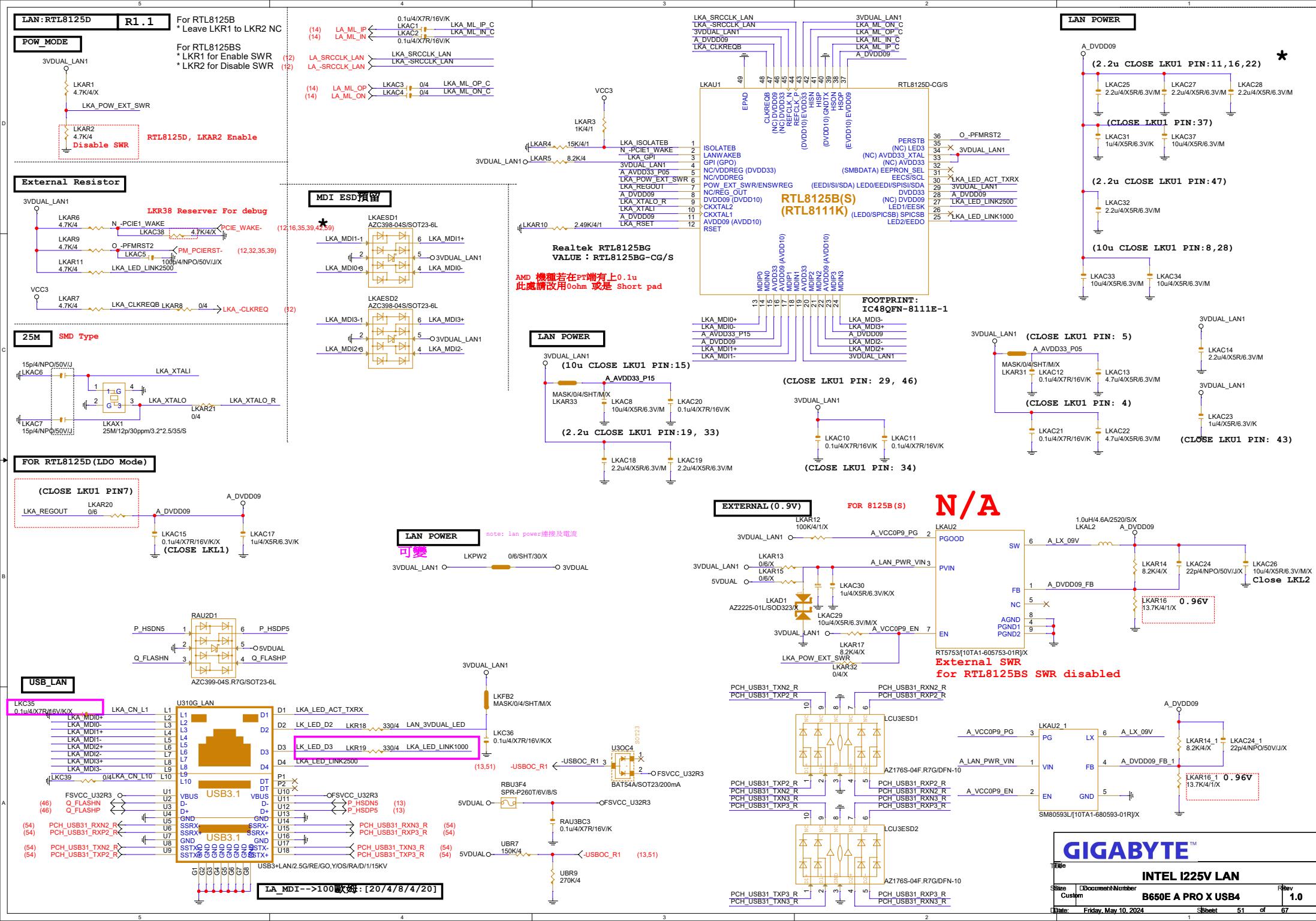
**Rev 1.0**

**KBL FAN LOCATION MAP REFER TO PAGE.27**

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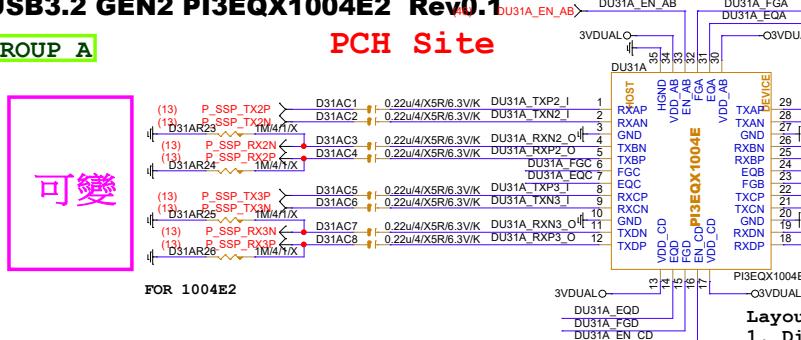


**USB3.2 GEN2 PI3EQX1004E2 Rev0.1**

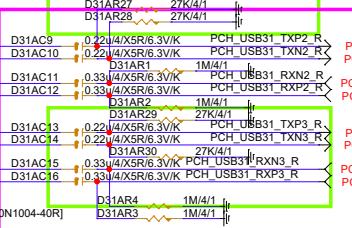
## PCH Site

P A

可變

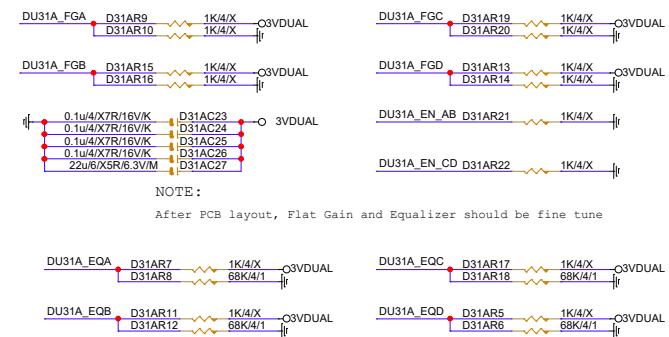


## **USB Type A Connector Site**

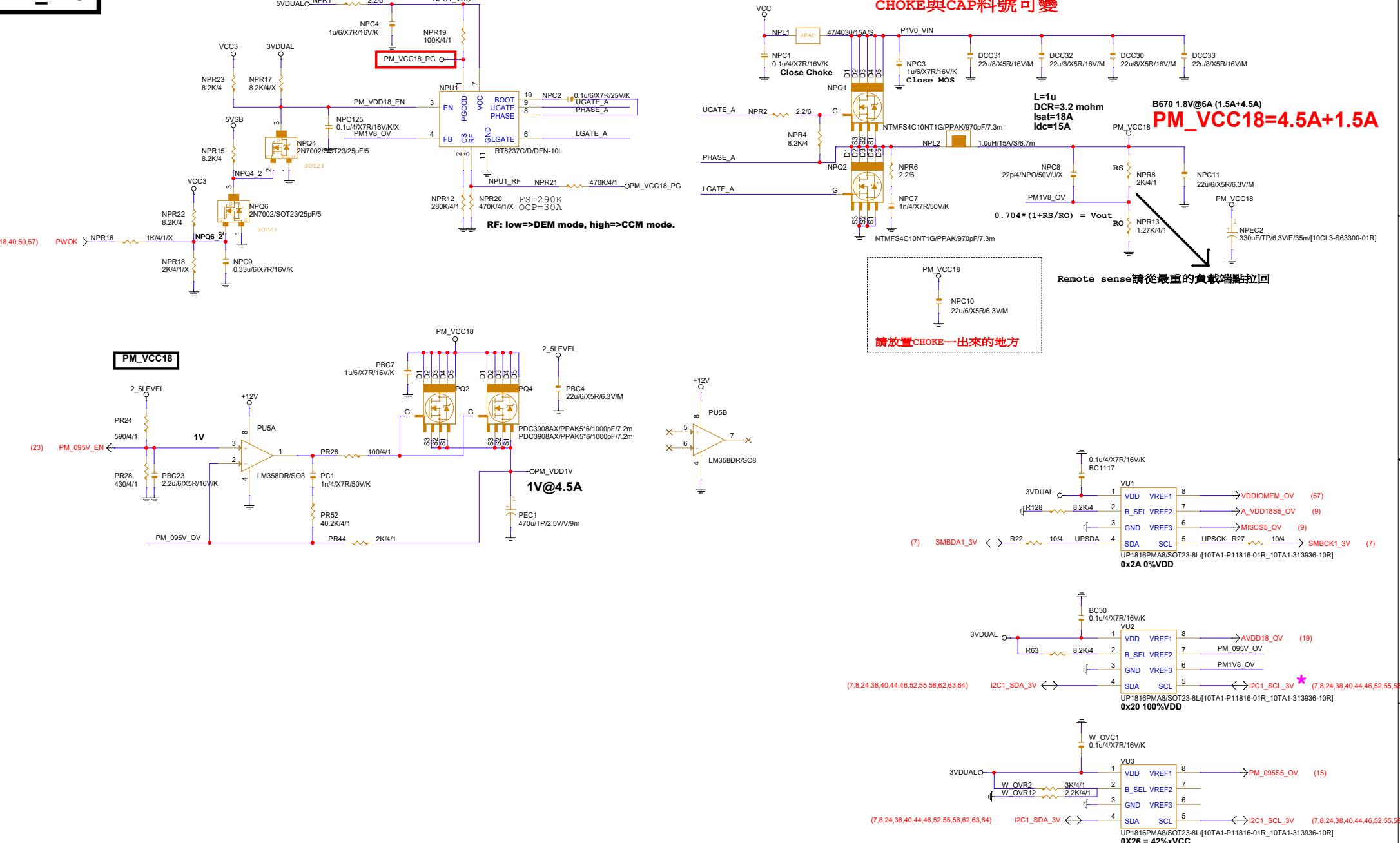


## Layout Rule

1. Differential Pair can't be swaped
  2. Redriver to Connector Length min. 1 inch
  3. PCH to Redriver Length min. 6 inch

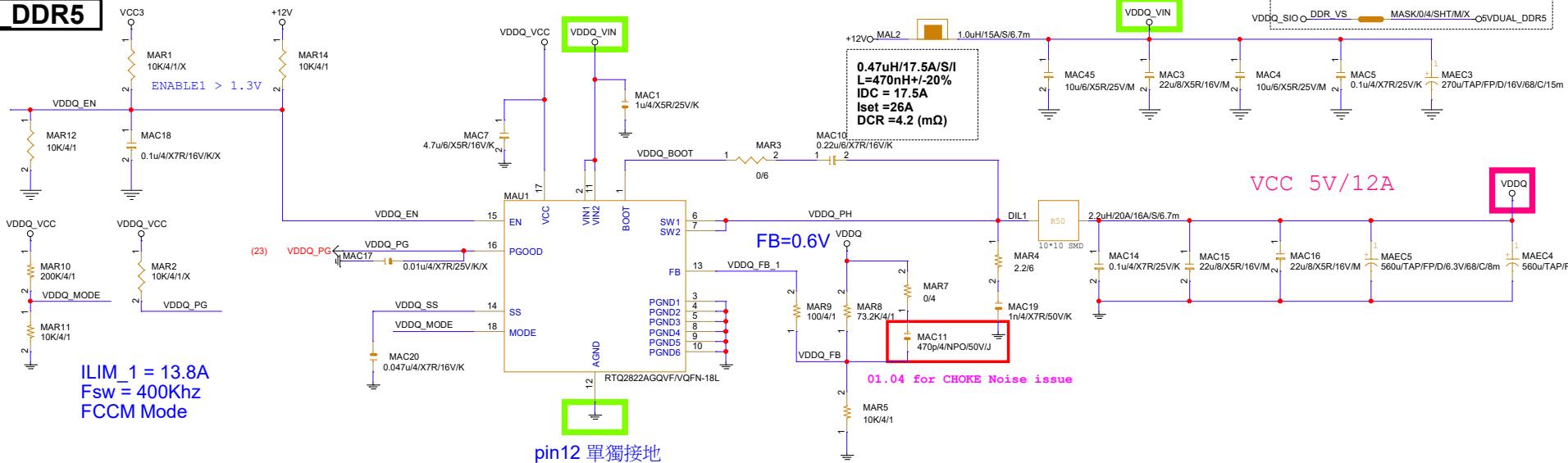


NOTE:  
After PCB layout, Flat Gain and Equalizer should be fine

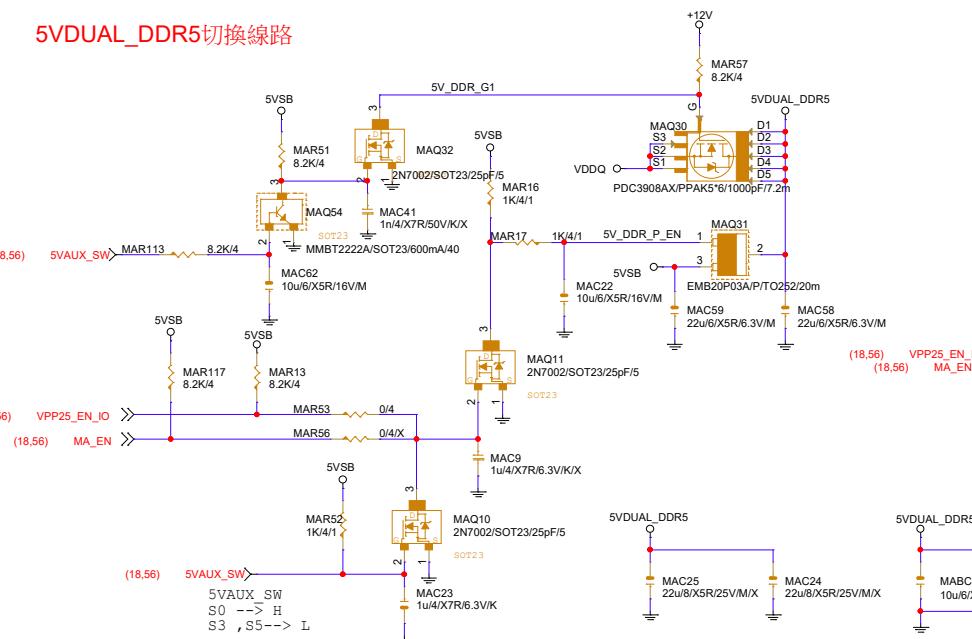


## **5VDUAL\_DDR5**

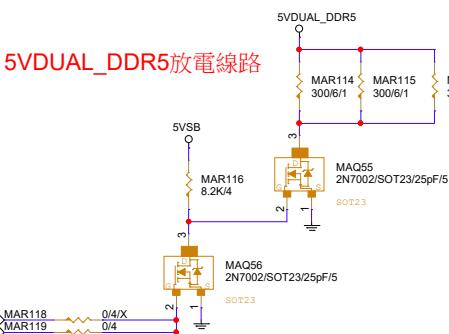
REV:0.13



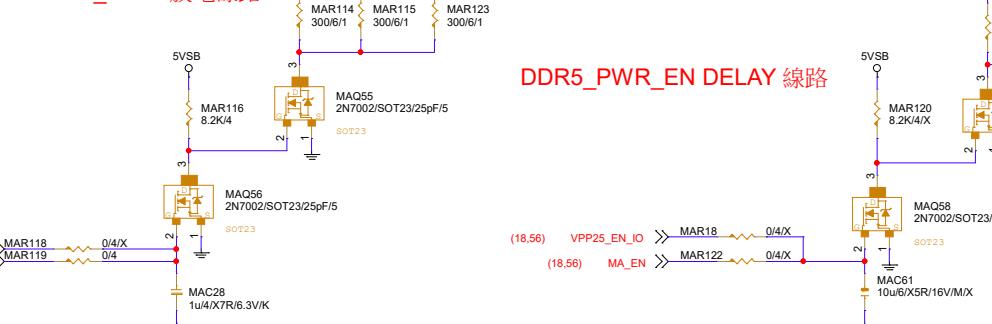
## 5VDUAL DDR5切換線路

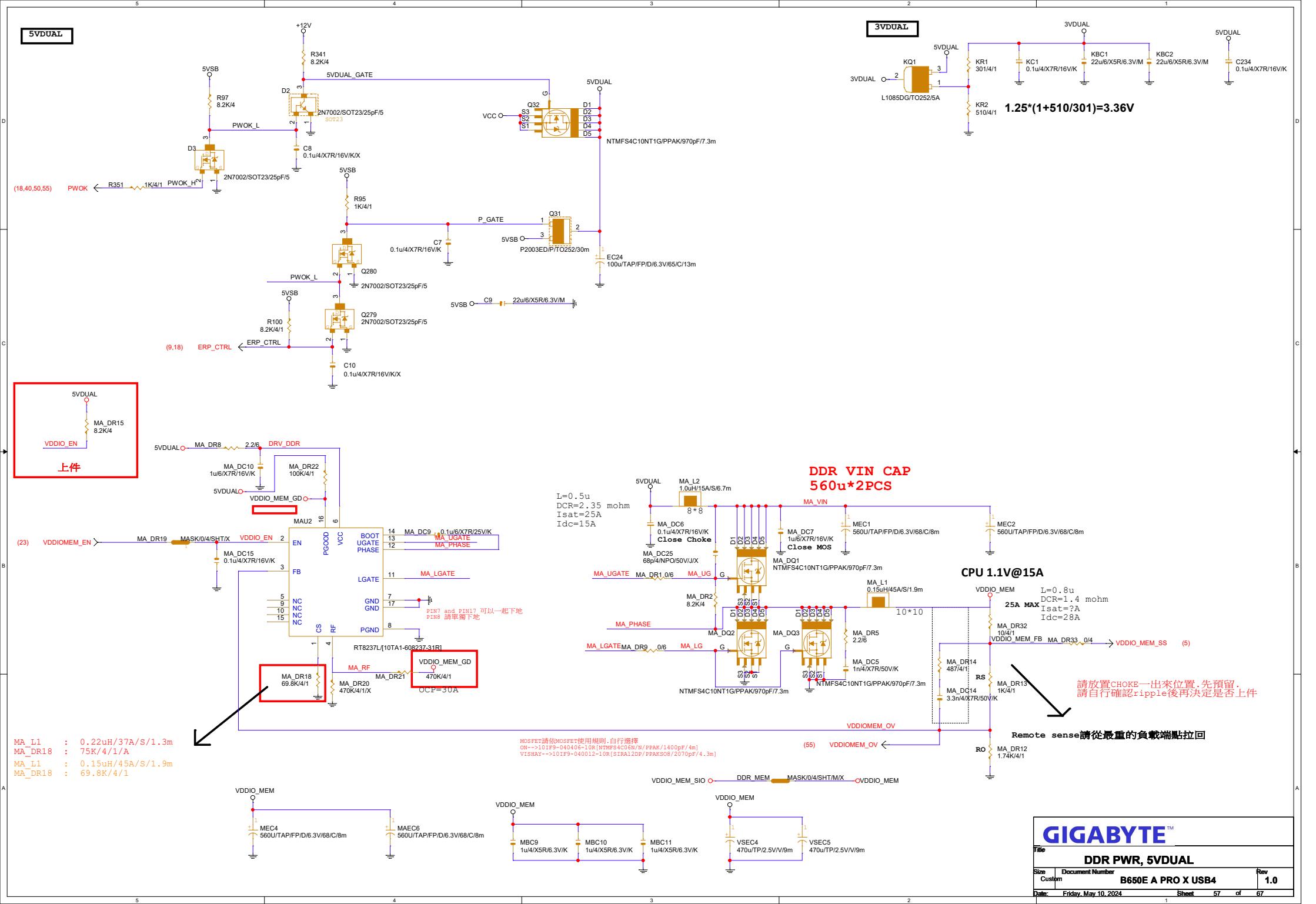


5VDUAL DDR5放電線路

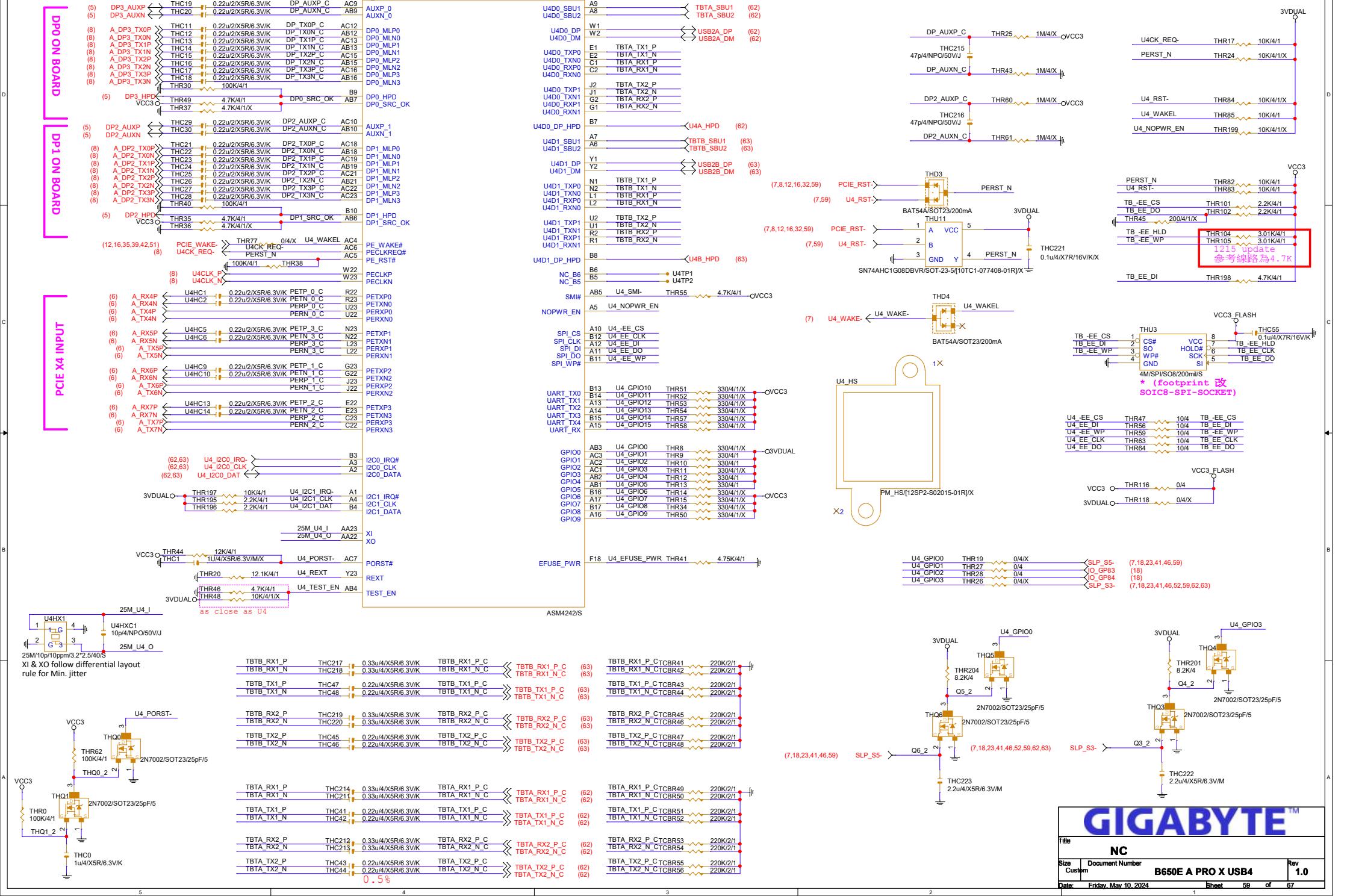


## DDR5 PWR EN DELAY 線路

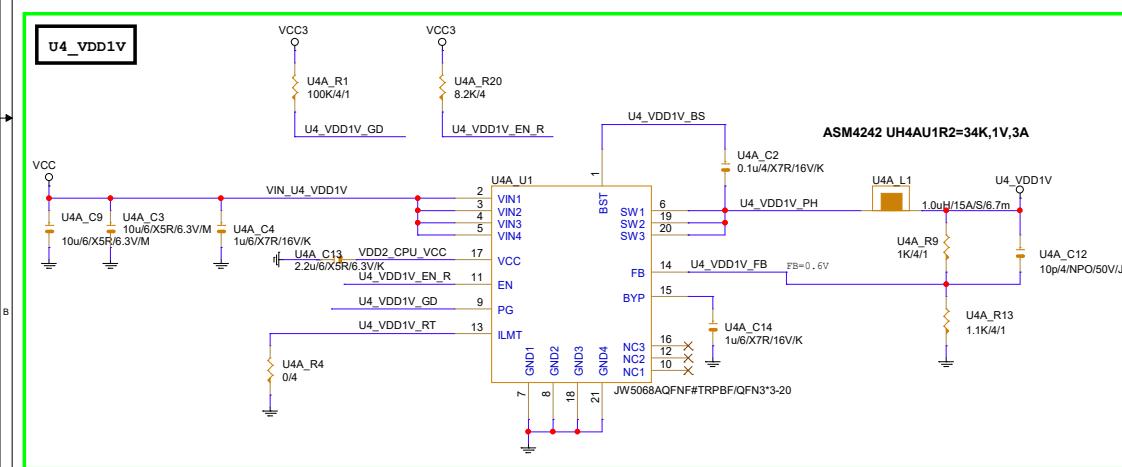
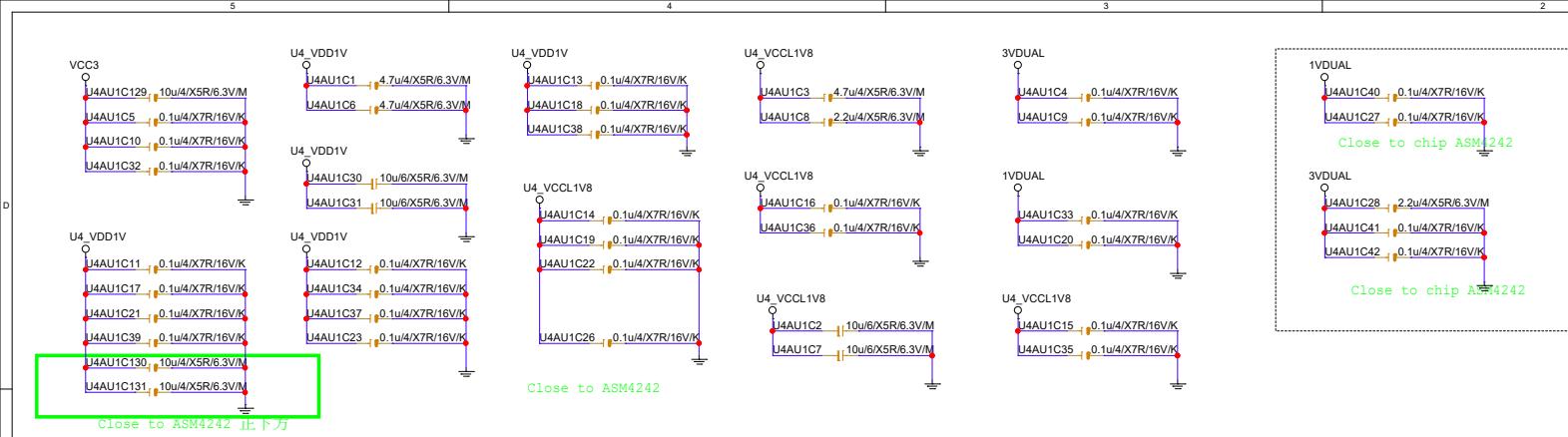






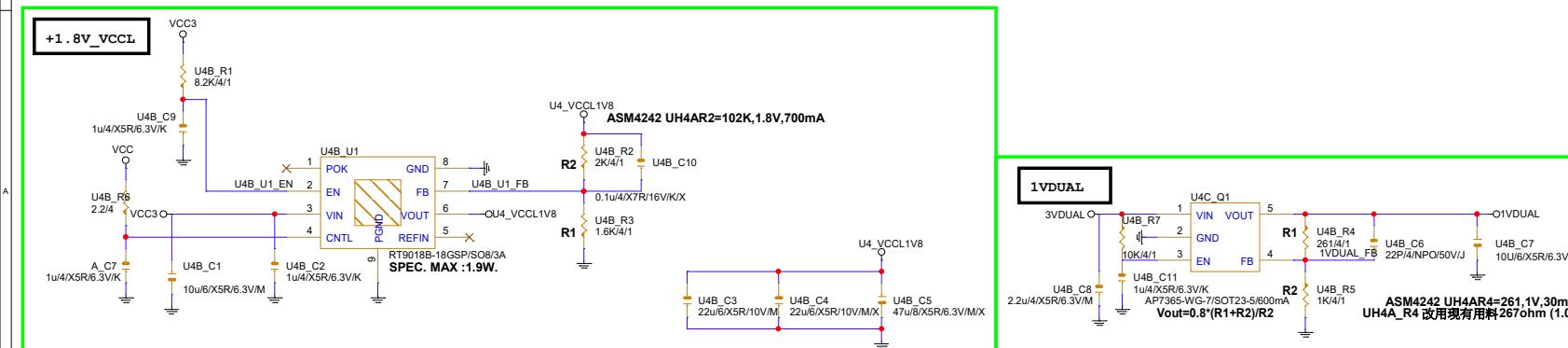






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+3.3V\_VCCH ----- 15mA  
 +1.8V\_VCCL ----- 700mA  
 +1V\_VDD----- 3000mA  
 VSUS\_1V----- 30mA  
 VSUS\_3V3----- 70mA

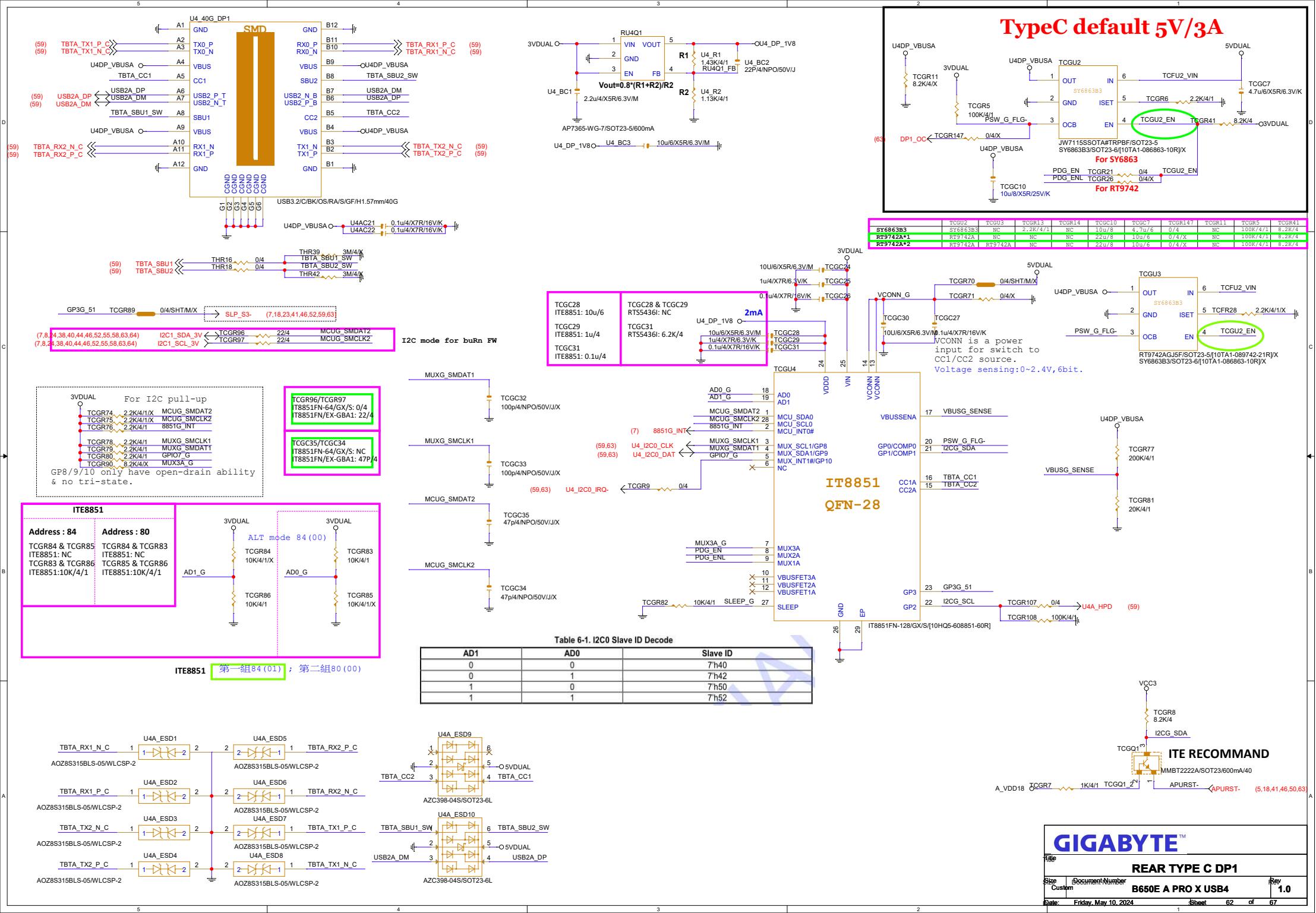


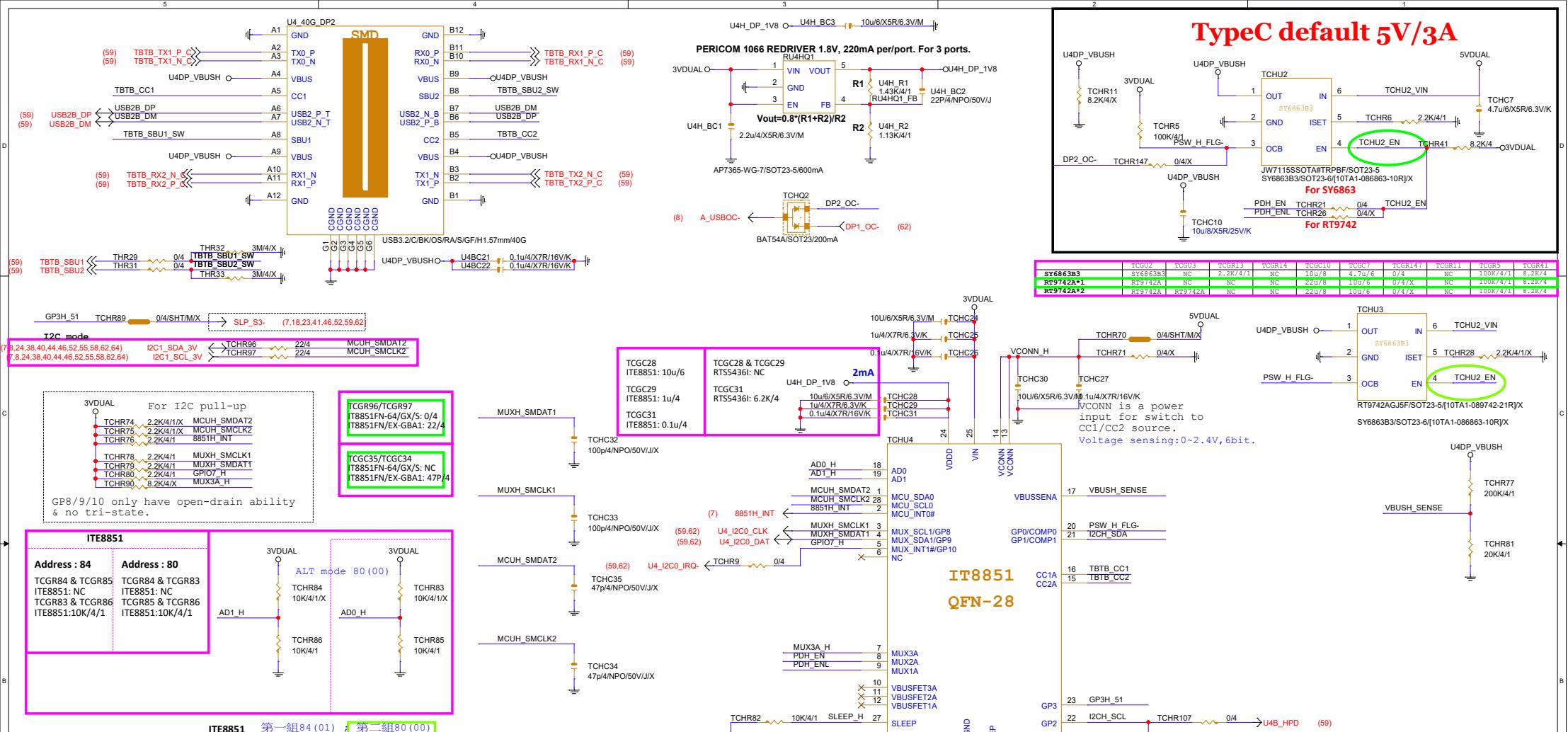
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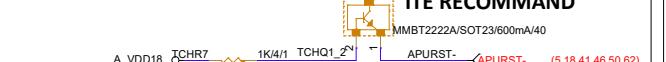
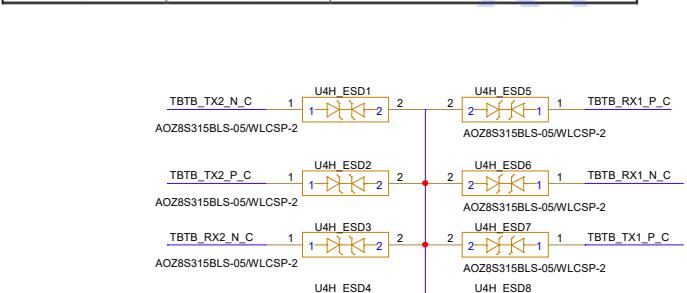
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**Table 6-1. I<sub>2</sub>C0 Slave ID Decode**

<b>AD1</b>	<b>AD0</b>	<b>Slave ID</b>
0	0	7h40
0	1	7h42
1	0	7h50
1	1	7h52



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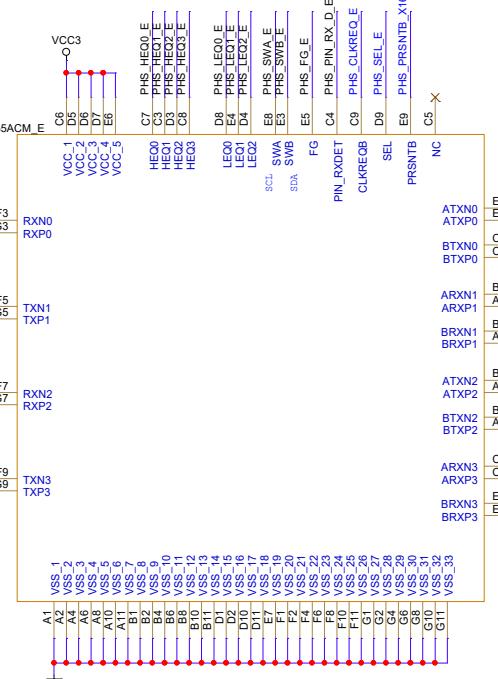
READY TO

**REAR TYPE C DP1**

**B650E A PRO X USB4**

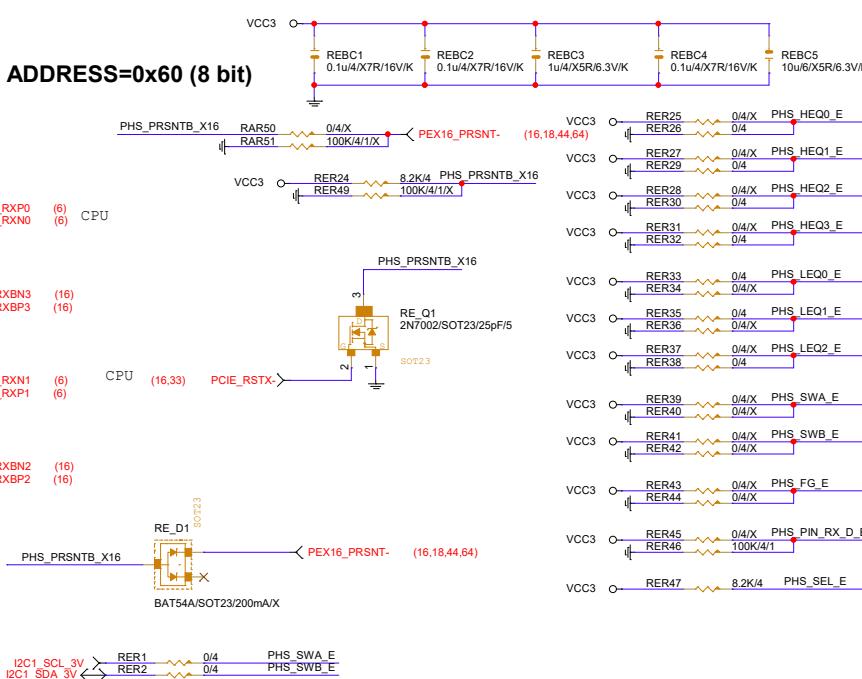
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# PCIE GEN 5 ACTITV MUX



PHS\_CLKREQ\_E RER48 0/4

ADDRESS=0x60 (8 bit)



**GIGABYTE™**

**U32G2C**

**B650E A PRO X USB4**

**Rev. 1.0**

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