



1. Description

1.1. Project

Project Name	test
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	03/23/2024

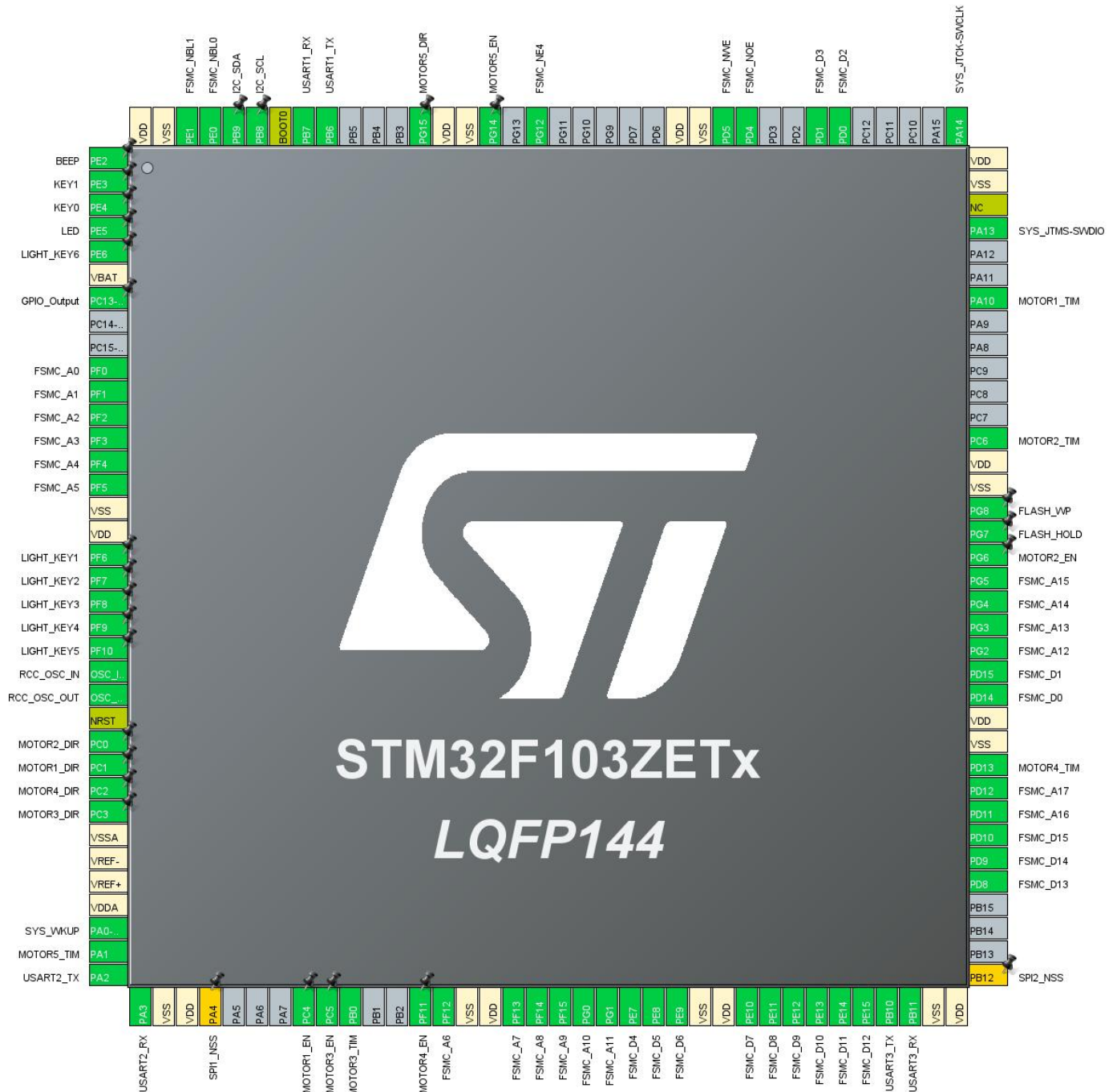
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103ZETx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M3
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2. Pinout Configuration



3. Pins Configuration

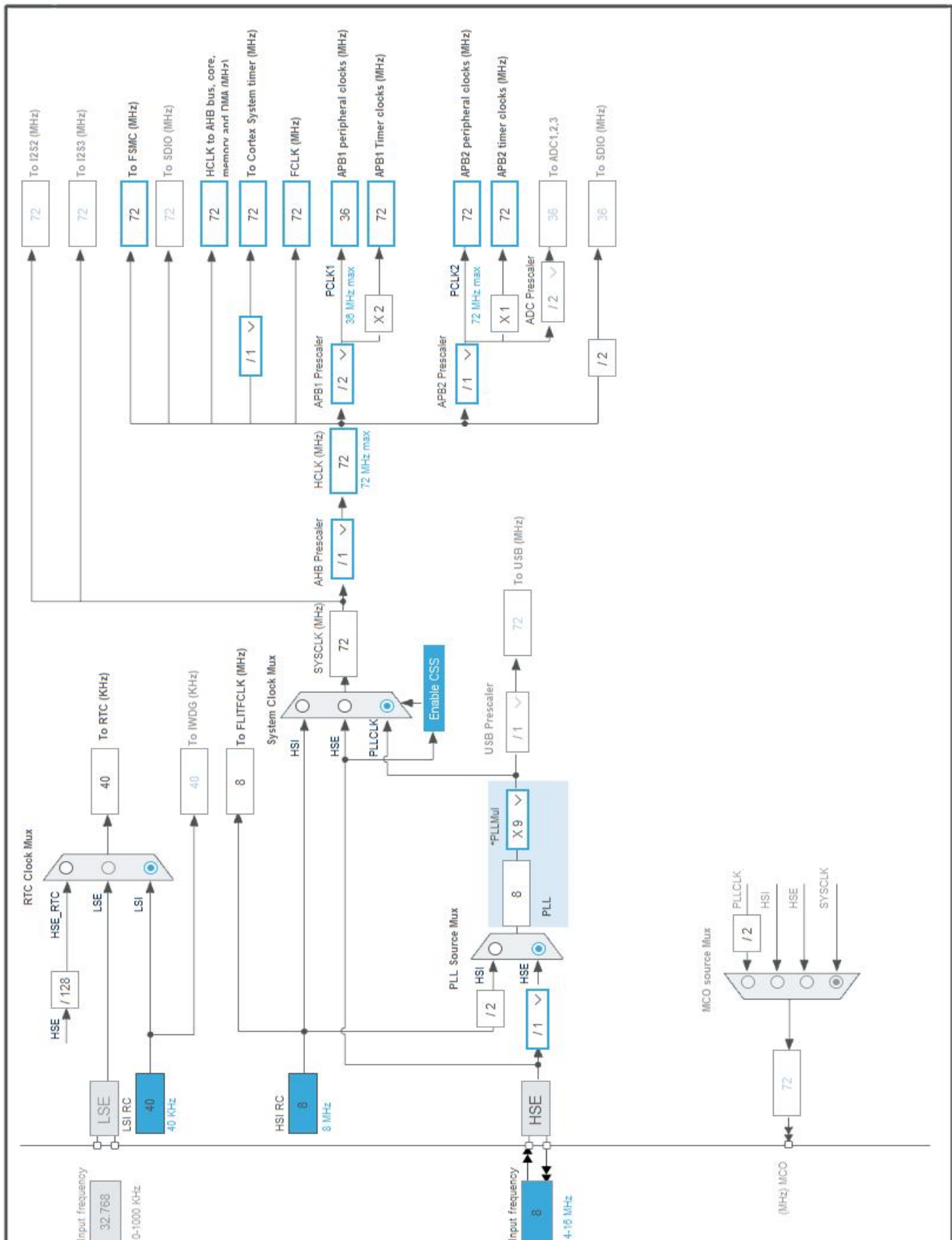
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	BEEP
2	PE3 *	I/O	GPIO_Input	KEY1
3	PE4 *	I/O	GPIO_Input	KEY0
4	PE5 *	I/O	GPIO_Output	LED
5	PE6 *	I/O	GPIO_Input	LIGHT_KEY6
6	VBAT	Power		
7	PC13-TAMPER-RTC *	I/O	GPIO_Output	
10	PF0	I/O	FSMC_A0	
11	PF1	I/O	FSMC_A1	
12	PF2	I/O	FSMC_A2	
13	PF3	I/O	FSMC_A3	
14	PF4	I/O	FSMC_A4	
15	PF5	I/O	FSMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Input	LIGHT_KEY1
19	PF7 *	I/O	GPIO_Input	LIGHT_KEY2
20	PF8 *	I/O	GPIO_Input	LIGHT_KEY3
21	PF9 *	I/O	GPIO_Input	LIGHT_KEY4
22	PF10 *	I/O	GPIO_Input	LIGHT_KEY5
23	OSC_IN	MonolO	RCC_OSC_IN	
24	OSC_OUT	MonolO	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Output	MOTOR2_DIR
27	PC1 *	I/O	GPIO_Output	MOTOR1_DIR
28	PC2 *	I/O	GPIO_Output	MOTOR4_DIR
29	PC3 *	I/O	GPIO_Output	MOTOR3_DIR
30	VSSA	Power		
31	VREF-	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	SYS_WKUP	
35	PA1	I/O	TIM2_CH2	MOTOR5_TIM
36	PA2	I/O	USART2_TX	
37	PA3	I/O	USART2_RX	
38	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	VDD	Power		
40	PA4 **	I/O	SPI1_NSS	
44	PC4 *	I/O	GPIO_Output	MOTOR1_EN
45	PC5 *	I/O	GPIO_Output	MOTOR3_EN
46	PB0	I/O	TIM3_CH3	MOTOR3_TIM
49	PF11 *	I/O	GPIO_Output	MOTOR4_EN
50	PF12	I/O	FSMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FSMC_A7	
54	PF14	I/O	FSMC_A8	
55	PF15	I/O	FSMC_A9	
56	PG0	I/O	FSMC_A10	
57	PG1	I/O	FSMC_A11	
58	PE7	I/O	FSMC_D4	
59	PE8	I/O	FSMC_D5	
60	PE9	I/O	FSMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FSMC_D7	
64	PE11	I/O	FSMC_D8	
65	PE12	I/O	FSMC_D9	
66	PE13	I/O	FSMC_D10	
67	PE14	I/O	FSMC_D11	
68	PE15	I/O	FSMC_D12	
69	PB10	I/O	USART3_TX	
70	PB11	I/O	USART3_RX	
71	VSS	Power		
72	VDD	Power		
73	PB12 **	I/O	SPI2_NSS	
77	PD8	I/O	FSMC_D13	
78	PD9	I/O	FSMC_D14	
79	PD10	I/O	FSMC_D15	
80	PD11	I/O	FSMC_A16	
81	PD12	I/O	FSMC_A17	
82	PD13	I/O	TIM4_CH2	MOTOR4_TIM
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FSMC_D0	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
86	PD15	I/O	FSMC_D1	
87	PG2	I/O	FSMC_A12	
88	PG3	I/O	FSMC_A13	
89	PG4	I/O	FSMC_A14	
90	PG5	I/O	FSMC_A15	
91	PG6 *	I/O	GPIO_Output	MOTOR2_EN
92	PG7 *	I/O	GPIO_Output	FLASH_HOLD
93	PG8 *	I/O	GPIO_Output	FLASH_WP
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	TIM8_CH1	MOTOR2_TIM
102	PA10	I/O	TIM1_CH3	MOTOR1_TIM
105	PA13	I/O	SYS_JTMS-SWDIO	
106	NC	NC		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
114	PD0	I/O	FSMC_D2	
115	PD1	I/O	FSMC_D3	
118	PD4	I/O	FSMC_NOE	
119	PD5	I/O	FSMC_NWE	
120	VSS	Power		
121	VDD	Power		
127	PG12	I/O	FSMC_NE4	
129	PG14 *	I/O	GPIO_Output	MOTOR5_EN
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Output	MOTOR5_DIR
136	PB6	I/O	USART1_TX	
137	PB7	I/O	USART1_RX	
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	I2C_SCL
140	PB9 *	I/O	GPIO_Output	I2C_SDA
141	PE0	I/O	FSMC_NBL0	
142	PE1	I/O	FSMC_NBL1	
143	VSS	Power		
144	VDD	Power		

- * The pin is affected with an I/O function
- ** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	test
Project Folder	C:\Users\Miao_kaw\Desktop\test
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.5
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_FSMC_Init	FSMC
4	MX_TIM1_Init	TIM1
5	MX_TIM2_Init	TIM2
6	MX_TIM3_Init	TIM3
7	MX_TIM4_Init	TIM4
8	MX_TIM8_Init	TIM8
9	MX_USART1_UART_Init	USART1
10	MX_USART2_UART_Init	USART2
11	MX_USART3_UART_Init	USART3

Rank	Function Name	Peripheral Instance Name
12	MX_TIM7_Init	TIM7
13	MX_RTC_Init	RTC

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103ZETx
Datasheet	DS5792_Rev12

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

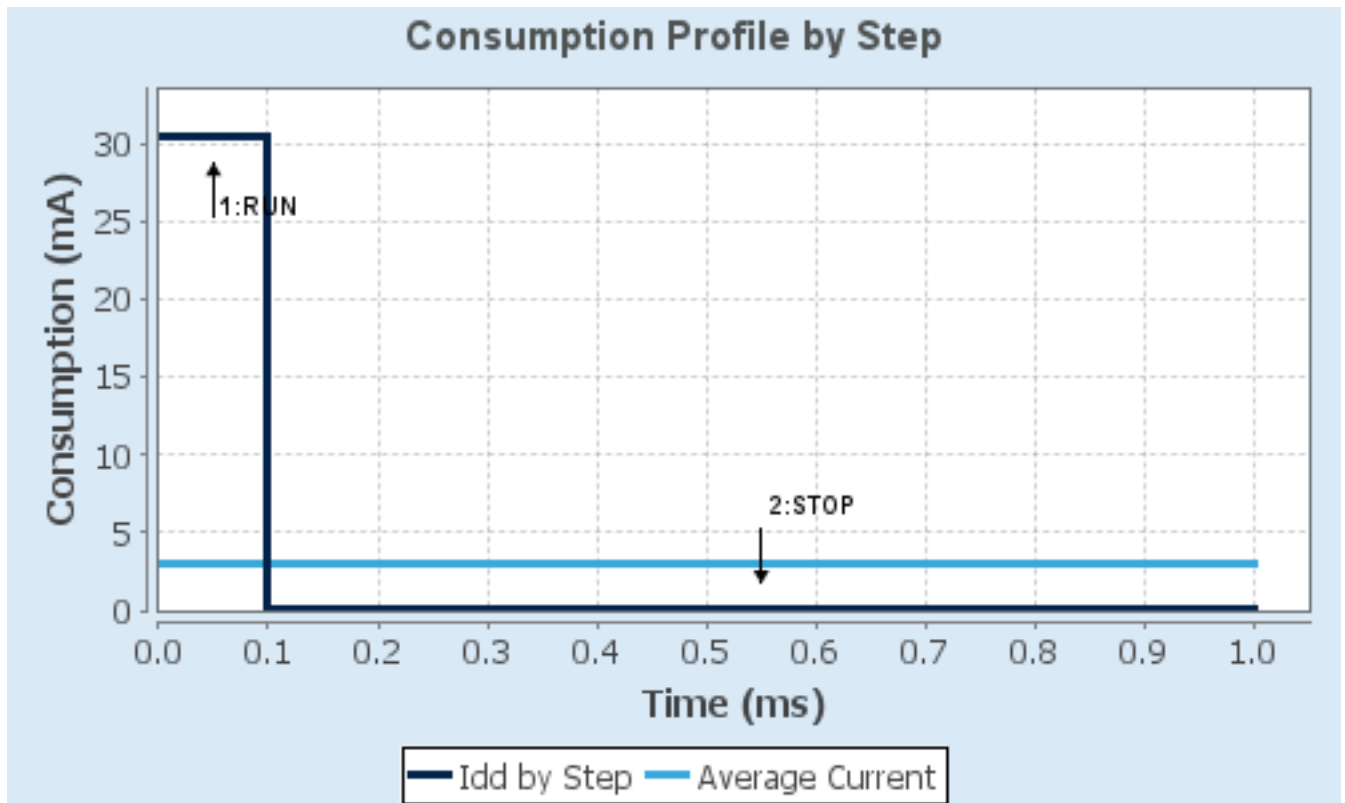
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	30.5 mA	25 μ A
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	101.98	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	3.07 mA
Battery Life	1 month, 15 days, 15 hours	Average DMIPS	61.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. FSMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE4

Memory type: SRAM

Address: 18 bits

Data: 16 bits

Byte enable: set

2.1.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 4
Write operation	Enabled *
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	0x0 *
Data setup time in HCLK clock cycles	0x3 *
Bus turn around time in HCLK clock cycles	0x0 *

2.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

2.3. RTC

mode: Activate Clock Source

mode: Activate Calendar

RTC OUT: No RTC Output

2.3.1. Parameter Settings:

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0

General:

Auto Predivider Calculation	Enabled
Asynchronous Predivider value	Automatic Predivider Calculation Enabled
Output	No output on the TAMPER pin

Calendar Date:

Week Day	Saturday *
Month	March *
Date	23 *
Year	0

2.4. SYS

Debug: Serial Wire

mode: System Wake-Up

Timebase Source: SysTick

2.5. TIM1

Channel3: Output Compare CH3

2.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	PSC *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	ARR *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 3:

Mode	Toggle on match *
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CH Idle State	Reset

2.6. TIM2

Channel2: Output Compare CH2

2.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	PSC *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	ARR *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare Channel 2:

Mode	Toggle on match *
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

2.7. TIM3

Channel3: Output Compare CH3

2.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	PSC *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	ARR *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare Channel 3:

Mode	Toggle on match *
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

2.8. TIM4

Channel2: Output Compare CH2

2.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	PSC *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	ARR *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare Channel 2:

Mode	Toggle on match *
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

2.9. TIM7

mode: Activated

2.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	USMART_PSC *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	USMART_ARR *
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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2.10. TIM8

Channel1: Output Compare CH1

2.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	PSC *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	ARR *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 1:

Mode	Toggle on match *
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CH Idle State	Reset

2.11. USART1

Mode: Asynchronous

2.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

2.12. USART2

Mode: Asynchronous

2.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

2.13. USART3

Mode: Asynchronous

2.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* **User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FSMC	PF0	FSMC_A0	Alternate Function Push Pull	n/a	High	
	PF1	FSMC_A1	Alternate Function Push Pull	n/a	High	
	PF2	FSMC_A2	Alternate Function Push Pull	n/a	High	
	PF3	FSMC_A3	Alternate Function Push Pull	n/a	High	
	PF4	FSMC_A4	Alternate Function Push Pull	n/a	High	
	PF5	FSMC_A5	Alternate Function Push Pull	n/a	High	
	PF12	FSMC_A6	Alternate Function Push Pull	n/a	High	
	PF13	FSMC_A7	Alternate Function Push Pull	n/a	High	
	PF14	FSMC_A8	Alternate Function Push Pull	n/a	High	
	PF15	FSMC_A9	Alternate Function Push Pull	n/a	High	
	PG0	FSMC_A10	Alternate Function Push Pull	n/a	High	
	PG1	FSMC_A11	Alternate Function Push Pull	n/a	High	
	PE7	FSMC_D4	Alternate Function Push Pull	n/a	High	
	PE8	FSMC_D5	Alternate Function Push Pull	n/a	High	
	PE9	FSMC_D6	Alternate Function Push Pull	n/a	High	
	PE10	FSMC_D7	Alternate Function Push Pull	n/a	High	
	PE11	FSMC_D8	Alternate Function Push Pull	n/a	High	
	PE12	FSMC_D9	Alternate Function Push Pull	n/a	High	
	PE13	FSMC_D10	Alternate Function Push Pull	n/a	High	
	PE14	FSMC_D11	Alternate Function Push Pull	n/a	High	
	PE15	FSMC_D12	Alternate Function Push Pull	n/a	High	
	PD8	FSMC_D13	Alternate Function Push Pull	n/a	High	
	PD9	FSMC_D14	Alternate Function Push Pull	n/a	High	
	PD10	FSMC_D15	Alternate Function Push Pull	n/a	High	
	PD11	FSMC_A16	Alternate Function Push Pull	n/a	High	
	PD12	FSMC_A17	Alternate Function Push Pull	n/a	High	
	PD14	FSMC_D0	Alternate Function Push Pull	n/a	High	
	PD15	FSMC_D1	Alternate Function Push Pull	n/a	High	
	PG2	FSMC_A12	Alternate Function Push Pull	n/a	High	
	PG3	FSMC_A13	Alternate Function Push Pull	n/a	High	
	PG4	FSMC_A14	Alternate Function Push Pull	n/a	High	
	PG5	FSMC_A15	Alternate Function Push Pull	n/a	High	
	PD0	FSMC_D2	Alternate Function Push Pull	n/a	High	
	PD1	FSMC_D3	Alternate Function Push Pull	n/a	High	
	PD4	FSMC_NOE	Alternate Function Push Pull	n/a	High	
	PD5	FSMC_NWE	Alternate Function Push Pull	n/a	High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG12	FSMC_NE4	Alternate Function Push Pull	n/a	High	
	PE0	FSMC_NBL0	Alternate Function Push Pull	n/a	High	
	PE1	FSMC_NBL1	Alternate Function Push Pull	n/a	High	
RCC	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA0-WKUP	SYS_WKUP	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	High *	MOTOR1_TIM
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	n/a	Low	MOTOR5_TIM
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	n/a	High *	MOTOR3_TIM
TIM4	PD13	TIM4_CH2	Alternate Function Push Pull	n/a	High *	MOTOR4_TIM
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	n/a	High *	MOTOR2_TIM
USART1	PB6	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PB7	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	High *	
	PA3	USART2_RX	Input mode	No pull-up and no pull-down	n/a	
USART3	PB10	USART3_TX	Alternate Function Push Pull	n/a	High *	
	PB11	USART3_RX	Input mode	No pull-up and no pull-down	n/a	
Single Mapped Signals	PA4	SPI1_NSS	Alternate Function Push Pull	n/a	High *	
	PB12	SPI2_NSS	Alternate Function Push Pull	n/a	High *	
GPIO	PE2	GPIO_Output	Output Push Pull	Pull-down *	Low	BEEP
	PE3	GPIO_Input	Input mode	Pull-down *	n/a	KEY1
	PE4	GPIO_Input	Input mode	Pull-down *	n/a	KEY0
	PE5	GPIO_Output	Output Push Pull	Pull-up *	Low	LED
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LIGHT_KEY6
	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LIGHT_KEY1
	PF7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LIGHT_KEY2
	PF8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LIGHT_KEY3
	PF9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LIGHT_KEY4
	PF10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LIGHT_KEY5
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR2_DIR
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR1_DIR

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR4_DIR
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR3_DIR
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR1_EN
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR3_EN
	PF11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR4_EN
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR2_EN
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FLASH_HOLD
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FLASH_WP
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR5_EN
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR5_DIR
	PB8	GPIO_Output	Output Push Pull	Pull-up *	High *	I2C_SCL
	PB9	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	High *	I2C_SDA

3.2. DMA configuration

nothing configured in DMA service

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD interrupt through EXTI line 16	unused		
RTC global interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 break interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupts	unused		
TIM8 capture compare interrupt	unused		
TIM7 global interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware					
System Core	Analog	Timers	Connectivity	Multimedia	Computing
DMA		RTC ✓	FSMC ✓		
GPIO ⚠		TIM1 ✓	USART1 ✓		
NVIC ✓		TIM2 ✓	USART2 ✓		
RCC ✓		TIM3 ✓	USART3 ✓		
SYS ✓		TIM4 ✓			
		TIM7 ✓			
		TIM8 ✓			

5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f1_bsd1.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f1_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
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Flyers	https://www.st.com/resource/en/flyer/fldpstpfc11120.pdf
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Device Option Lists	https://www.st.com/resource/en/device_option_list/opl_stm32f103_512k.zip
Errata Sheets	https://www.st.com/resource/en/errata_sheet/es0340-stm32f101xcde-stm32f103xcde-device-errata-stmicroelectronics.pdf
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Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn0516-overview-of-the-stm32f0xf100xxf103xx-and-stm32f2xxf30xf4xx-mcus-pmsm-singledual-foc-sdk-v40-stmicroelectronics.pdf
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