

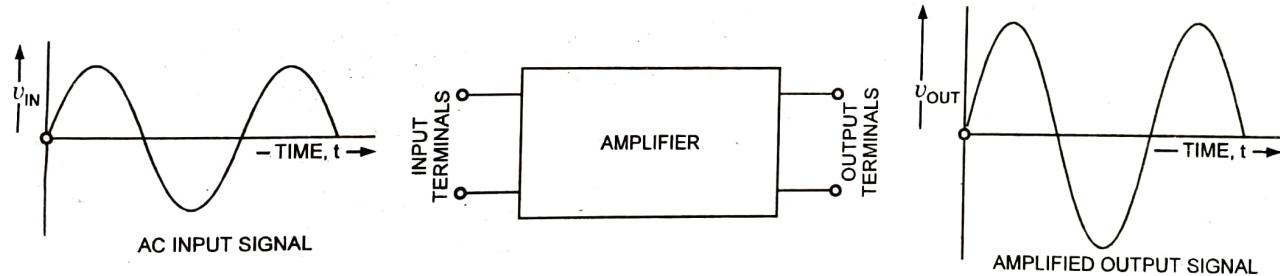
## 8.16. COMPARISON OF CHARACTERISTICS OF TRANSISTORS IN DIFFERENT CONFIGURATIONS

The essential characteristics of each of basic configurations are tabulated follows:

<i>Configuration Characteristics</i>	<i>Common Base</i>	<i>Common Emitter</i>	<i>Common Collector</i>
Input impedance	Low (about $100 \Omega$ )	Medium (about $800 \Omega$ )	Very high (about $750 \text{ k}\Omega$ )
Output impedance	Very high (about $500 \text{ k}\Omega$ )	High (about $50 \text{ k}\Omega$ )	Low (about $50 \Omega$ )
Current gain	Less than unity but usually more than 0.9 (about 0.98)	High (about 80)	High (about 100)
Voltage gain	About 150	About 500	Less than unity
Leakage current	Very small ( $5 \mu\text{A}$ for Ge and $1 \mu\text{A}$ for Si)	Very large ( $500 \mu\text{A}$ for Ge and $20 \mu\text{A}$ for Si)	Very large
Signal phase	In phase with input	Reverse	In phase with input
Applications	For high frequency applications	For AF applications	For impedance matching

## 8.17. TRANSISTOR AS AN AMPLIFIER

The main utility of a transistor lies in its ability of amplifying weak signals. The weak signal is applied at the input terminals and the amplified output is obtained across the output terminals, as illustrated in fig. 8.26.



*Block Diagram of An Amplifier*

*Fig. 8.26*

A transistor alone cannot perform the function of amplification and some passive components such as resistors and capacitors and a biasing battery is to be connected. Common emitter (CE) configuration, because of its high current, voltage and power gains, is much suited for most of the amplifier circuits. A common emitter N-P-N transistor amplifier circuit is given in fig. 8.27.

The weak signal is applied between emitter-base junction and output is taken across a load resistor  $R_L$  connected in series with collector supply voltage  $V_{CC}$  (fig. 8.27). In order to obtain faithful amplification, it is necessary that the input circuit remains always forward biased regardless the polarity of the ac input signal. So a battery  $V_{BB}$  is inserted in the circuit with the polarity indicated in addition to the signal voltage. This dc voltage is called the *bias voltage* and its magnitude is such as to keep the input circuit

always forward biased regardless the polarity of the input signal.

The input circuit being forward biased has low resistance and a small change  $\Delta V_{IN}$  in input signal voltage causes a relatively large change  $\Delta I_E$  in emitter current. This causes almost the same change in collector current because of transistor action. The collector current flowing through a high load resistance  $R_L$  develops a large voltage across it. The change in output voltage across load resistance  $R_L$  may be many times the change in input signal

voltage. Thus voltage amplification  $A = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$  will be greater than unity, and the transistor acts as an amplifier. This is further illustrated below by considering typical circuit values.

Let the load resistance  $R_L$  be of  $10\text{ k}\Omega$  and a change of  $0.1\text{ V}$  in input signal voltage cause a change  $0.5\text{ mA}$  in emitter current. This change of  $0.5\text{ mA}$  in emitter current will also change collector current  $I_C$  by approximately  $0.5\text{ mA}$ . This change of  $0.5\text{ mA}$  in collector current will produce a change of  $0.5 \times 10^{-3} \times 10 \times 10^3$  i.e.  $5\text{ V}$  in output voltage appearing across the load resistor  $R_L$  of  $10\text{ k}\Omega$ . Thus the change of  $0.1\text{ V}$  in input signal voltage causes a change of  $5\text{ V}$  in the output voltage giving a voltage amplification of  $\frac{5}{0.1} = 50$ .

**Necessity of Biasing.** For most of the applications, transistors are required to operate as *linear amplifiers* (i.e. to amplify output voltage as a linear function of the input voltage). To achieve this, it is necessary to operate the transistor over region of its characteristic curves which are linear, parallel and equi-spaced for equal increments of the parameter. Such an operation can be ensured by proper selection of zero signal operating point and limiting the operation of the transistor over the linear portion of the characteristics. For proper selection of zero signal operating point, proper biasing i.e. application of dc voltages at emitter-to-base junction and collector-to-base junction is required.

If the transistor is not biased properly, it would work inefficiently and produce distortion in the output signal.

### 8.18. TRANSISTOR LOAD LINES

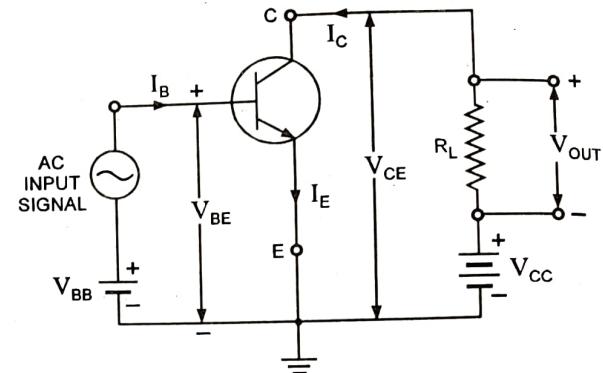
The concept of load line is very important in understanding the working of a transistor. It is defined as the locus of operating point on the output characteristic of the transistor. It is the line on which the operating point moves when ac signal is applied to the transistor.

**8.18.1. DC Load Line.** In the circuit shown in fig. 8.27  $V_{CC}$  is the supply voltage to collector,  $R_C$  (or  $R_L$ ) is the collector resistance (or load resistance) and  $V_{CE}$  is the collector-to-emitter voltage. Applying Kirchhoff's second law to the output or collector circuit we have.

$$V_{CC} = V_{CE} + I_C R_C \quad \dots(8.35)$$

$$\text{or } I_C = \frac{V_{CC} - V_{CE}}{R_C} \quad \text{or } I_C = \frac{-V_{CE}}{R_C} + \frac{V_{CC}}{R_C} \quad \dots(8.36)$$

This equation is to be plotted on the output characteristic of the transistor,  $V_{CE}$  and  $I_C$  are variables.



Common Emitter NPN Transistor  
Amplifier Circuit

Fig. 8.27

Identify this equation as  $y = mx + c$  where  $m = \frac{-1}{R_C}$  as the slope of the line and

$c = \frac{V_{CC}}{R_C}$  as intercept of the line on vertical current axis (fig. 8.28)

Consider the following two particular situations :

(i) When  $V_{CE} = 0$ ,  $I_C = \frac{V_{CC}}{R_C}$

...saturation point A

(ii) When  $I_C = 0$ ,  $V_{CE} = V_{CC}$

...cut-off point B

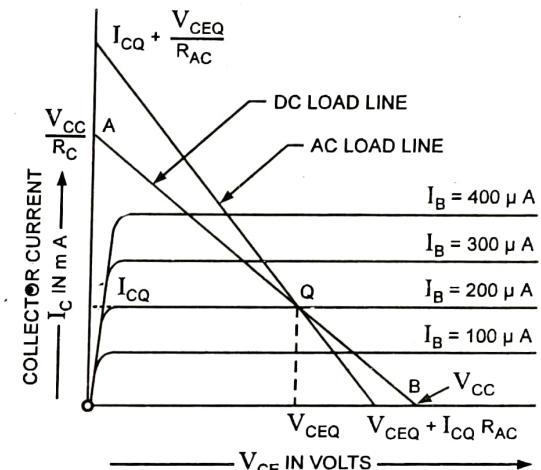
By joining these two points A and B, *dc load line* is obtained. The *dc load line* represents the dynamic characteristic of the device. The dc load line gives the values of collector current  $I_C$  and collector-emitter voltage  $V_{CE}$  corresponding to zero signal conditions.

**8.18.2. Quiescent Point.** It is a point on the dc load line which represents dc collector-emitter voltage  $V_{CE}$  and collector current  $I_C$  in the absence of ac signal. It is also called the *operating point* because the variations in  $V_{CE}$  and  $I_C$  take place about this point when signal is applied. The best position for this point is midway between

cut-off and saturation points where  $V_{CE} = \frac{1}{2} V_{CC}$ . Point Q is quiescent point marked on the output characteristics shown in fig. 8.28. Selection of the

operating point is done as per application for which the device is to be used. For example in case of a small signal amplifier, in which power is conserved, operating point is selected so as to give lowest quiescent value of  $I_C$ , while for an amplifier operated to deliver small amount of power, operating point is selected so that available quiescent current is about one-half of the maximum permissible collector current  $I_C$ .

**8.18.3. AC Load Line.** When an ac signal is applied, the transistor voltage  $V_{CE}$  and collector current  $I_C$  vary above and below the quiescent point Q. So point Q is common to both dc and ac load lines. The *ac load line* gives the values of  $V_{CE}$  and  $I_C$  when an ac signal is applied. For drawing ac load line, take a convenient collector current change  $\Delta I_C$  and compute the corresponding collector-emitter voltage change  $\Delta V_{CE} = -\Delta I_C R_C$  to obtain another point lying on the ac load line. Now the ac load can be drawn by joining this point and point Q. AC load is steeper than dc load line but the two lines intersect at the quiescent point Q determined by the biasing dc voltages and currents. AC load line takes into account the ac load resistance while the dc load line considers only the dc load resistance.



Common Emitter Transistor Output  
Characteristics and DC and AC Load Lines  
Fig. 8.28

**11.5.3. Self Bias or Emitter Bias or Potential Divider Bias Circuit.** This is the most commonly used biasing arrangement. The arrangement is shown in fig. 11.10. The name voltage divider is derived due to the fact that the voltage divider is formed by the resistors  $R_1$  and  $R_2$  across  $V_{CC}$ . The emitter resistor  $R_E$  provides stabilization. The resistor  $R_E$  causes a voltage drop in a direction so as to reverse bias the emitter junction. Since the emitter-base junction is to be forward biased, the base voltage is obtained from supply  $V_{CC}$  through  $R_1 - R_2$  network. For forward biasing the emitter-base junction  $R_1$  and  $R_2$  are so adjusted that the base terminal becomes more positive than emitter. The net forward bias across the emitter-base junction,  $V_{BE}$  is equal to  $V_B$  minus dc voltage drop across  $R_E$ . The dc bias circuit is independent of transistor current gain factor  $\beta$ . In case of amplifiers, to avoid the loss of ac signal (because of feedback caused by  $R_E$ ) a capacitor of large capacitance is connected across  $R_E$ . The capacitor offers a very small reactance to the ac signal and so it passes through the capacitor.

**Circuit Analysis.** Assume that the current flowing through resistance  $R_1$  is  $I_1$ . As base current  $I_B$  is very small so current flowing through resistance  $R_2$  can be also assumed to be equal to  $I_1$

$$\text{and } I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$\text{Voltage across resistance } R_2, V_B = \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

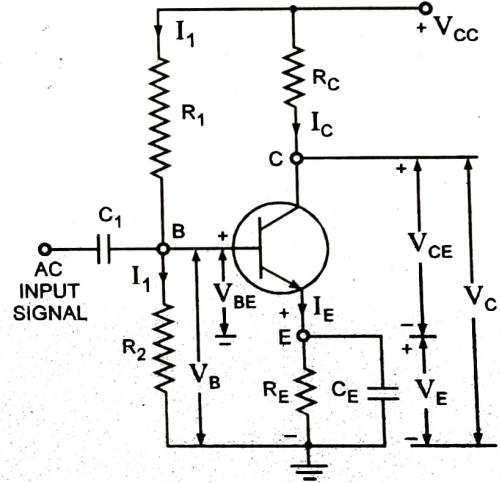
Applying Kirchhoff's second (or voltage) law to the base circuit (fig. 11.10) we have

$$V_B = V_{BE} + V_E = V_{BE} + I_E R_E \quad \text{or} \quad I_E = \frac{V_B - V_{BE}}{R_E}$$

$$\text{and collector current, } I_C \approx I_E \approx \frac{V_B - V_{BE}}{R_E} \quad \dots(11.15)$$

Applying Kirchhoff's second (or voltage) law to the collector side we have

$$\begin{aligned} V_{CC} &= I_C R_C + V_{CE} + I_E R_E = I_C R_C + V_{CE} + I_C R_E \quad \text{since } I_C \approx I_E \\ &= V_{CE} + I_C (R_C + R_E) \end{aligned}$$



Self Bias Circuit

Fig. 11.10

$$\text{or } V_{CE} = V_{CC} - I_C (R_C + R_E) \quad \dots(11.16)$$

From equations (11.15) and (11.16) the values of  $I_C$  and  $V_{CE}$  can be determined and the quiescent point Q is established.

It is clear from equation (11.15) that  $I_C$  does not at all depend upon  $\beta$ . Though collector current  $I_C$  depends upon  $V_{BE}$  but in practice  $V_{BE}$  is very small in comparison to  $V_B$  and so collector current  $I_C$  is practically independent of  $V_{BE}$ . Thus collector current  $I_C$  in this biasing circuit is almost independent of transistor parameters and hence good stabilisation is ensured.

In this biasing circuit the emitter resistance  $R_E$  provides excellent stabilisation. This is explained as below :

Now let the temperature of transistor junction rise when it is loaded. This causes increase in leakage currents and so increase in the value of  $\beta$ . Hence collector current  $I_C$  tends to increase. With the increase in the value of  $I_C$ , voltage drop across emitter resistance  $R_E$  increases. Since voltage drop across  $R_2$  (i.e.  $V_B$ ) is independent of collector current, therefore  $V_{BE}$  decreases and so  $I_B$ ,  $I_E$  and  $I_C$ .

Thus we see that the circuit has tendency to hold the Q point ( $I_C$ ) stable automatically. This is due to feedback action. The increase in  $I_C$  has immediately a reaction change of feedback so as to correct the situation.

Stabilising Factor  $S_f$ : The junction to the left of the base terminal is replaced by its

### 1.12.1 R-C Coupled Amplifier

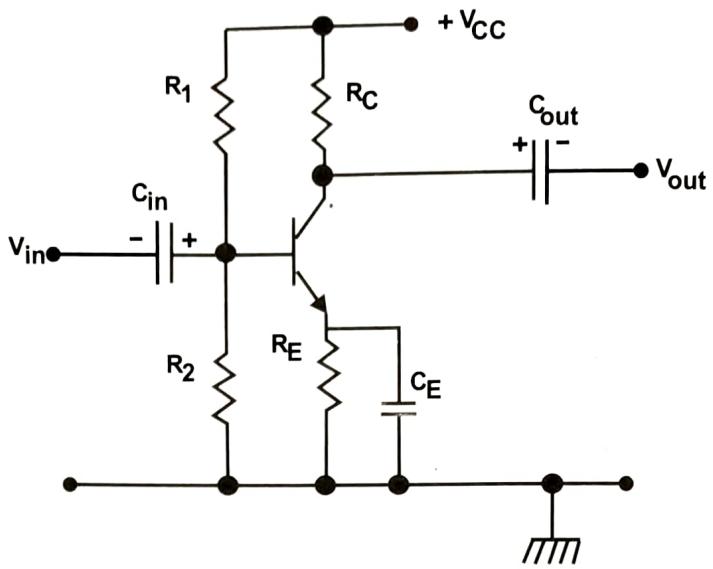


Fig: R-C Coupled Amplifier

#### Circuit description

The figure shows the single stage common emitter R-C Coupled amplifier circuit. Here both forward bias voltage at emitter-base junction and reverse bias voltage at the collector-emitter junction are derived from the single supply voltage  $V_{CC}$ .

The magnitude of these bias voltages are adjusted to operate the transistor in active region. In this arrangement base is the input terminal and collector is the output terminal. The resistors  $R_1$ ,  $R_2$  and  $R_E$  form the biasing network. In multistage amplifiers coupling from one stage to next stage is obtained by a coupling capacitor followed by a connection to a shunt resistor, therefore such amplifiers are called **Resistance-Capacitance coupled** or **R-C Coupled amplifiers**. The input capacitor  $C_{in}$  couples a.c signal voltage to base of the transistor. In the absence of  $C_{in}$  the signal source will be in parallel with resistor  $R_2$  and the bias will be affected. Thus the function of  $C_{in}$  is to allow only the alternating current from the signal source to flow into the input circuit. The emitter bypass capacitor  $C_E$ , offers low reactance path to the signal. If it is not present, then the voltage drop across  $R_E$  will reduce the effective voltage available across the base-emitter terminals (the input voltage) and thus reduces the gain. The coupling capacitor  $C_{out}$  transmits a.c signal but blocks the d.c voltage of the first stage from reaching the base of the second stage in the case of multistage amplifiers. Thus the d.c biasing of the next stage is not interfered with. For this reason, the coupling capacitor  $C_{out}$  is also called the blocking capacitor.

## Working

When an input signal is applied in the emitter-base junction, the signal is superimposed in the d.c voltage at emitter-base junction. Therefore during the positive half-cycle of the input signal the forward bias across the junction increases, because it is already positive with respect to ground. This increase in forward bias increases the base current  $I_B$ . Due to increase in base current the collector current also increases. In CE configuration the corresponding increase in collector current will be ' $\beta$ ' times the increase in  $I_B$ . This increase in collector current produces more voltage drop across the output terminal. During negative half-cycle of the input signal the forward bias across emitter junction will be decreased and decreases base current. This decrease in base current results in corresponding ( $\beta$ -times) decrease in collector current. Consequently the drop across output terminals will be decreased. It is clear that the collector current varies according to the input signal applied and variation is  $\beta$ -times to that of input current variation. Due to this action an amplified form of input signal can be obtained at the output terminal.

In common emitter amplifier the input and output voltages are of 180 degree out of phase, even though the input and output currents are in phase. It means that when the input voltage increases in positive direction the output voltage increases in negative direction and vice versa. When the input signal increases in the positive half cycle it increases the forward bias on emitter junction, which in turn increase the base current and results in increase of collector current. Hence the drop across  $R_C$  increases.  $V_{CC}$  is kept constant. The output of the circuit is taken from collector and emitter and is given by the equation,  $V_{CE} = V_{CC} - I_C R_C$ . This indicates that as the signal voltage increases in the positive half cycle, the output voltage increases in negative direction.

## Frequency Response and Bandwidth

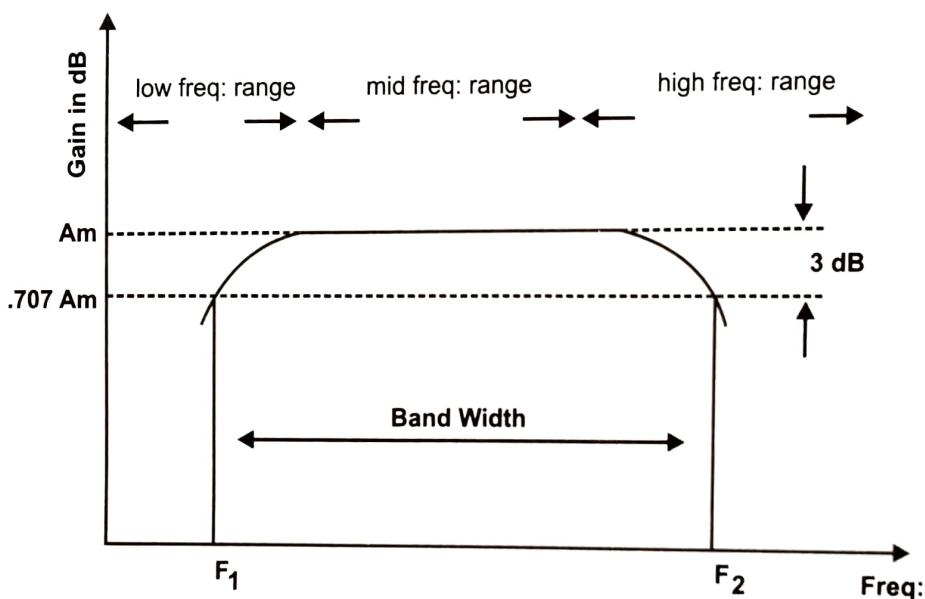
An important characterization of an amplifier is in terms of its response to input sinusoids of different frequencies. Such characterization of amplifier performance is known as **frequency response** of the amplifier. The ratio of the amplitude of the output sinusoid ( $V_o$ ) to the amplitude of the input sinusoid ( $V_i$ ) is the magnitude of the amplifier gain at frequency,  $f$ .

$$|A_V(f)| = \frac{V_o}{V_i} \quad \text{and} \quad \angle A_V(f) = \phi$$

The values of  $|A_V|$  and  $\phi A_V$  are measured with different frequencies of the input sinusoid and the gain magnitude and phase angle are plotted with frequency. These two plots together constitute the frequency response of the amplifier ; the first is known as amplitude response and second is known as phase response. The voltage gain in decibel(dB) may be expressed as

$$\text{Voltage Gain in } dB = 20 \log_{10} \frac{V_o}{V_i}$$

The frequency response curve of a typical R-C Coupled amplifier is shown in figure. At *lower frequencies* (below 50Hz) higher capacitive



**Fig: Frequency Response of an RC Coupled Amplifier**

reactance of coupling capacitor allows very small part of signal to pass from one stage to next and also because of higher reactance of emitter bypass capacitor  $C_E$ , the emitter resistor  $R_E$  is not shunted. Thus the voltage gain falls off at low frequencies.

In the *mid frequency range* (50Hz -20KHz), the voltage gain of the amplifier is constant. With increase in frequency in this range, the reactance of the coupling capacitor reduces thereby increasing the gain but at the same time lower capacitive reactance causes higher loading resulting in lower voltage gain. Thus the two effect cancel each other and uniform gain is obtained in mid frequency range.

At *high frequencies* (exceeding 20 KHz), gain of amplifier decreases with increase in frequency. At high frequencies, the reactance of cou-

pling capacitor become very small and it behaves as a short-circuit. This increases the loading of the next stage and reduces the voltage gain. The other factor responsible for the reduction in gain at higher frequencies is the presence of inter electrode capacitance  $C_{bc}$  between base and collector. It connects the output with the input. Because of this, negative feedback takes place in the circuit and the gain decreases. This feedback effect is more, when  $C_{bc}$  provides a path for higher frequency ac currents.

In the figure,  $A_m$  is the maximum gain of the amplifier and  $f_1, f_2$  are lower and upper cut-off frequencies respectively. The difference between *upper cut-off frequency* ( $f_2$ ) and *lower cut-off frequency* ( $f_1$ ) is called the **Bandwidth (BW)**.

$$\text{Bandwidth} = f_2 - f_1$$

At these frequencies, the output voltage is  $\frac{1}{\sqrt{2}}$  times the maximum voltage. Since the power is proportional to the square of the voltage, the output power at these cut-off frequencies become one half of the power at mid-frequencies. On dB scale this is equal to a reduction in power by 3dB. For this reason these frequencies are called **3 dB frequencies** and corresponding gain is called **3 dB gain or mid band gain**.

### **Advantages of R-C Coupled Amplifier**

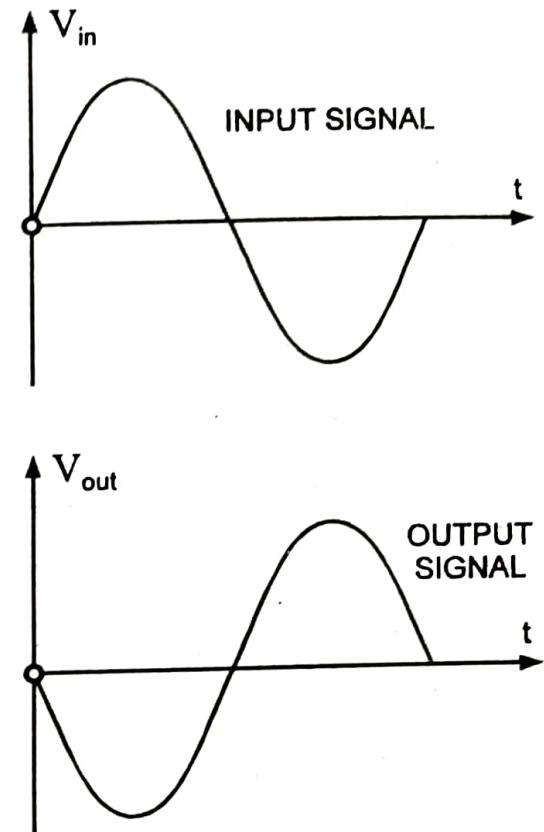
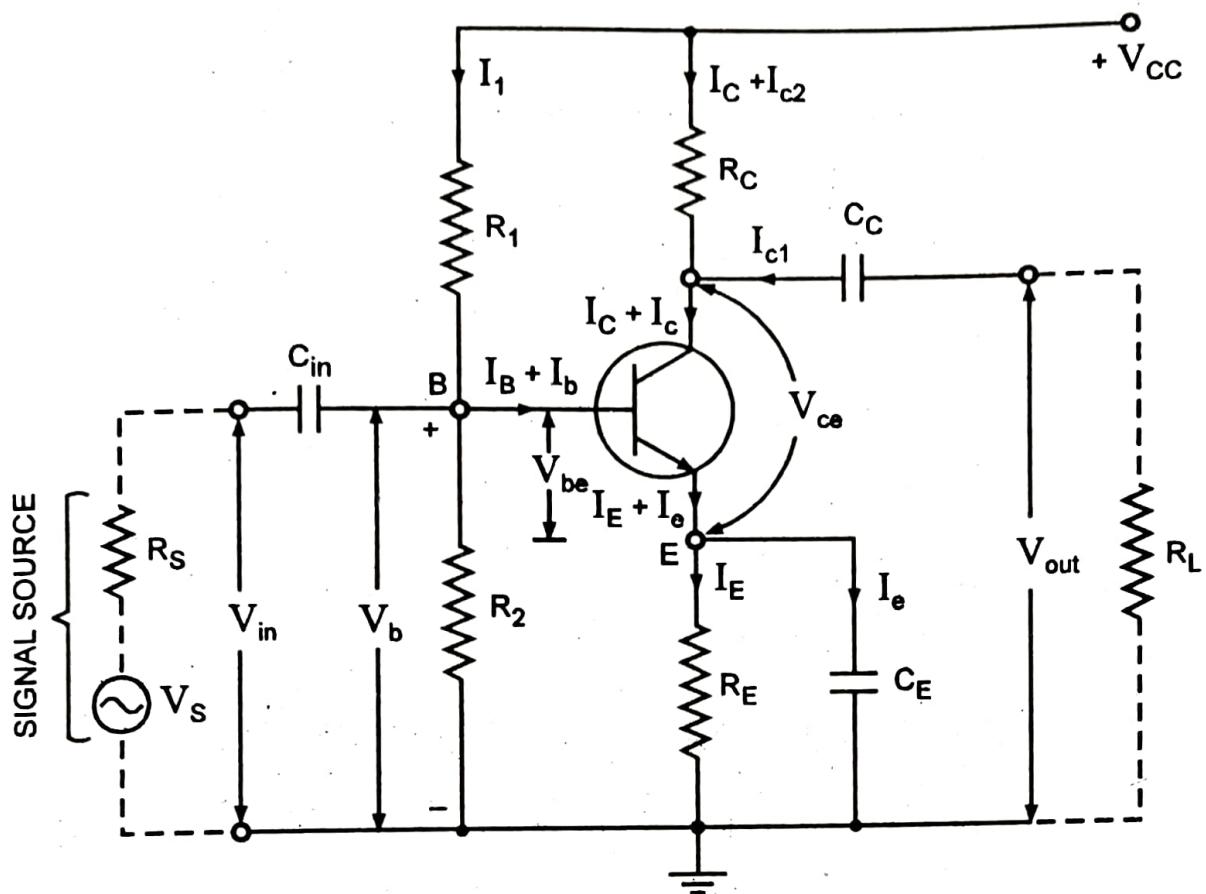
- Excellent frequency response.
- Cheaper in cost.
- Very compact circuit.

### **Disadvantages of R-C Coupled Amplifier**

- Low voltage and power gain.
- Tendency of becoming noisy with age.
- Poor impedance matching.

### **Applications**

Widely used as **voltage amplifiers** because of their excellent audio-fidelity over a wide range of frequency.



*Common Emitter Transistor Amplifier Circuit With Self Biasing*  
*Fig. 12.30*