# 18CSS201J_ADE_CT 2_Set A_CSEQ1

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Q.No 1 to 25 (25*1=25)

Each Question Carry 1 Mark

The AND gate in data flow modeling is represented as

- ○ C<=A and B
- ○ C = A and B
- ○ C = A * B
- ○ C<=A * B

In FPGA, the vertical and horizontal direction directions are separated by _____

- ○ A line
- ◉ A channel
- ○ A strobe
- ○ A flip-flop

Clear selection

Propagation delay is important because

- (●) the logic gates must be given a short break during each clock cycle or else they will overheat
- ( ) it limits the maximum operating frequency of a gate
- ( ) it is a measure of how long the clock must be applied to the gate before it will make the required decision
- ( ) all the gates in a system must have the same propagation times in order to be compatible

Clear selection

Under which modelling the functionality of the logic system and basic blocks are described?

- ( ) Behavioral
- ( ) Structural
- (●) Dataflow
- ( ) Component

Clear selection

Consider the following statements in respect of ECL gate:

1. Its switching speed is high
2. It provide OR and NOR logic operations
3. Its power dissipation is small as compared to other logic gates
4. Its logic levels are compatible with other logic family gates

- (●) 1 & 2
- ( ) 1,2 & 3
- ( ) 1,2 & 4
- ( ) 3 & 4

Clear selection

_____of a logic circuit is determined by the time between the application of input and change in the output of the circuit?

- (●) Speed
- ( ) Fan-in
- ( ) Power dissipation
- ( ) Fan-out

Clear selection

The minimum number of transistors can be used by 2 input AND gate is

- ( ) 3
- (●) 2
- ( ) 4
- ( ) 5

Clear selection

If the device with short propagation delay has

- ○ Low speed
- ○ Medium speed
- ◉ High speed
- ○ No change speed

Clear selection

Which of the following is not the subfamilies of TTL

- ○ Standard TTL
- ○ Low power TTL
- ◉ Low speed TTL
- ○ Fast TTL

Clear selection

Match list I (Type of gates) with list II (Values of propagation delay) and select the corresponding answer:

| List-I | List-II |
|---|---|
| A. ECL | 1. 5ns |
| B. TTL | 2. 20ns |
| C. CMOS | 3. 100ns |
| D. NMOS | 4. 1 ns |

- ○ A = 1; B = 4; C= 3; D= 2
- ○ A = 4; B = 1; C= 3; D= 2
- ○ A = 1; B = 4; C= 2; D= 3
- ◉ A = 4; B = 1; C= 2; D= 3

Clear selection

_____ determines the number of inputs the logic gate can handle ?

- ○ Fan-out
- ◉ Fan-in
- ○ Power
- ○ Frequency

Clear selection

In RTL NOR gate, the output is at logic 1 only when all the inputs are at

- ○ +5v
- ○ Logic 1
- ◉ Logic 0
- ○ +10v

Clear selection

The main disadvantage of TTL with totem pole output is

- ○ High power dissipation
- ○ Low fan out
- ◉ Wire operation is not allowed
- ○ Low noise margin

Clear selection

Which of the following logic families has the least propagation delay?

- ○ RTL
- ○ DTL
- ○ CMOS
- ◉ I^2L [ I square L]

Clear selection

Why CMOS logic families is most preferred in large scale integrated circuits ?

- ○ Low noise immunity
- ○ Less power dissipation
- ◉ High noise immunity and less static power dissipation
- ○ Less static power dissipation

Clear selection

The structure of PMOS logic can be obtained by replacing NMOS transistors in the CMOS Circuit by _____ ?

- ○ A charged capacitor
- ○ A low resistance
- ◉ A pull down resistance
- ○ Using both a capacitor and a resistor

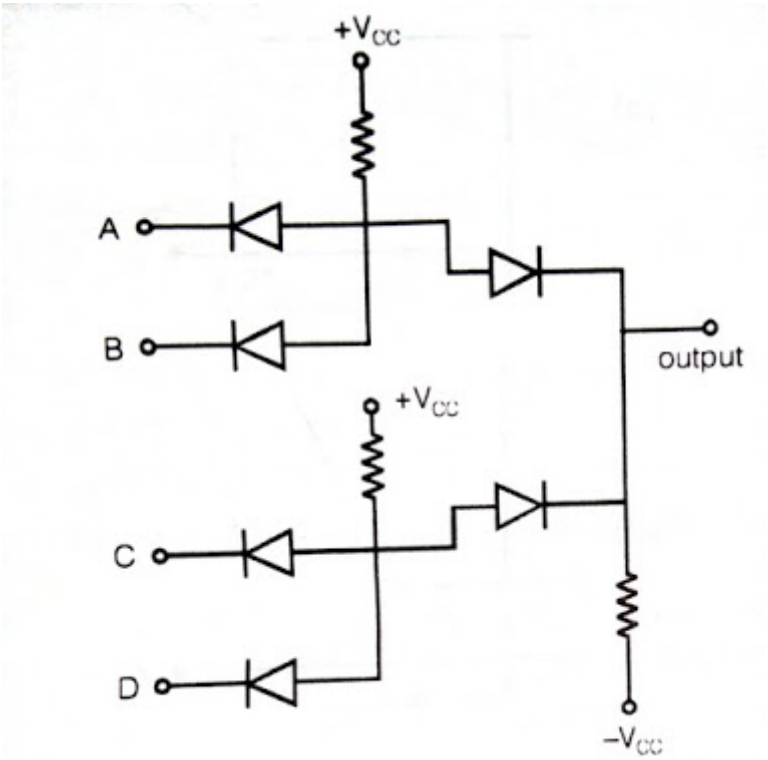
Clear selection

When o/p changes from low to high, the o/p transistor of the gate goes from

- ○ Unsaturation to cut – off
- ○ Saturation to cut – off
- ◉ Cut – off to saturation
- ○ Cut – off to unsaturation

Clear selection

What is the output of the gate circuit shown in below figure?




- (A+B) (C+D)
- AB+CD
- (AB+CD)'
- ((A+B) (C+D))'

Clear selection

How many types of output configurations are there in TTL

- 1 type
- 2 types
- 3 types
- 4 types

Clear selection

A package in VHDL consists of _____

- ○ Commonly used architectures
- ○ Commonly used tools
- ◉ Commonly used data types and subroutines
- ○ Commonly used syntax and variables

Clear selection

CMOS inverter has _____ input resistance and _____ output impedance

- ○ high, high
- ○ low, high
- ◉ high, low
- ○ low, low

Clear selection

Which of the following is an advantage of Il L?

- ○ External resistance required for proper functioning
- ○ Lower packaging density than n-MOS
- ○ Lower noise margin
- ○ Low power dissipation

In Structural modelling the Ports are also known as _____ to the component.

- ○ Structure
- ○ Behavior
- ○ Function
- ○ Interface

The disadvantage of RTL is that

- ○ High noise creation
- ○ It uses a maximum number of registers
- ○ It uses a minimum number of registers
- ◉ It results in high power dissipation

Clear selection

The third state of Tri-state buffer mainly known as?

- ○ High-resistance
- ○ Low-Impedance
- ○ Low-Resistance
- ◉ High-Impedance

Clear selection

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