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EXPERIMENT 12

MUX AND ALU

Aim:- To implement Multiplexer Higher Order Multiplexer using Lower Order Multiplexer and ALU using 8:1 Multiplexer.

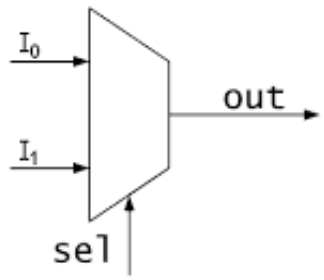
Definition:-

1) Multiplexer-A Multiplexer is a device that allows one of several analog or digital input signals which are to be selected and transmits the input that is selected into a single medium. Multiplexer is also known as Data Selector. A multiplexer of 2n inputs has n select lines that will be used to select input line to send to the output. Multiplexer is abbreviated as Mux

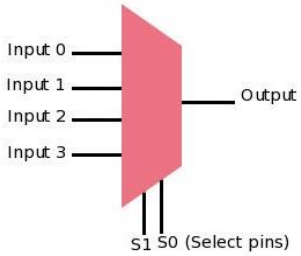
2) ALU-An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU).

Block Diagram:-

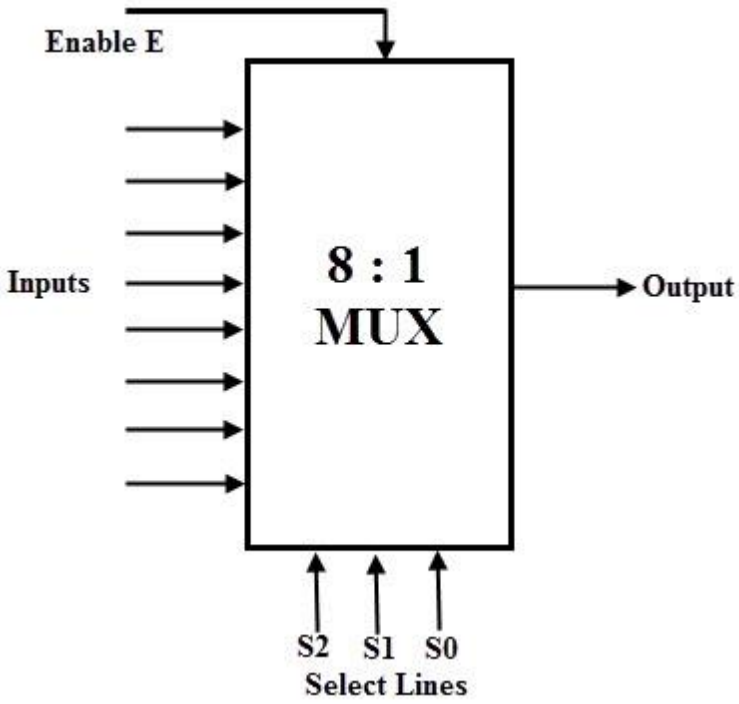
1) 2:1 MUX



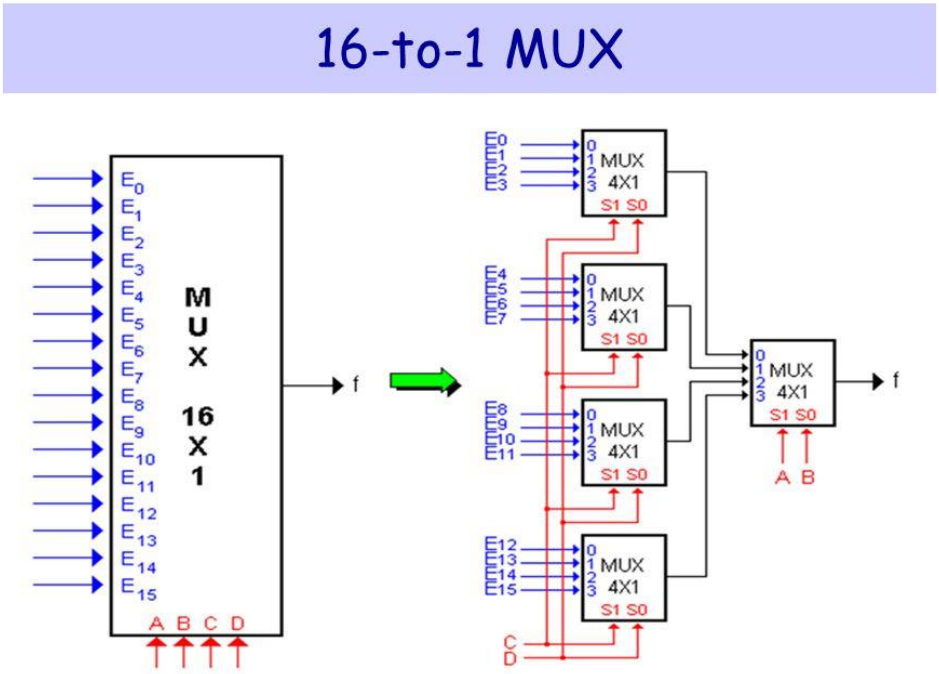
2) 4:1 MUX



3) 8:1 MUX



4) 16:1 MUX



Truth Table:-

1) 2:1 MUX

Truth Table

x	f
0	1
1	0

2) 4:1 MUX

Truth Table

S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

3) 8:1 MUX

Select Data Inputs			Output
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

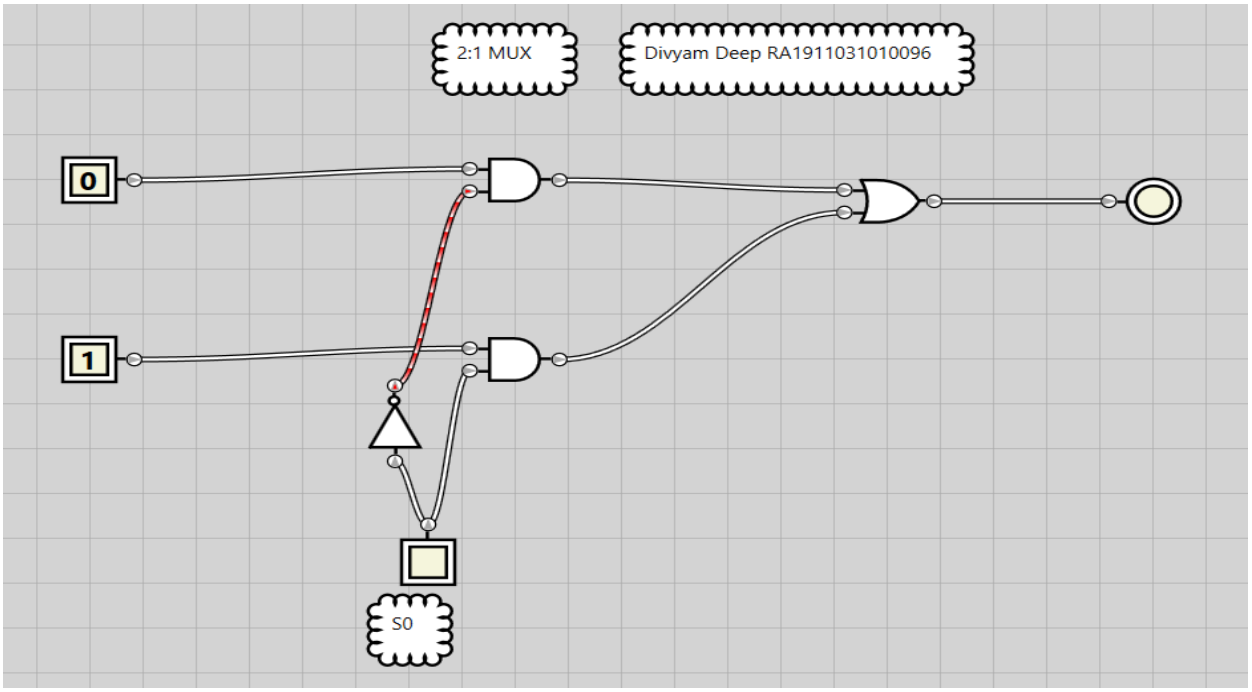
4) 16:1 MUX

TRUTH TABLE

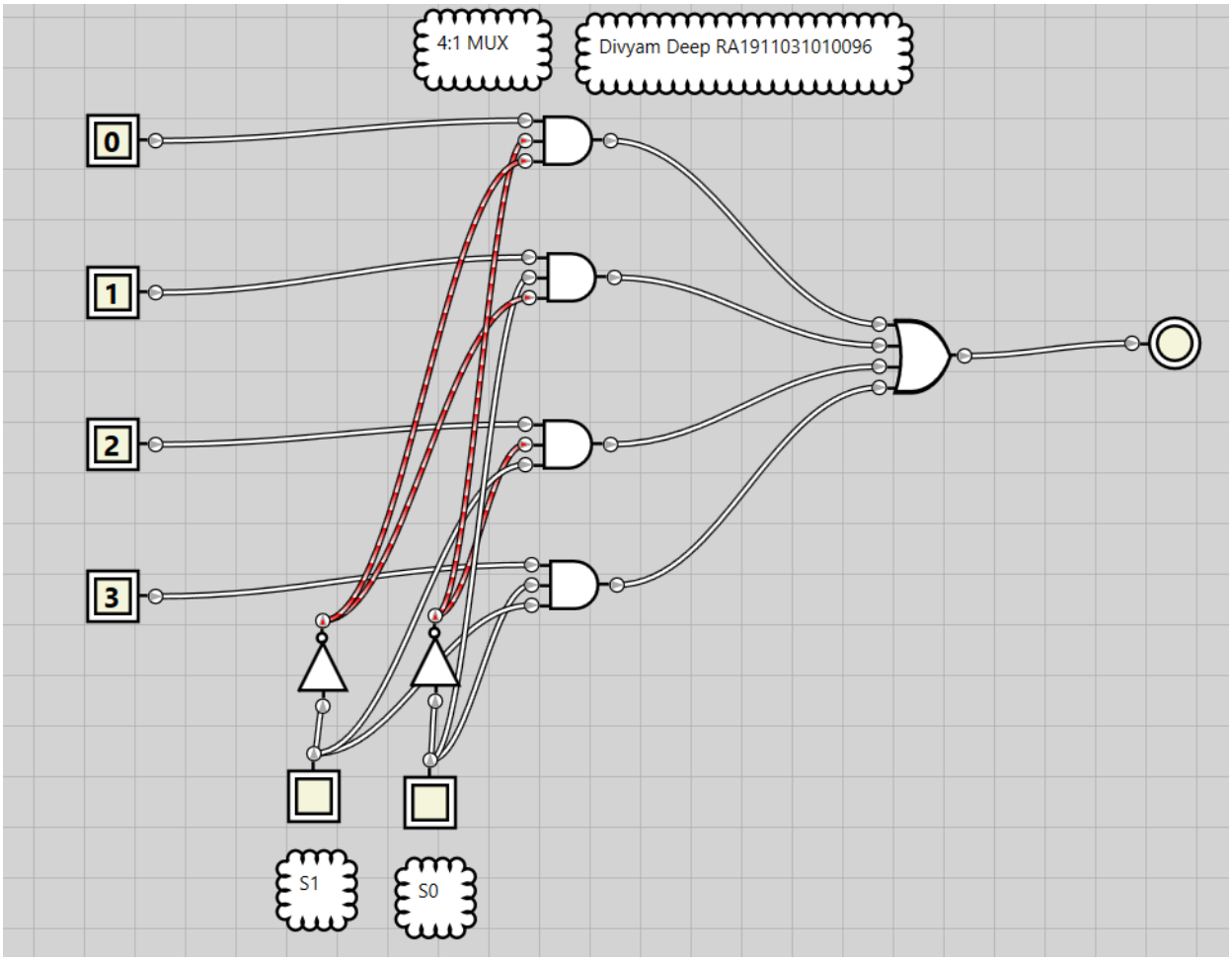
S0	S1	S2	S3	$\overline{E}$	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

Snapshot:-

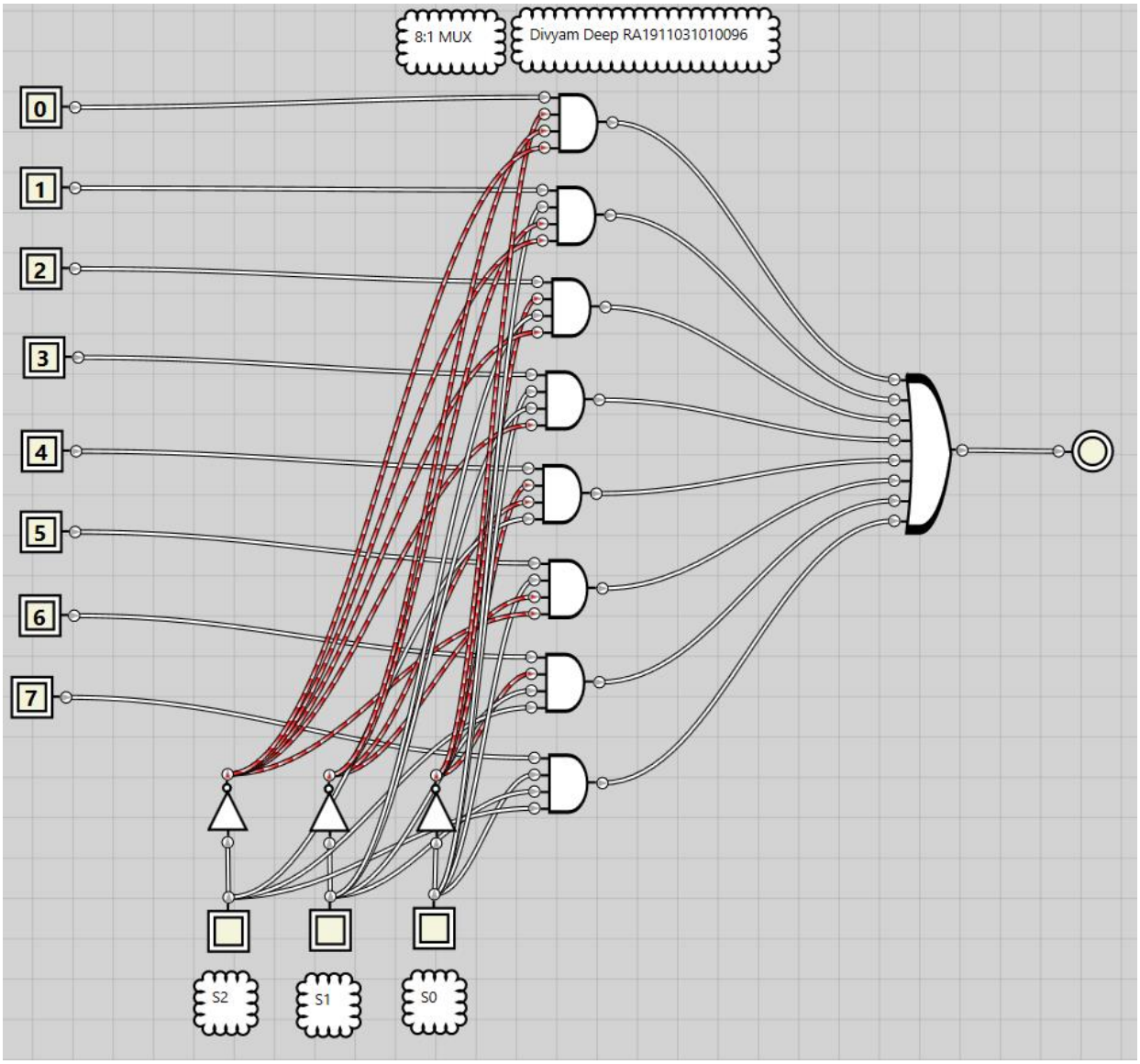
1) 2:1 MUX



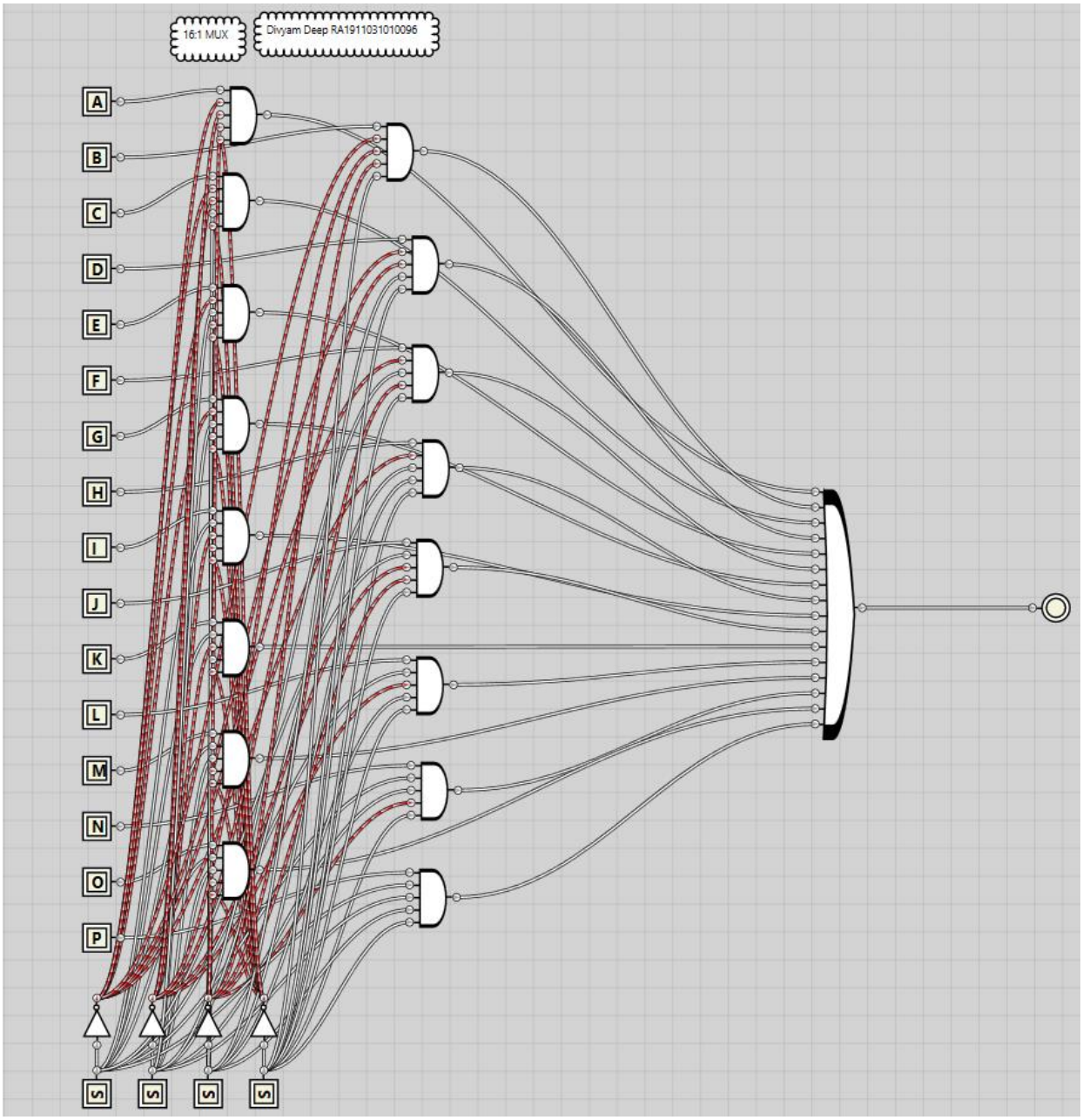
2) 4:1 MUX



3) 8:1 MUX

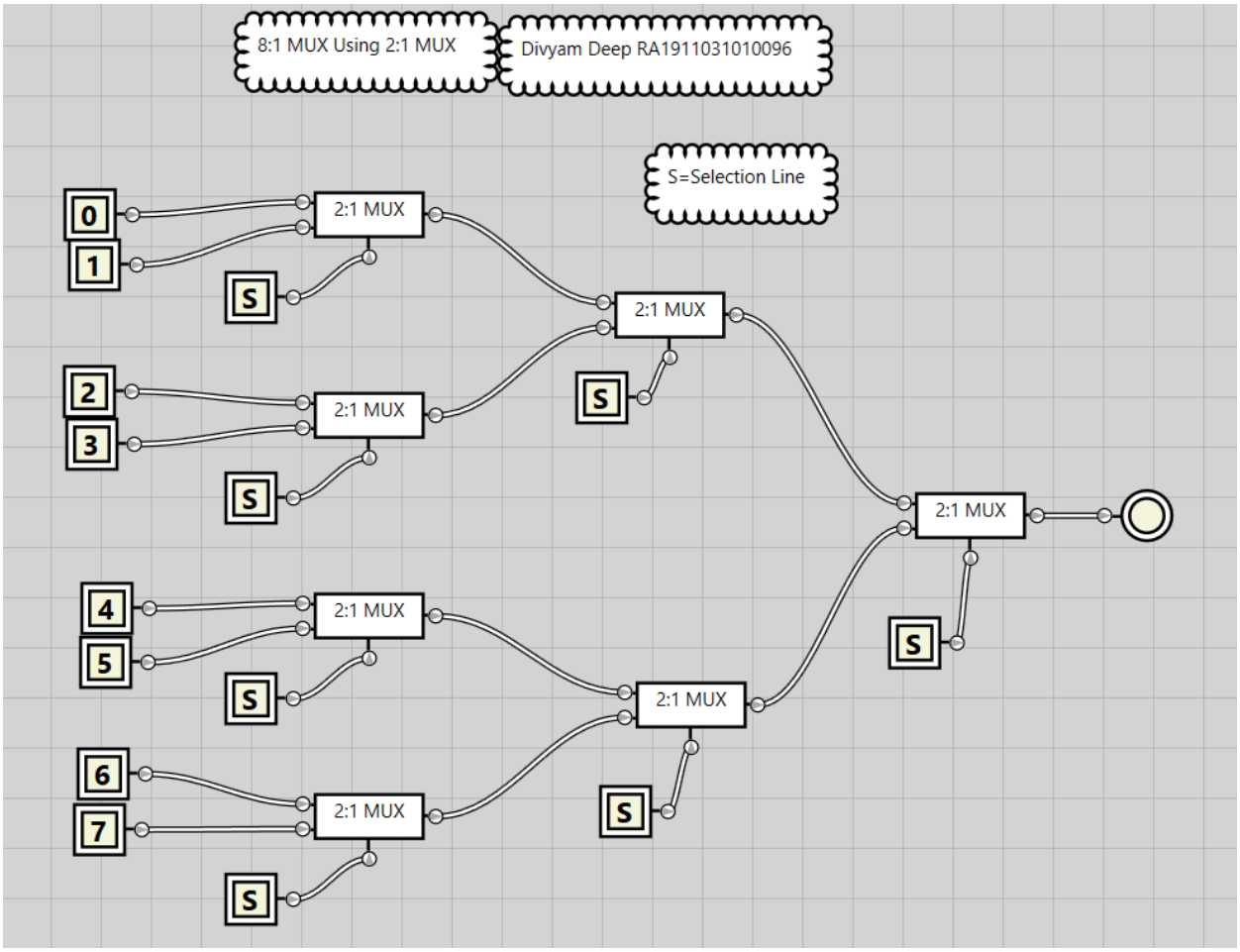


4) 16:1 MUX

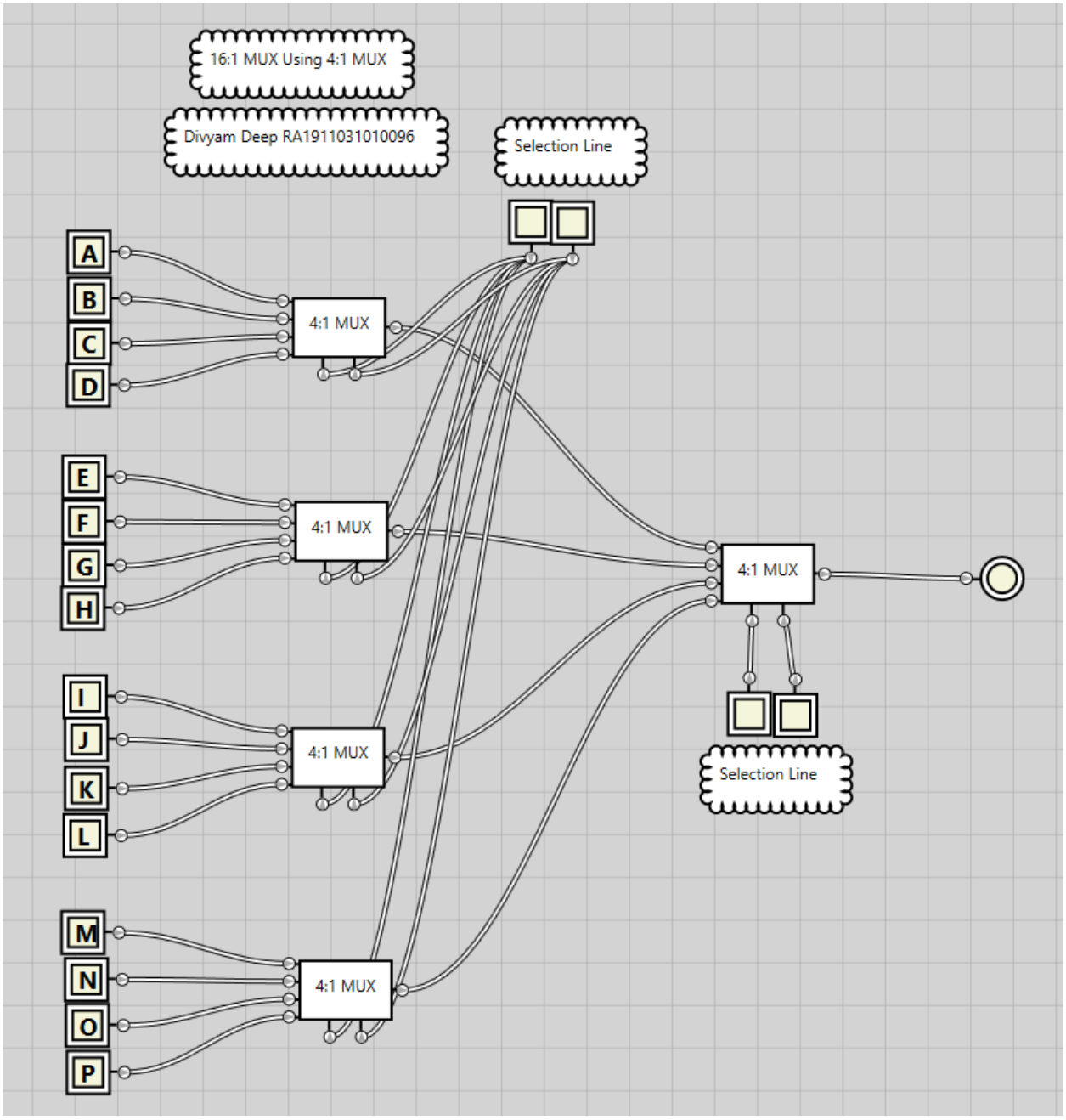

16:1 MUX
Divyam Deep RA1911031010096
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
S
S
S
S

Snapshot of Higher Order MUX Using Lower Order:-

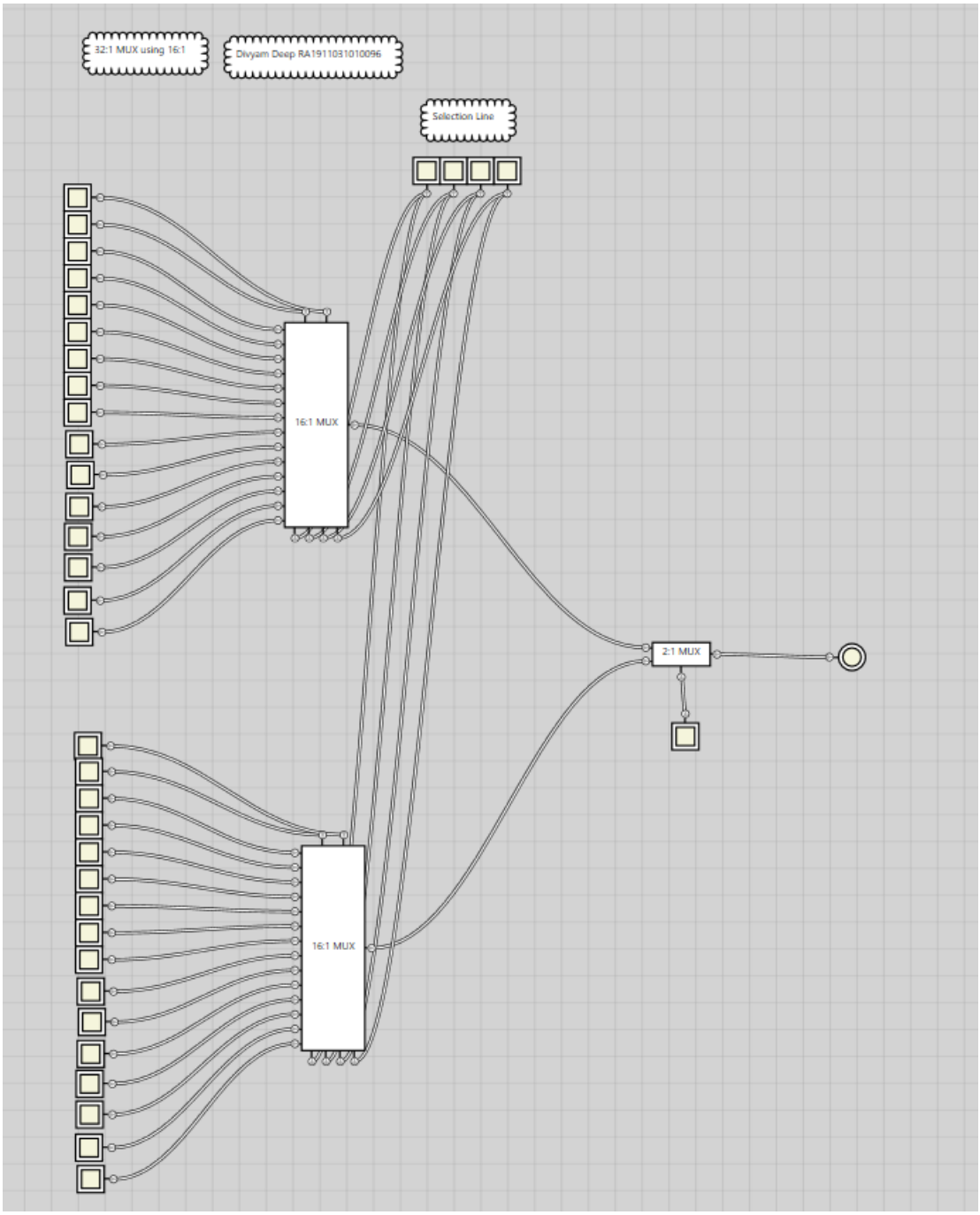
1) 8:1 MUX using 2:1 MUX



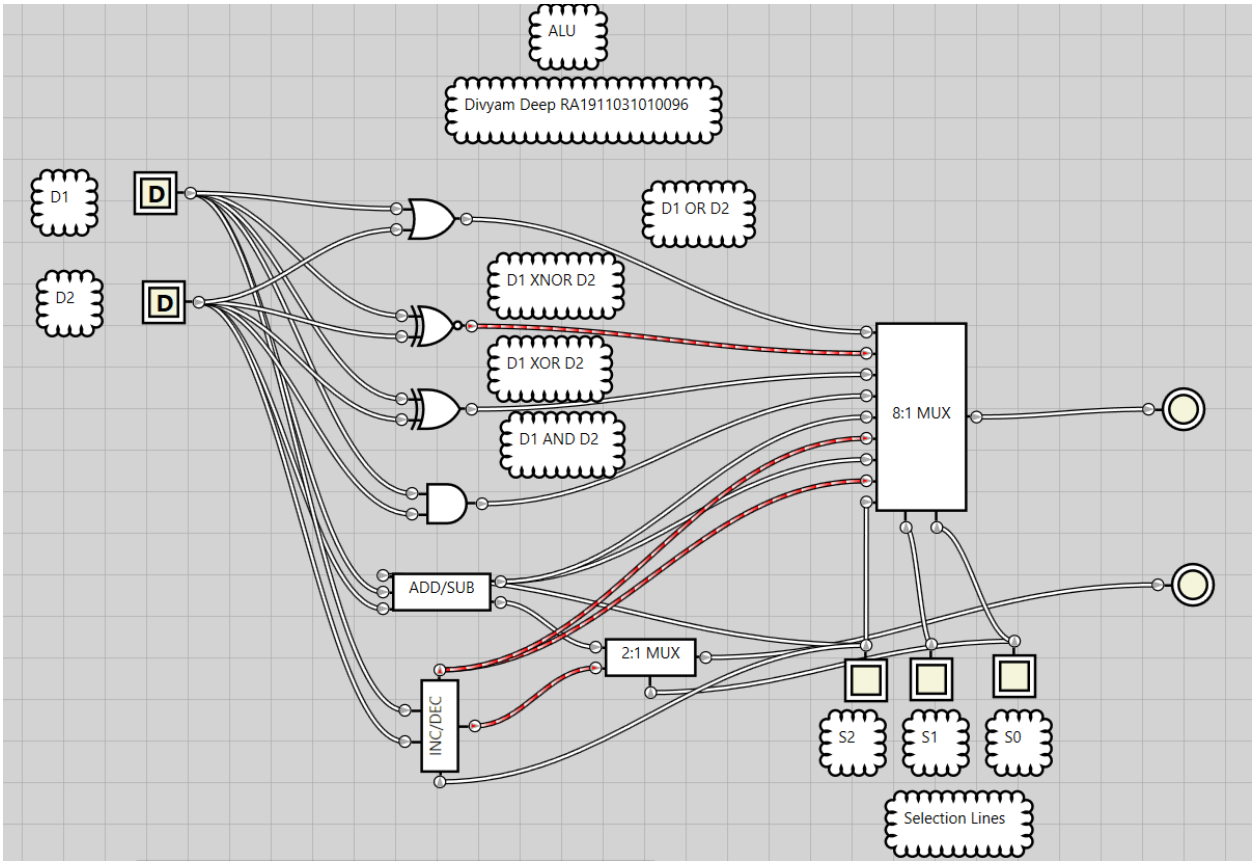
2) 16:1 MUX Using 4:1 MUX



3) 32:1 MUX Using 16:1 MUX



Snapshot of ALU:-



Result:-

Hence Multiplexer Higher Order Multiplexer using Lower Order Multiplexer and ALU using 8:1 Multiplexer is successfully implemented.