hw5(共27分)

5.37(3分)

PC, PCMUX, MAR, Memory, MDR, GateMDR, IR, SEXT unit connected to IR[8:0], ADDR2MUX set to [8:0]SEXT , ADDR1MUX set to PC, along with the ADDER they connect to, MARMUX, GateMARMU, RegFiles, ALU, GateALU.

3 分，全对或者与答案相差不大（只要器件能覆盖 dataflow 的整体流向）给满，否则酌情扣分。如果有其他用不上的元件需要扣分。

5.39(3分)　　LEA不会设置CC！！！！！！

PC, PCMUX, (MAR, Memory, MDR)(这些是取指令的时候需要用到的), IR, SEXT unit connected to IR[8:0], ADDR2MUX set to [8:0]SEXT , ADDR1MUX set to PC, along with the ADDER they connect to, MARMUX, GateMARMU, RegFiles.

同上

6.24(3分)

x6041

0110 000 001 000001

3分，源寄存器，目的寄存器，偏移量，各一分

7.32 (10分)

Symbol table: 每一行一分，多写一个或少些一个扣一分

LABEL	ADDRES
SKIP	8009
A	800A
B	8011
BANNER	8012
C	801F

x8006: 0010 001 000000011

x8007: 0000 010 000000001

x8008: 0011 000 000001000

每行一分，共3分

The contents of line 7, which is a ST instruction, will store value 5 in location B when the program is running. However, the content of line 10, which is a pseudo-ops will cause location B contain the value 5 during assembly process.

意思对即可，2分

7.34(8分)

```
(a) NOT R2, R0
(b) ADD R2, R2, #1
(c) BRz DONE
(d) ADD R0,R0, #1
```

每问两分，有其他合理答案也可给分。

选做题

5.58

a.

LD.PC	LD.MAR	LD.MDR	LD.CC	LD.TEMP	GatedPC	GatedMDR	GatedALU	SR1MUX	ALUMUX	ALUK	MIO.EN	R.W
0	1	0	0	0	0	0	1	01	0	11	-	0
0	0	1	0	0	0	0	0	-	-	-	0	0
0	0	0	0	1	0	1	0	-	-	-	-	0
0	0	0	1	0	0	0	1	-	1	00	-	0
0	0	0	0	0	0	0	0	-	-	-	-	0

b.

```
if(Reg3==mem[Reg2]):
    mem[Reg2]=Reg1
```

6.26

a. 从左到右，从上到下顺序，依次为：

```
30, xA202, GateMDR=1 LD.IR=1, 10, LD.MAR=1 GateMARMUX=1 MARMUX=ADDER ADDR2MUX=
[8:0]SEXT ADDR1MUX=PC, 26, GateMDR=1 LD.MAR=1,27
```

b. LDI, R1, #2

c. x3010

d. 2 cycles

e.

location	content

location	content
x3010	xA202
x3013	x4567
x4567	x0000