hw2

共配置29‘

2.40

(a) 2 (1')

(b) -17 (1')

(c) Positive infinity(1')

(d) -3.125(1')

2.48

(a) x100 (1')

(b) x6F (1')

(c) x75BCD15 (1')

(d) xD4(1')

3.6

A	B	C	D	Z
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

(共2' 有一处错误扣一分)

Z = (C or D)’ = (A’ or B’)’ = A and B　(2' 过程一分 结果一分)

3.20

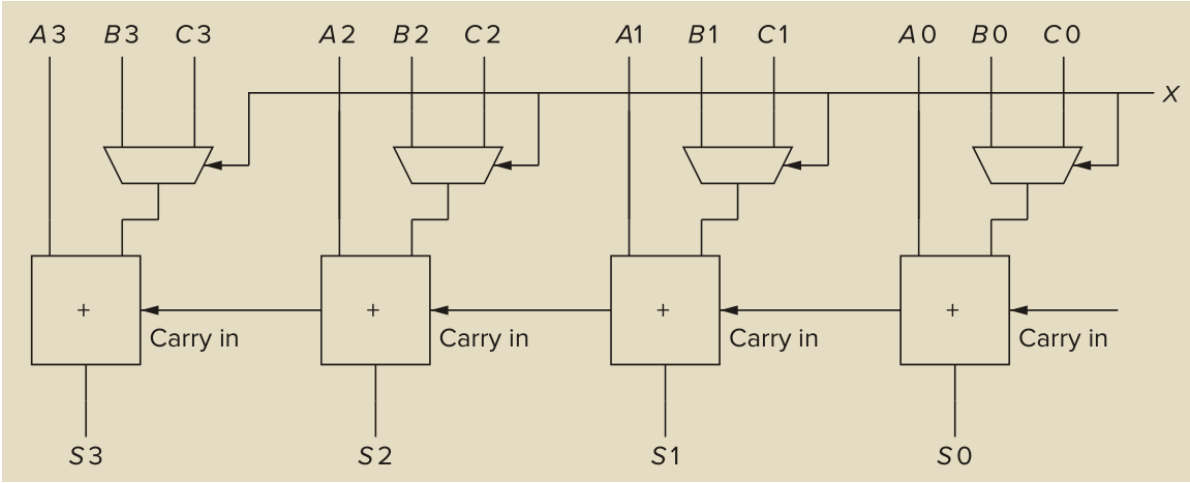
1(1')

4(1')

3.30

（a）X=0 => S = A+B, X=1 => S = A+C　(1')

（b）Circuit diagram is same as following Figure with the following modifications: C = NOT (B), Carry-in = X　(2' 两个修改各一分)

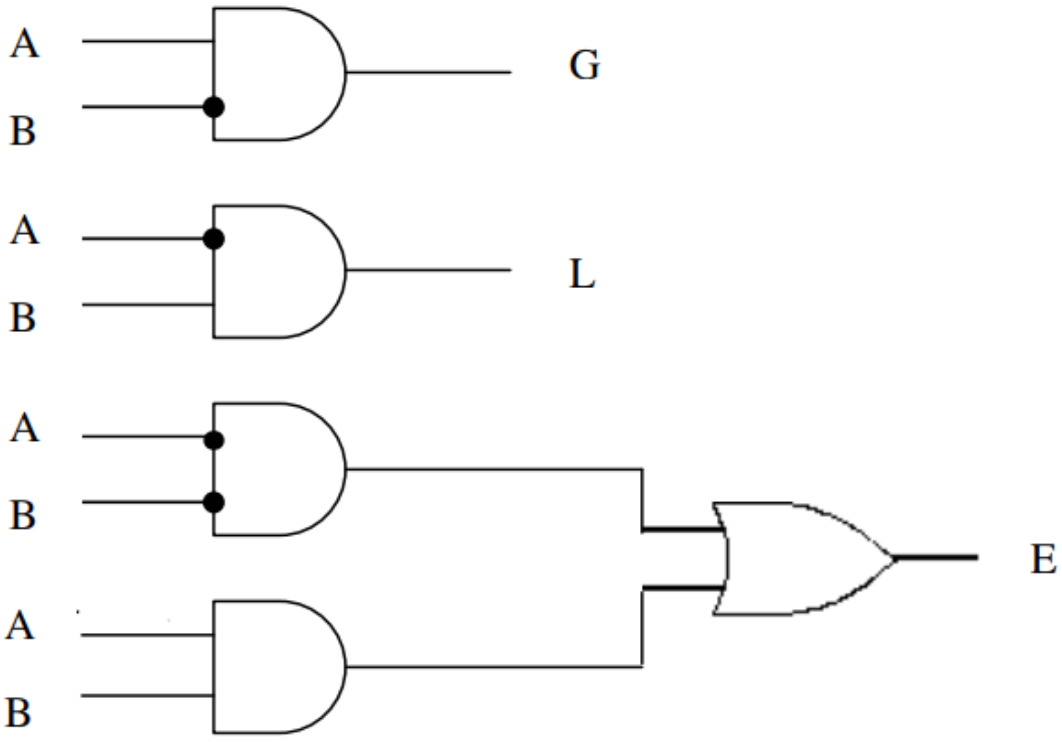


3.36

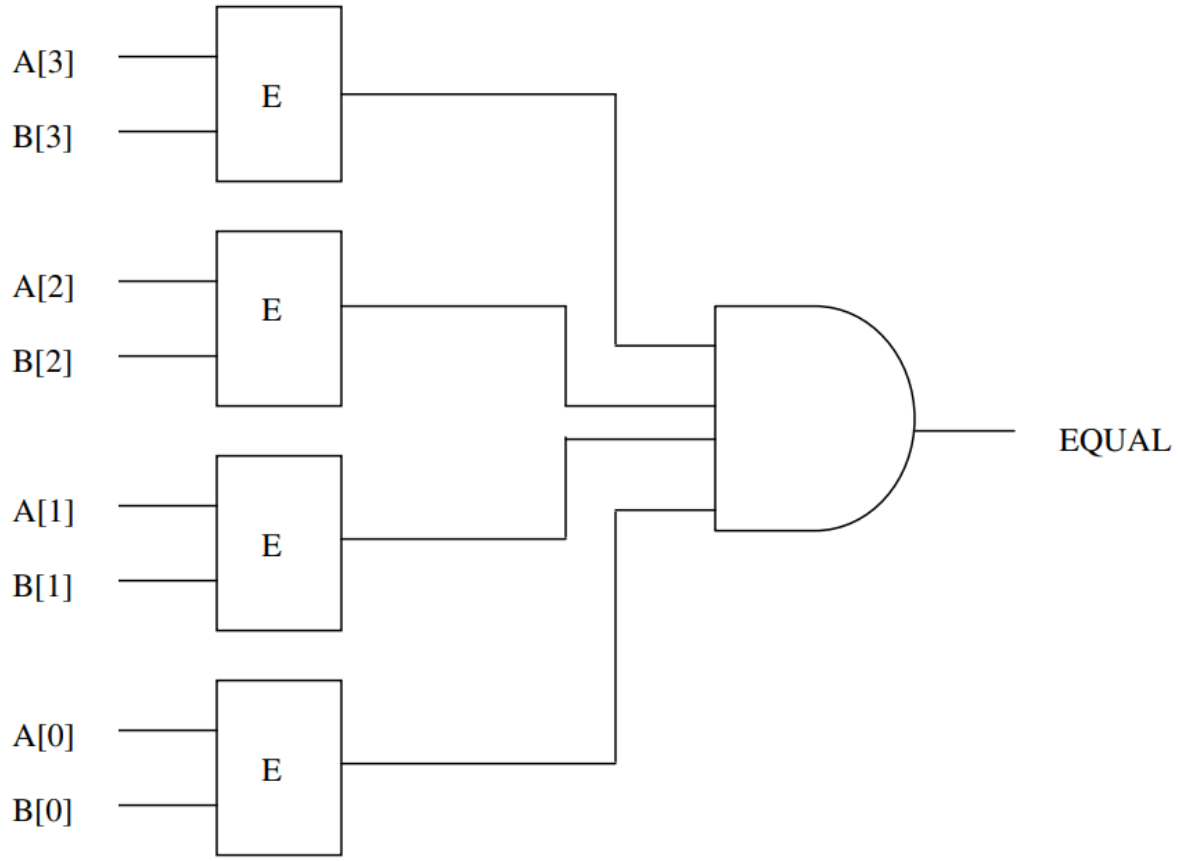
（a）(共2' 有一处错误扣一分)

A	B	G	E	L
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

（b）(共2' 有一处错误扣一分)



（c）(共2' 有一处错误扣一分)



3.40

（a）4 locations (1')

（b）4 bits (1')

（c）0001(1')

3.50

(3‘ 每个步骤各1’)

（1）implement a NOT gate with a NAND gate（A nand A）

（2）implement an AND gate using a NAND gate followed by a NOT gate（nand后面加一个（1）中的not即可）

（3）implement an OR gate using just AND gates and NOT gates（德摩根定律）