TWINS BMC FIRMWARE SPECIFICATION

VERSION 1.3

CESBG/CABG
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REVISION HISTORY

Revision	Affected Section	Revision History	Date
0.1		draft version	2017/2/13
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0.3		Update sensor information	2017/6/16
0.4		1.Modify Sensor setting & data 2.Add new sensor: PS1_Temp. PS2_Temp	2017/07/05
0.5		1.Modify sensor name for different use 2.Rmove Redfish spec	2017/07/07
0.6		1.Modify sensor name & sensor number for consistency with other project	2017/08/28
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0.8		1. Modify Device ID – 00168Bh to 0056DEh 2. Modify Temp Sensor threshold	2018/01/18
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1.0		1. Update block diagram 2. Add OCP temp sensor 3. Modify LED behavior when KVM enabled	2018/04/09
1.1		1. Update Sensor Table	2018/8/10
1.2		1. Update Sensor Table	2019/01/15
1.3		1. Update Sensor TablE。2.Update OEM cmd table.	2019/09/03

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GLOSSARY & ABBREVIATION

Glossary & Abbreviation	Explanation
BMC	**B**aseboard **M**anagement **C**ontroller, this is the common abbreviation for an IPMI Baseboard Management Controller
IBMC	**I**ntegrated **B**aseboard **M**anagement **C**ontroller, this is the name for the 2nd generation of IBMC hardware, we use AST2500 on Platform
IMM	**I**ntegrated **M**anagement **M**odule, this means the same as IBMC
IPMI	**I**ntelligent **P**latform **M**anagement **I**nterface, a standardized system management interface
IPMB	**I**ntelligent **P**latform **M**anagement **B**us, I2C based bus
SOL	**S**erial **O**ver **L**AN, Host serial port traffic redirected over a LAN connection for remote control and management
SDR	**S**ensor **D**ata **R**ecord, A data record that provides platform management sensor type, locations, event generation, and access information
Serial Port Sharing	Ability to share a serial connector between the iBMC's serial controller and a system serial controller by using circuitry to allow it to be switched between the two
POST	**P**ower **O**n **S**elf **T**est
OEM	**O**riginal **E**quipment **M**anufacturer
FRU	**F**ield **R**eplaceable **U**nit
VPD	**V**ital **P**roduct **D**ata, this is the term given to system component manufacturing information such as, but not limited to, serial number and FRU part number
SEL	**S**ystem **E**vent **L**og
SMS	**S**ystem **M**anagement **S**oftware
SMM	**S**ystem **M**anagement **M**ode
NMI	**N**on **M**askable **I**nterrupt
SMI	**S**ystem **M**anagement **I**nterrupt
IERR	**I**nternal **Err**or. A signal from the Intel Architecture processors indicating an internal error condition
PERR	**P**arity **Err**or. A signal on the PCI bus that indicates a parity error on the bus
SERR	**S**ystem **Err**or. A signal on the PCI bus that indicates a 'fatal' error on the bus
PECI	**P**latform **E**nvironment **C**ontrol **I**nterface
FRB	**F**ault **R**esilient **B**ooting

SCOPE

This document describes Twins BMC and implementation specification. This documents does not describe every detail of a general BMC implementation, but only those specific to Twins projects. For those features and implementation that were implemented in Spirit series will be referred to but will not be described.

Audience:

This specification is intended for the following audiences:

- Server Management Firmware Engineers
- System BIOS Engineers
- Diagnostic Software and Utilities Engineers
- Validation Engineers
- OEM Design Engineers

CHAPTER 1. HARDWARE

1.1.SYSTEM SPECIFICATIONS

Refer to

1.

System Block Diagram

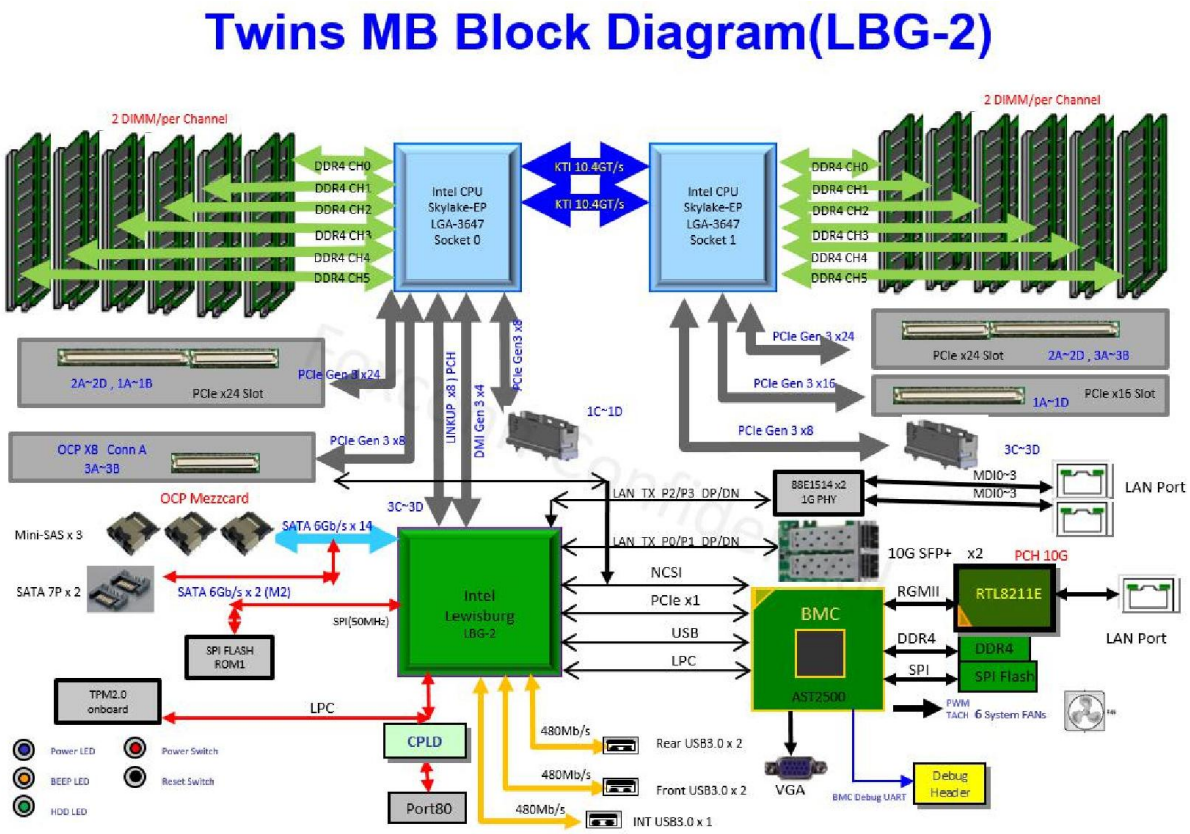

Figure 1-1 System block diagram

1.2.PLATFORM MAIN COMPONENTS RELATED TO IBMC

Table 1-1 Main component related to BMC

Intel Purley platform	- CPU(Skylake-EP) + PCH(Lewisburg) - NM4.0 supported
IBMC	AST2500 (refer to Appendix A)
Flash ROM	BIOS side: W25Q256FVFIQ (32M, U109, primary) W25Q256FVFIQ (32M, U59, secondary) BMC side: MX25L25635FM (32M, U90)

Memory	MT40A512M16HA (1GB)
LAN	RMII1: IBMC dedicated LAN. PHY RTL8211E RMII2: Share NIC. OCP Mezz slot (J18)
FRU device	CAT24C64 (8KB)
GPIO/SGPIO	Refer to EE / CPLD GPIO table: 1. BMC AST2500 PIN MAP20161022.xlsx 2. TWINS_BMC AST2500 PIN MAP20170110.xlsx
UART	UART1: System UART (J8) UART2: CM console (J17) UART5: BMC console (J29)
LED	System Health LED (Green/Amber) BMC HeartBeat LED UID LED
Button	Power button System Reset button UID/BMC Reset button
IDs	Board Ver ID: 3 GPIO pins are used as FM_FAB_REV_ID[2:0] (connect to BMC) Board SKU ID: 3 GPIO pins are used as FM_SKU_ID[2:0] (connect to PCH)
CPLD	Lattice LCMXO3LF-2100C
VR controllers	TPS53659 TPS53626
Firmware Vendor of Code Base	AMI MegaRAC 11.6

1.3.I2C BLOCK DIAGRAM

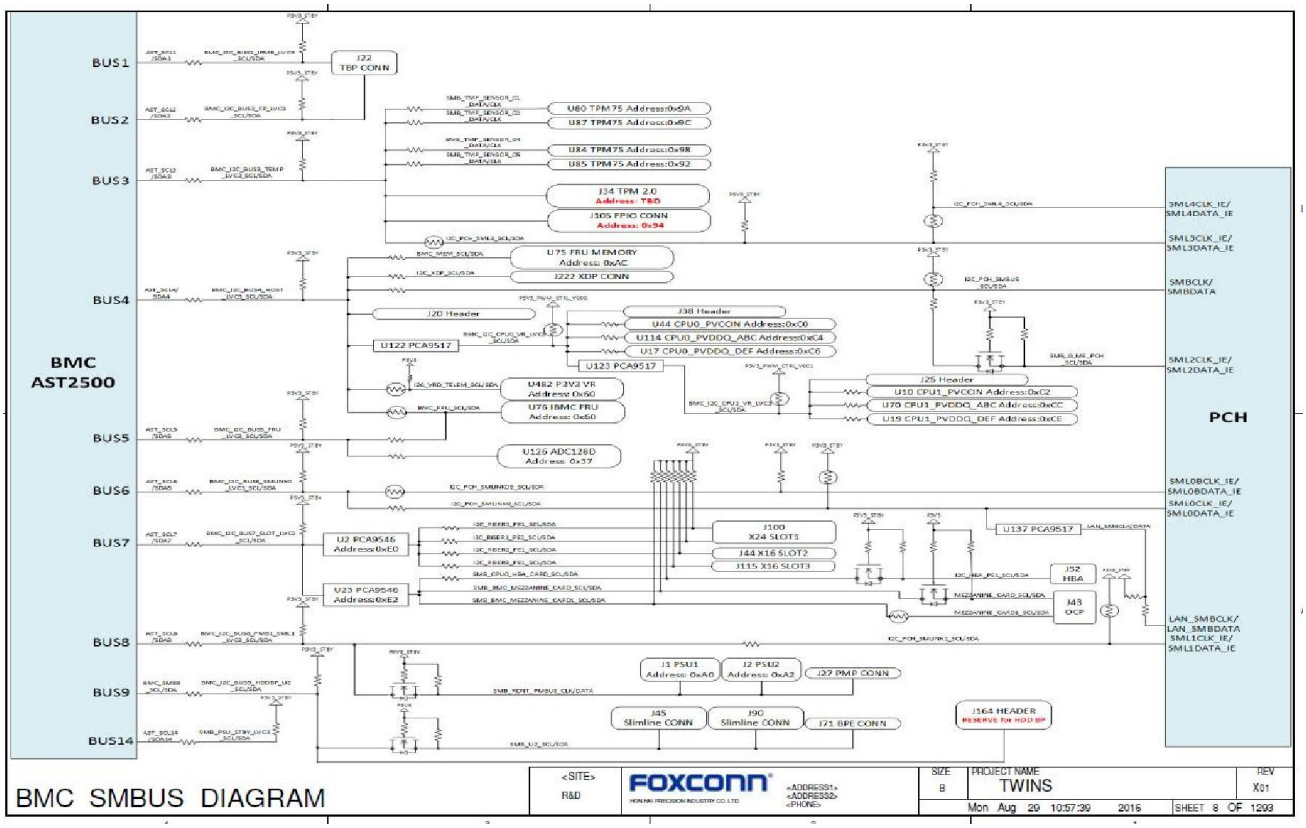

Figure 1-2 I2c block diagram

1.3.1.I2c Bus Access

IPMI provides the Master Write-Read I2C command (IPMIv2.0 Section 22.11 *Master Write-Read Command*) for generic I2C access to the IBMC's private busses as well as the IPMB. The bus identifiers for Twins platform are listed in the below table. It should be noted that this command is only available to get to the physical busses attached to the IBMC. The state of any downstream MUX is not guaranteed and so great caution should be taken if this command is used to communicate with a bus on which a MUX is present.

Table 1-2 Master Write-Read Bus IDs

Physical Bus Number	Bus ID (channel no + bus ID + bus type)	Slave address	BMC use? (V)	Remark
1	01h			2x6 SAS Expander
		0x58 / 0x5E	V	ADT7470 (FCB)
		0x34 / 0x38		PCA9557 (FCB)
		TBD		CPLD (CPLD DB)

2	03h	0xA0		MB FRU (PIB)
		0x98		Temp sensor (PIB)
3	05h	0x9A	V	Temp sensor
		0x9C	V	Temp sensor
		0x98	V	Temp sensor
		0x92	V	Temp sensor
4	07h	0xAC		FRU memory
		0xD0		VR CPU0 PVCCIN
		0xC4		VR CPU0 PVDDQ ABC
		0xC6		VR CPU0 PVDDQ DEF
		0xD4		VR CPU1 PVCCIN
		0xCC		VR CPU1 PVDDQ ABC
		0xCE		CPU1 PVDDQ DEF
5	09h	0xA0	V	IBMC FRU
		0x37		ADT128 Voltage Sensor
6	0Bh	0x2C	V	PCH SMLink0
7	0Dh	0xE0		PCA9546A
				OCP MEZZ connector
				PCIE x16 Riser
				Extend Connector
8	0Fh	0x80	V	SN13110

CHAPTER 2. GENERAL FEATURES

2.1.IPMI MESSAGING INTERFACE

2.1.1.Channel Management

IPMI uses a 'channel model' for directing communication between different interfaces in the BMC. Channels serve as the means for identifying the medium for a messaging interface, and for configuring user information and passwords, message authentication, access modes and privilege limits associated with that interface. Please refer to the IPMIv2.0 for more detail information. The common assignments of all channels are shown in below table.

Table 2-1 Channel Assignments

Interface	Channel Number	Supports Sessions
IPMB	00h	Yes
LAN	01h	Yes
LAN(NCSI)	08h	Yes
Serial Channel	02h	Yes
Host/SMS interface	0Fh	No

2.1.2.LPC/KCS

The IBMC FW supports 3 KCS interfaces. These interfaces are mapped into the host I/O space and can be accessed through the LPC bus by host. These interfaces are assigned with the following usages and I/O addresses:

Table 2-2 KCS Interface

Name	Usage	Address
Host/SMS Interface	SMS, BIOS POST, and utility access	CA2h/CA8h/CA0h

Note: The location of the KCS registers and the I2C address of the IBMC will be reported through a Type 38 SM BIOS table entry.

2.1.3.LAN Messaging

BMC receives and responds IPMI messages via RGMII which connects BMC with on board external PHY. The channel number of LAN messaging is **01h**.

2.1.3.1.Firmware MAC Address

The MAC address will be programmed in an external EEPROM during manufacturing. And it is read only for the end user. "PS list" command of u-boot is used to show the detail configuration for the firmware developer. The bus number is 5

on which the chip of MAC address is and the chip slave address is 0xA0. The offset of MAC0 address (Dedicate LAN) in EEPROM is 0x1C00.The offset of MAC1 address (share LAN) in EEPROM is 0x1C08.

2.1.4.Serial/Modem Interface

Transmission of IPMI messages between a remote console and the BMC is in one of three configurable modes: Basic Mode, PPP Mode, and Terminal Mode.

Basic Mode This mode uses a simple clear text password to activate a session. IPMI messages are encoded and delimited using a simple framing scheme based on 'escaped' characters. Basic Mode is the most efficient standard operating mode for enabling a remote console application to communicate with the BMC using IPMI messages.

PPP/UDP Mode This mode uses the same session and authentication operation as IPMI over LAN. It uses PPP as the protocol for establishing a point-to-point communications link over which IPMI messages are sent encapsulated in UDP datagrams. This mode incurs significant overhead in message size and handshake complexity beyond that required for Basic Mode IPMI messaging, but has the advantage of using a widely supported standard.

Terminal Mode This mode is intended primarily for direct serial connection operation. The mode is designed so that a simple terminal or terminal emulator can be used to generate requests and get responses from the BMC.

2.1.5.Intelligent Platform Management Bus (IPMB)

When an IPMB is implemented in the system, the BMC serves as a controller to give system software access to the IPMB. The IPMB allows non-intelligent devices as well as management controllers on the bus. To support this operation, the BMC provides the master Write-Read command via its interface with system software. The Master Write-Read command provides low-level access to non-intelligent devices on the IPMB, Such as FRU SEEPROMS.

The Master Write-Read command provides a subset of the possible IIC and SMBus operations that covers most IIC/SMBus-compatible devices.

In addition to supporting non-intelligent devices on the IPMB, the Master Write-Read command also provides access to non-intelligent device on Private Busses behind management controllers. The main purpose of this is to support FRU SEEPROMs on Private Busses.

By default the IBMC will respond at address 20h on this bus, and the IPMB will be channel number 00h as required by the IPMIv2.0 specification.

2.1.6 Users & Password Support

The IBMC FW supports the IPMI 2.0 user model including User ID 1 support. **10** user IDs are supported. These 10 users can be assigned to any channel. The following restrictions are placed on user-related operations:

1. User names for User ID 1 can not be changed. It is always "(Null/blank)" respectively. A "CCh" error completion code is returned if a user attempts to modify this name.

2. User ID 2 is the default user. It can't be disabled until another user ID is available, except user ID 1.

3. All user passwords (including passwords for user ID 1) may be modified.

4. User IDs 3 ~10 are not set by default. They can be set in the Web GUI or by "Set User Name" and "Set User Password" commands.

Table 2-3 Default User Configuration

User ID	User Name	Password(*1)	Status	Default Privilege
1	[Null]	[Null]	Disabled	Administrator
2	**Admin(*2)**	**Admin(*2)**	**Enabled**	**Administrator**
3 ~ 10	Undefined	Undefined	Disabled	Undefined

Note:

1: Default password is per IPMIv2.0 format (The password is 20 bytes).

2: The User Name and Password can be customized by customers' special requests.

2.2.PLATFORM MONITORING

Refer to **Appendix E** for all supported sensors.

2.2.1.Analog/I2c/TACH Sensors

2.2.1.1.Temperature Monitoring

The IBMC FW provides temperature monitoring capability for ambient and physical components on the main board. This monitoring capability is instantiated in the form of IPMI analog/threshold sensors.

1. **MB_Inlet_TEMP Temperature Sensor:** is reported by a TPM75 chip on the main board.
2. **MB_Outlet_TEMP Temperature Sensor:** is reported by a TPM75 chip on the main board.
3. **DIMM Internal Temperature Sensors:** are accessed via ME.
4. **PCH_TEMP Temperature Sensor:** is accessed via ME.
5. **CPU DTS Sensors:** are accessed via ME.
6. **VRx_TEMP Temperature Sensors:** are reported by TPS53659 and TPS53626 chips on the main board. (Not supported now)
7. **HSC_TEMP Temperature Sensor:** is reported by SN13110 chips on the PIB. (Not supported now)

2.2.1.2.Power/Voltage/Current Monitoring

The IBMC FW provides voltage monitoring capability for voltage sources on the main board and processors such that all major areas of the system are covered. This monitoring capability is instantiated in the form of IPMI analog/threshold sensors.

1. **P12V/P3V3/P5V/P12V_STBY/BAT_P3V:** are reported by the ADC channel of AST2500 BMC chip on the main

board.

2. **HSC_Input_Power / HSC_Input_Volt sensors:** are reported by SN13110 chips on the PMP board. (Not supported now)

2.2.1.3.Fan Speed Monitoring

The IBMC FW controls and monitors the system fans. Each fan is associated with a fan speed sensor that detects fan failure. This monitoring capability is instantiated in the form of IPMI analog/threshold sensors.

1. **FANx sensors:** are reported by TACH channels of two ADT7470 chips on the FCB.

2.2.2.Discrete Sensor

BMC firmware access and display discrete sensors in SDR. BMC should log abnormal sensor reading to SEL. The discrete sensors required and the SEL format is listed as below for error decoding purpose. Please refer to BMC sensor table for more detail implementation requirement.

1. **DIMMG0_1_Hot / DIMMG1_1_Hot / DIMM_Alert / CPUx_Hot / CPUx_Thermaltrip / SYS_PWR_Reset / CPU_Err / DIMMGx_VR_Fault / CPU_VR_Fault sensors:** are reported by the SGPIO channel of AST2500 BMC chip.
2. **SEL_sensor sensor:** is reported by internal sensors of AST2500 BMC chip.
3. **Watchdog2 sensor:** is reported by internal sensors of AST2500 BMC chip.
4. **SYS_PWR_Monitor sensor:** is to monitor the SYS_PWROK pin status of PCH by the GPIO channel of AST2500 BMC chip.
5. **NMI_State sensor:** is reported by the GPIO channel of AST2500 BMC chip. (Not supported now)

2.2.2.1.Critical Interrupt Sensor (TBD)

The IBMC FW provides an IPMI sensor of type critical interrupt for monitoring status NMI.

- **Software NMI:** The IBMC FW could response to the Chassis Control command (pulse diagnostic interrupt) or Watchdog Timer pre-timeout expiration with NMI / diagnostic interrupt action, and generates an NMI to the host system. This event will be logged as “Software NMI”. BIOS will trigger a software NMI SEL.

2.2.3.Event Only sensor

The event only sensors are not shown in SDR. These sensors trigger SEL if abnormal value is detected. The event only discrete sensors are provided as below, and Event Data 1,2 and 3 format is for decoding purpose.

1. None. (there is no event only sensor)

2.3.PLATFORM CONTROL

2.3.1.Chassis Control

IBMC FW provides a mechanism for providing power up, power down, power cycle control via chassis control command. And this command can be executed through IPMI-Over-LAN (IOL) and Web GUI. So, the chassis can be controlled remotely. Detail information of the chassis control command is listed below.

Table 2-4 Supported Chassis Control Options

Item	Supported	Description
Power Down	Yes	
Power Up	Yes	
Power Cycle	Yes	
Hard Reset	Yes	
Software Interrupt	No	Simulate NMI to the host system
Soft Shutdown	Yes	

Note: It should wait at least 7 seconds to complete the process Power Down function

2.3.2.LED

The supported LED control options are shown below.

Table 2-5 Supported LED Control Options

Item	Supported	Description
System Power LED	Yes	(1) Power LED is solid Amber while power cable is connected but power is off (2) Power LED is solid green while power cable is connected and power is on
System Health LED	Yes	(1) Status LED show solid Amber while SEL events happen. (2) Status LED show solid Green while system is in normal state.
UID LED	Yes	It is controlled by chassis identify command and UID button pressed.

2.3.3.Buttons

The supported buttons control options are shown below.

Table 2-6 Supported Buttons Control Options

Item	Supported	Description
Power Button	Yes (*1)	BMC FW can simulate a power button behavior
System Reset Button	Yes	
BMC Reset Button	No	
UID Button	Yes	1. Press UID Button less than 4s is to turn on/off UID LED.

		2. Press UID Button larger than 4s is to do IPMI warm reset command.

Note 1: It's activated by CPLD firmware.

2.4.SYSTEM EVENT LOG (SEL) AND EVENT MESSAGES

The IBMC FW provides a System Event Log interface. SEL can be accessed via all the supported interfaces and Web GUI. The IBMC FW allocates non-volatile storage space of SPI flash to store SELs. Up to 453 SEL records can be stored at a time. When SEL is full, default is stopping logging SEL.

2.4.1.Event Logging Disabled Sensor

This sensor provides the ability to alert users when the log becomes almost full (75% full) or full (100% full). And it can also indicate that the log area is reset or cleared.

0ffset:

0x02- Log Area Reset/Cleared

0x04- SEL Full.

0x05- SEL Almost Full

2.4.2.IPMI SEL Time

Each SEL record contains a four-byte timestamp that indicates when the record was created. The IBMC FW maintains a 4-byte internal timestamp clock. This internal timestamp clock is read and set using the Get SEL Time and Set SEL Time commands, respectively. The Get SDR Time command can also be used to read the timestamp clock, but is not recommended.

2.4.2.1.Internal Timestamp Init

During IBMC FW initialization, it cannot guarantee the validity of its internal timestamp due to no battery backup. Therefore, it resets its clock counter to zero. The pre-init timestamp range 0x00000000 through 0x20000000 are used for events that occur after the initialization of the System Event Log device up to the time that the timestamp is set with the system time value. Thus, these timestamp values are relative to the completion of the SEL device's initialization, not January 1, 1970.

2.4.2.2.System Clock Sync

According to IPMI v2.0 Spec, the BIOS must send the Set SEL Time command with the current system time to the IBMC FW during system Power-on Self Test (POST). Synchronization during very early POST is preferred, so that any SEL entries recorded during system boot can be accurately time stamped. If the time is modified through an OS interface, then the IBMC FW's timestamp is not synchronized until the next system reboot.

Additionally, the IBMC FW can supports to synchronize IBMC time with system RTC clock through SMLink0 during IBMC boots. If NTP Server is supported, IBMC will also synchronize IBMC time with NTP servers.

2.4.2.3.Supported SEL events

Please refer to **Appendix E,** Table E-2., and Table E-3.

2.5.PLATFORM EVENT FILTERING (PEF) AND ALERT POLICIES

PEF (IPMIv2.0 Chapter 17 *Platform Event Filtering (PEF)*) will be supported to allow alerting in response to configured system events. On the platform, the following event filters and alert policies will be implemented by default. Any additional filters or alert policies desired by the user must be configured using the Set PEF Configuration Parameters command discussed in Section 30.3 of the IPMIv2.0 specification.

2.5.1.Alert Policy Table

Table 2-7 Alert Policy Table

Byte	Field	Description
		DATA BYTES
1	Policy Number / Policy	This value identifies the entries belonging to a particular policy set. When an Alert Action is taken, the BMC will scan the Alert Policy Table and will attempt to generate alerts based on the entries that form the policy set. [7:4] - policy number. 1 based. 0000b = reserved. [3] - 0b = this entry is disabled. Skip to next entry in policy, if any. 1b = this entry is enabled. [2:0] - policy 0h = always send alert to this destination. 1h = if alert to previous destination was successful, do not send alert to this destination. Proceed to next entry in this policy set. 2h = if alert to previous destination was successful, do not send alert to this destination. Do not process any more entries in this policy set. 3h = if alert to previous destination was successful, do not send alert to this destination. Proceed to next entry in this policy set that is to a different channel. 4h = if alert to previous destination was successful, do not send alert to this destination. Proceed to next entry in this policy set that is to a different destination type.
2	Channel / Destination	Channel that the alert is to be sent over. Channel determines which set of destination addresses or phone number/s is used. Destination addresses and/or phone numbers are set via the LAN and/or serial/modem configuration parameter commands. The Alert Type (e.g. PET, TAP, Dial Page, etc.) is specified in the configuration parameters associated with the specified destination. [7:4] = Channel Number. [3:0] = Destination selector.
3	Alert String Key	This field holds information that is used to look up the Alert String to send for this Alert Policy entry. 00h = no alert string. [7] - Event-specific Alert String 1b = Alert String look-up is event specific. The following Alert String Set / Selector sub-field is interpreted as an *Alert String Set Number* that is used in conjunction with the Event Filter Number to lookup the Alert String from the PEF Configuration Parameters. 0b = Alert String is not event specific. The following Alert String Set / Selector sub-field is interpreted as an *Alert String Selector* that provides a direct pointer to the desired Alert String from the PEF Configuration Parameters. [6:0] - Alert String Set / Selector. This value identifies one or more Alert Strings in the Alert String table. When used as an *Alert String Set Number*, it is used in conjunction with the Event Filter Number to uniquely identify an Alert String. When used as an *Alert String Selector* it directly selects an Alert String from the PEF Configuration Parameters. The Alert String Key and lookup mechanism allows the Alert String to be 'Event Specific' - meaning the string selection is determined by both the Event Policy Entry and Event Filter, or; the string can be selected by the Event Policy alone. An Alert String can be pointed to by multiple policy entries. The Alert Policy Entry identifies a particular channel and destination for an alert. This in turn, identifies the alert type. Thus, the binding of an Alert Policy Entry and an Alert String effectively provides a mechanism for allowing different Alert Strings to be selected based on the alert destination, or the type of alert destination. For example, a single Alert String could be shared among all Alert Policy Entries for 'Dial Page' destinations, while event-specific Alert Strings could be used for alerts to LAN destinations.

The IBMC FW reserves 40 alert policy entries. The default value is showed in below table.(TBD)

Table 2-8 Alert Policy Default

Alert Policy Entry Number	Setting
1	0x10 0x10 0x81
2	0x10 0x10 0x81
3	0x10 0x10 0x81
4	0x10 0x10 0x81
5	0x10 0x10 0x81
6	0x10 0x10 0x81
……	……

Alert String Key:

[7] – 1b = Alert String look-up is event specific, and it will be searched in PEF configuration parameter 12#

– 0b = Alert String look-up is event not specific, and it will be searched in PEF configuration parameter 13#

2.5.2.Alert String Keys and Alert Strings (TBD)

The IBMC FW reserves 40 sets of alert string keys and strings. The default value is showed in below table.

Table 2-9 Alert String Keys and Strings

Selector Number	Alert String key	Alert String (48Bytes, 3 Blocks)
1	0 0	N/A
2	0 0	N/A
3	0 0	N/A
4	0 0	N/A
5	0 0	N/A
6	0 0	N/A
7	0 0	N/A
8	0 0	N/A
…	…	…

2.5.3.PEF Action PEF Action

The IBMC FW supports the following PEF actions:

- Power off
- Power cycle
- Reset
- Alerts
- NMI

The IBMC FW provides an IPMI type sensor 02h, system event, for the PEF action. This sensor is disabled by default.

Please refer to the PEF configuration parameters.

2.5.4.Event Processing When the SEL Is Full

If the SEL is full and Event Message Buffer is enabled, new events could still be put into the buffer. Up to 10 event messages can be stored in the buffer at a time. The Event Message Buffer for IPMI v1.5 is not overwritten if new events come in. Therefore, if the Event Message Buffer is full, further events will not go into the event message buffer until it's cleared.

"Get BMC global enables" command can be used to retrieve the present setting of Event Message Buffer enables. "Set BMC global enables" command can be used to enable the buffer.

2.6.FRU

FRU data will be available in IPMI FRU format through the IPMI FRU Commands. The FRU storage area will be located in a special EEPROM chip connected to BMC through I2C bus. The system FRU information should be provided via FRU Device ID and the access information will be defined as below:

2.6.1.FRU Devices & Access Information

IPMI provides FRU information in two ways: via an IBMC, or via FRU SEEPROMs. FRU information that is managed by an IBMC is accessed using IPMI commands. In this project, FRU information is stored in SEEPROMs. The SEEPROM information is shown below,

Table 2-10 FRU Devices

FRU Device ID	Description	I2C Bus ID	Slave Address	Base Offset
0x00	System FRU	0X09(*1)	0xA0	0x0000

Note: 1. I2C bus ID is the 1st request data byte of Master Write-Read command.

2.6.2.FRU Byte Definition

FRU data byte definition follows FRU spec V1.0. The FRU information for Twins project can be refer to Appendix D

2.7.SOL

The IBMC FW supports IPMI 2.0 SOL. SOL sessions are only supported on serial port 2 (COM2).

IPMI 2.0 introduced a standard serial-over-LAN feature. This is implemented as a standard payload type (01h) over RMCP+.

Three commands are implemented for SOL 2.0 configuration:

- "Get SOL 2.0 Configuration Parameters" and "Set SOL 2.0 Configuration Parameters": These commands are used to get and set the values of the SOL configuration parameters. The parameters are implemented on a per-channel basis. See Table 52.
- "Activating SOL": This command is not accepted by the BMC. It is sent by the BMC when SOL is activated, to notify

a remote client of the switch to SOL.

Activating a SOL session requires an existing IPMI-over-LAN session. If encryption is used, it should be negotiated when the IOL session is established. 02

Note: The function keys and keypad setting of tool using should compatible with the setting in BIOS.

You can manually input unsupported keystrokes by entering escape sequences.	
ESC+2	F2
ESC+7	F7
ESC+@	F12

Table 2-11 SOL Configuration Parameters

Parameter Name	#	Default Value
SOL Enable	1	01 – SOL payload enabled
SOL Authentication	2	84h [7] = 1b – Force Encryption [6] = 0b – Authentication controlled by remote software [3:0] = 04h – Administrator level
Character Accumulate Interval & Character Send Threshold	3	0Ch 60h
SOL Retry	4	07h 32h
SOL NV bit rate (non-volatile)	5	06h –115.2kbps
SOL volatile bit rate (volatile)	6	06h – 115.2 kbps
SOL Payload Channel (optional, Read Only)	7	01h
SOL Payload Port Number (Read Only or Read/Write – see description)	8	6Fh 02h – 26Fh

2.8.1FIRMWARE UPDATE

2.8.1.BMC FW

2.8.1.1.Update via Web GUI

The steps of FW update via Web GUI are showed below.

1. Log into Web GUI via Web Browser
2. Select “Maintenance” -> "Firmware Update" menu of the left view menu
3. Choose the “Preserve all configuration” on the checkbox if all configurations need to be preserved.
4. “Select Firmware Image” to select the BMC FW image.

5. Click “Start Firmware Update”
6. Choose “Flash selected section” (Default is all) to start BMC FW update.
7. After BMC FW is updated, system will pop up a message.

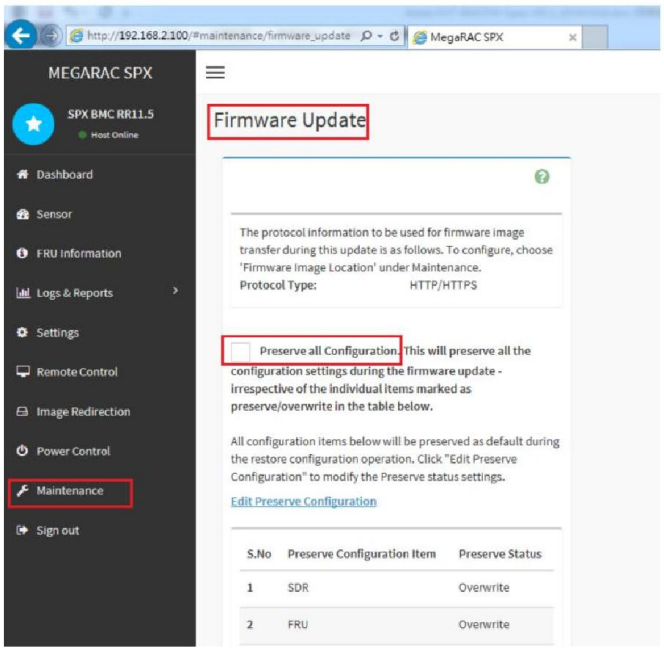

Figure 2-1-1

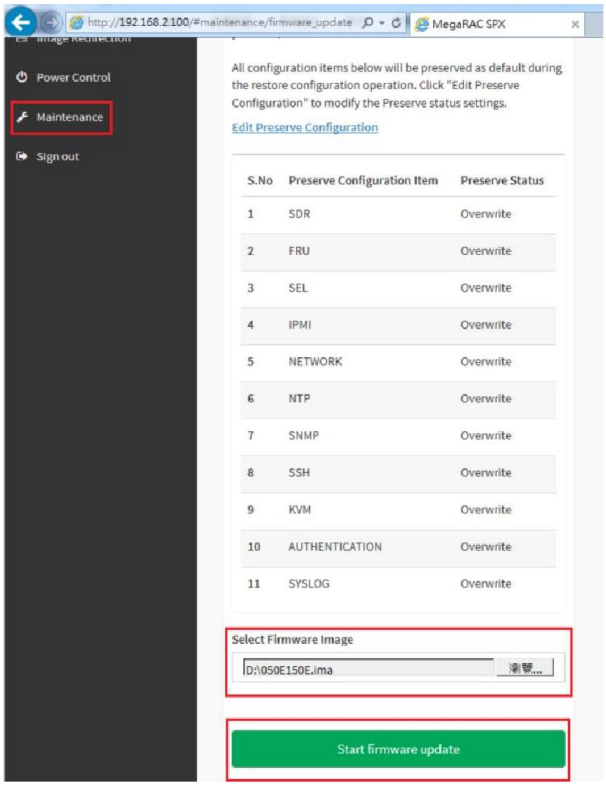

Figure 2-1-2

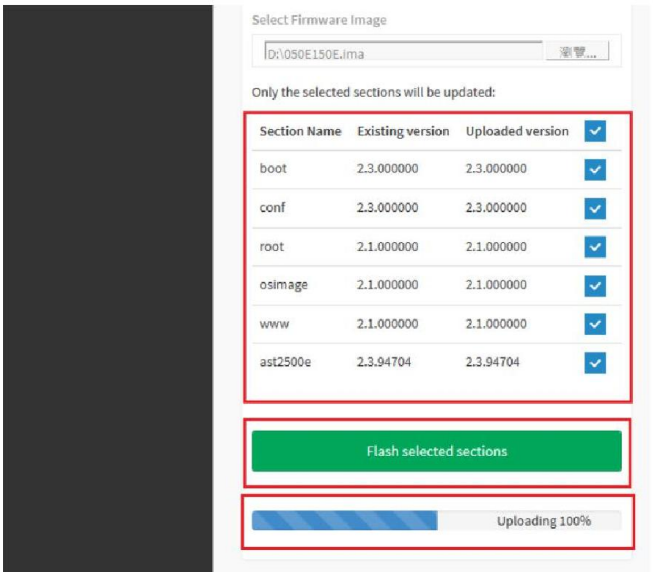

Figure 2-1-3

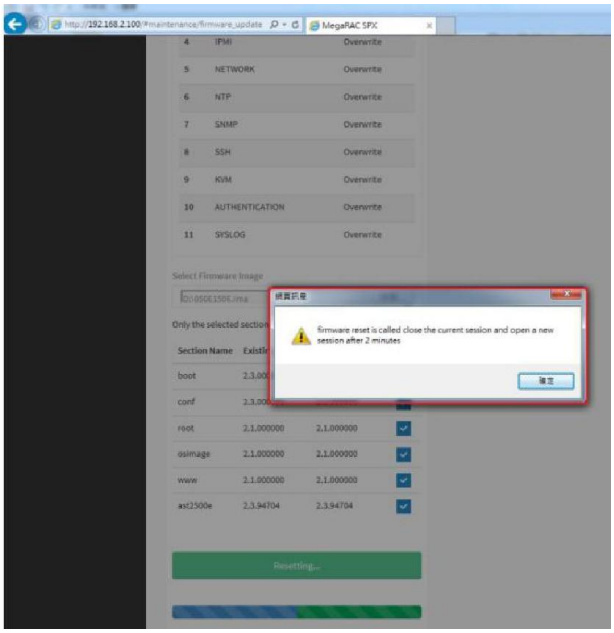

Figure 2-1-4

Figure 2-1 Firmware Update via WebUI

2.8.1.2.Update Utilities of AMI

FW update utilities of AMI, named Yafuflash, are used to perform IBMC firmware update under UEFI, Linux 32/64bits.

2.8.1.3.Update Utilities of Aspeed

FW update utilities of Aspeed, named socflash, are used to do engineering validation only, and UEFI, Linux 32/64bits are supported. The latest socflash can be download from the Web site of Aspeed.

Note: Socflash uses rom file to update firmware, and it will restore default configuration always.

2.8.2.Others

Table 2-12 Supported FW update lists

Items	Supported	Comments
BMC FW	V	Refer to Sec.2.8.1
BIOS FW image (including BIOS/ME/Gbe….)	V	
CPLD FW image		
VR FW image		
PSU FW image		

2.9.WEB GUI

Web GUI is a friendly interface for the end users. Users can access the IBMC FW via a HTML5 supported web browser, and then can go through the server status and do many configurations to the IBMC FW. Web user privilege only allows administrator initially.

2.9.1.Specification

Please refer to IBMC FW Web GUI specification, Twins_BMC_WebGUI_Spec-V0.1-20170126.pdf

2.9.2.Supported Web Browser

The IBMC FW can support below Web Browser (Recommend using the latest version):

- Microsoft IE
- Firefox
- Chrome (Recommended)

2.10.WATCHDOG TIMER ACTIONS

The following actions are supported on expiration of the Watchdog Timer:

- System Reset
- System Power Off
- System Power Cycle

2.10.1.Pre-timeout Interrupt

The Watchdog Timer offers a 'Pre-timeout Interrupt' option. This option is enabled whenever the 'Interrupt on timeout' option is selected coincident with any of the other Watchdog Timer actions.

2.10.2.Watchdog Timer Event Logging

By default, the BMC will automatically log the corresponding sensor-specific watchdog sensor event when a timer expiration occurs. A "don't log" bit is provided to temporarily disable the automatic logging. The "don't log" bit is automatically cleared (logging re-enabled) whenever a timer expiration occurs.

2.10.3.Common Usage in System

- **BIOS FRB2 Timeout:** An FRB-2 (fault-resilient booting, level 2) timeout has occurred. This indicates that the last system reset or power cycle was due to the system timeout during POST, presumed to be caused by a failure or hang related to the bootstrap processor. The timeout interval can be set in BIOS setup menu.
- **OS Load Timeout:** The last reset or power cycle was caused by the timer being used to 'watchdog' the interval from 'boot' to OS up and running. This mode requires system management software, or OS support. BIOS should starts this timer after POST completes, and clear this flag if it starts this timer during POST. The timeout interval can be set in BIOS setup menu.

SMS "OS Watchdog" Timeout: This indicates that the timer was being used by System Management Software. During run-time, System Management Software (SMS) starts the timer, and then periodically resets it to keep it from expiring. This periodic action serves as a 'heartbeat' that indicates that the OS (or at least the SMS task) is still functioning. If OS and SMS hang, the timer expires and the IBMC FW generates a system reset. This is also called ASR (Auto Server Restart). When SMS enables the timer, it should make sure the 'SMS' bit is set to indicate that the timer is being used in its 'OS Watchdog' role.

2.10.4.HW WDT for IBMC

After a programmable counter counts down to zero, a system reset signal is generated to reset BMC or full chip. (TBD)

2.11.SERIAL REDIRECTION

The system can take control of the shared serial port to perform text console redirection. Additionally, the IBMC FW can be configured to capture the host serial port traffic and redirect it to the system network controller via RMCP+ messages. This enables remote management via a serial over LAN (SOL) interface.

2.11.1.KVM Redirection

The IBMC firmware supports keyboard, video, and mouse redirection (KVM) over LAN. This feature is available remotely from the embedded Web GUI as a Java applet. This feature requires that Java 1.5.7 or later is installed on the host system. Java Web Start 1.6 is required to launch the KVM over an IPv6 network. The features of KVM is listed below.

- Converts the analog keyboard, video and mouses(KVM) signals into digital packets, compressing them and transmitting them securely over TCP/IP connections.
- Requirements:(TBD)
  - Performance, bandwidth, frame per second
- DVC, buffered/un-buffered core
  - Maximum resolution
- Support the following host resolutions:
  - 1280 x 1024 @ 60 Hz
  - 1024 x 768 @ 60, 72, 75 and 85 Hz
  - 800 x 600 @ 60, 72, 75 and 85 Hz
  - 640 x 480 @ 60, 72, 75 and 85 Hz
- Provide two levels of video quality:
  - YUV420 – lower quality and higher compression
  - YUV444 – higher quality and lower compression (this mode requires more processor time and network bandwidth)

Note: There is 1 virtual USB keyboard, and there are 2 virtual USB mice for KVM function: one mouse is for Windows, and the other is for Linux. These virtual USB devices will always exist during BMC firmware life time.

2.12.FSC (FAN SPEED CONTROL)

IBMC FW will implement the FSC table provided by thermal team.

2.12.1.Sensors and Fans

The FSC supports max of 5 fan profiles. Each sensor set is mapping to each fan profile.

Table 2-13 Sensors and Fan actions

Sensor Name	Sensor	Actions	Supported
Ambient Sensor	On board Ambient sensor	Open loop profiles	V
CPU	CPU0,CPU1_System Detected	Close loop profiles	V
DIMM	DIMM Internal chip sensor		V
PCH	PCH Internal chip sensor		V
PCIe	PCIe card temperature sensor		TBD

2.12.2.Open Loop Control Policy

Expected PWM duty cycle of fan speed is depended on the ambient sensor, and follows following formula.

PWM Duty cycle (%) = a*Sys Amb^2+b*Sys Amb(C)+c.

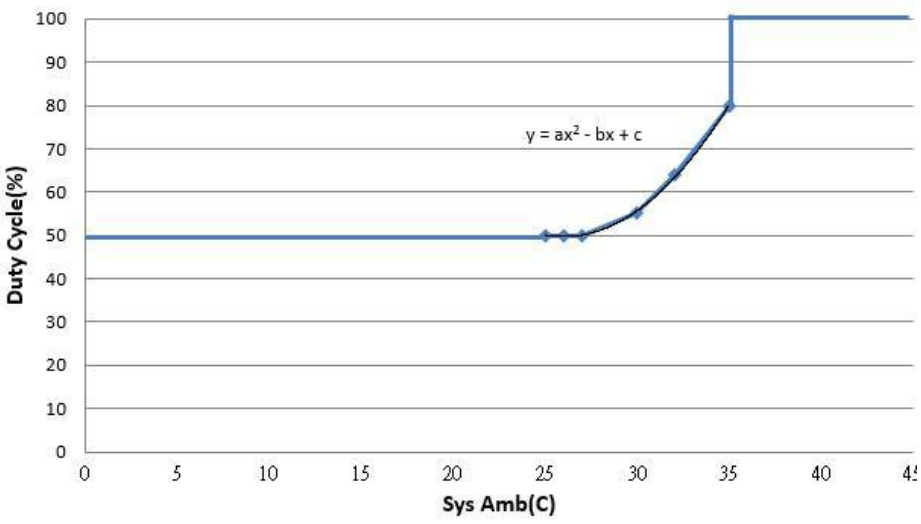

Figure 2-2 Open loop policy

2.12.3.Close Loop Control Policy

Expected PWM duty cycle of fan speed is depended on related sensors, and follows following flow chart.

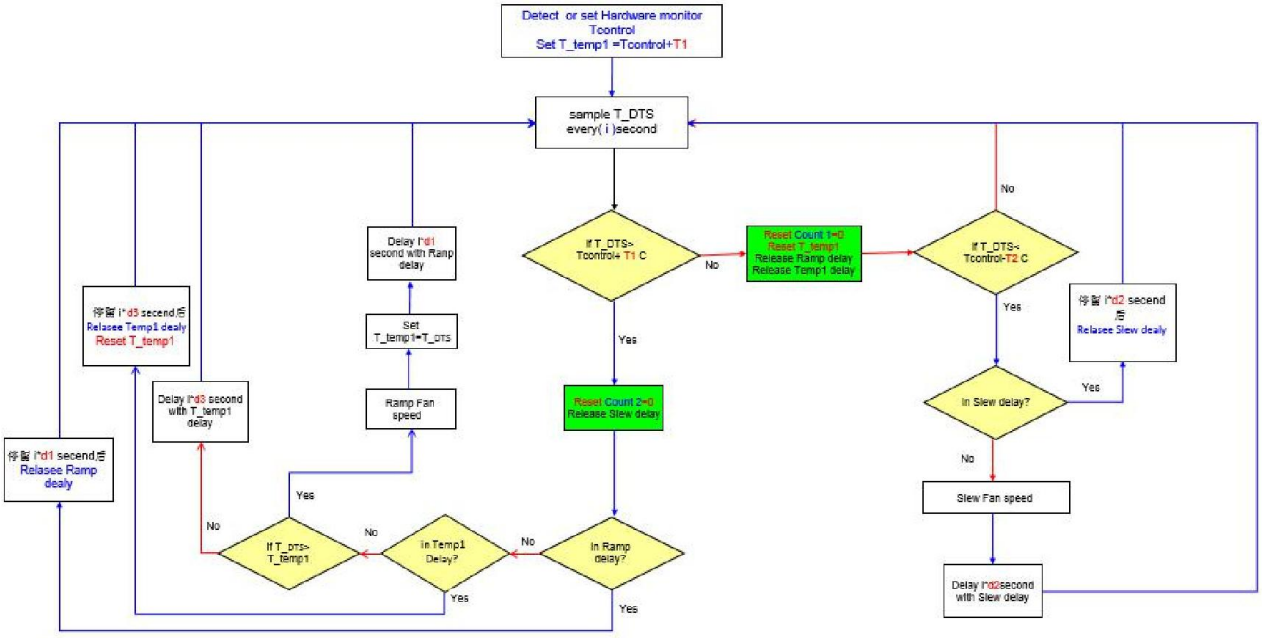

Figure 2-3 Close loop control policy

2.12.4.Threshold Definition

The FSC table defines in which temperature IBMC should alert/de-alert SEL events or let system shut down to avoid thermal damage. Below table is a threshold definition example.

Table 2-14 Sensor Threshold Definitions

Sensor Items	Normal	UNC(*1)	UC(*2)	Shutdown
CPU	<-3	-3	-1	NA
DIMM	<83	83	85	NA
PCH	<90	90	92	NA
System Ambient	<35	35	38	NA

Note: 1 UNC: Upper Non-Critical

2. UC: Upper Critical

2.13.SECURITY

2.13.1.firmware firewall

The IBMC FW can support Firmware Firewall. Firmware firewall is an IPMIv2.0 optional capability that is supported on all iBMC implementations. Details can be found in the IPMIv2.0 specification Chapter 21.

Firmware firewall implements three basic categories of commands for the purposes of preventing inadvertent or malicious access to the IBMC or system.

- The first category provides external software to query which commands are supported, known as “command discovery commands”.
- The second category allows queries of which commands can be enabled or disabled, known as “configurable

command discovery".

■ The final category allows configurable commands to be enabled or disabled. By default, all supported commands are enabled in the BMC implementations.

2.14.VIRTUAL MEDIA

Virtual Media allows a floppy image, floppy drive or CD/DVD drive on your system, to be available on the managed system's console as if the floppy image or drive were present on the local system. For example, after you virtualize a drive on a managed system running the Microsoft(R) Windows(R) operating system, the virtualized drive appears in Windows Explorer as a real drive with a new drive letter (for example, G:).

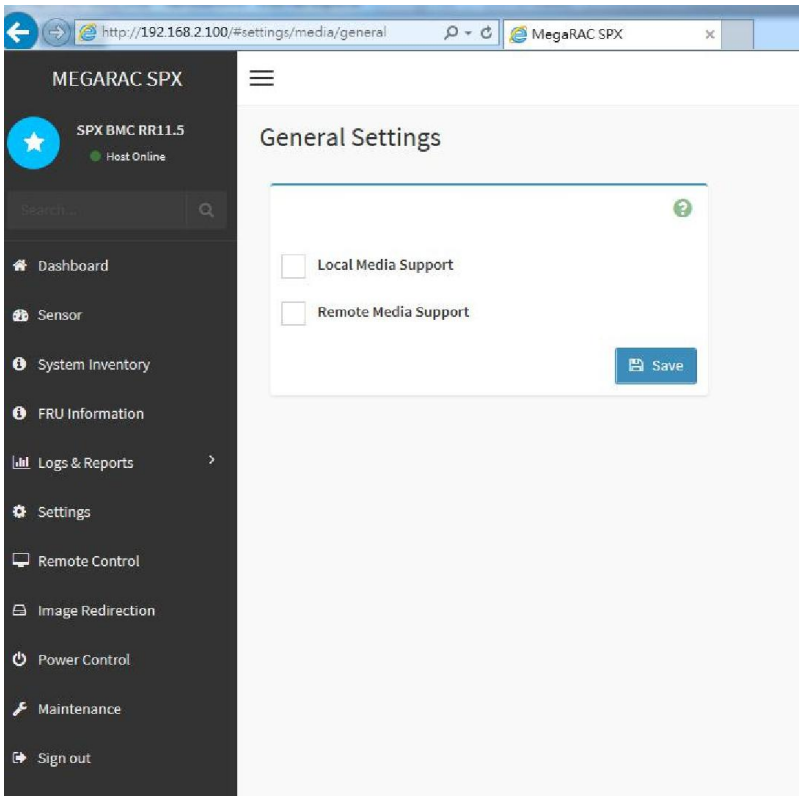

Figure 2-4 Virtual Media

Note: All virtual USB devices (excluding the keyboard and mouse) will not mount to the host system until the end user opens the virtual media session from Web GUI.

2.15.SMASH-CLP

SMASH-CLP sessions to the IBMC FW could be supported by Secure Shell (SSH) connection.

2.16.IBMC FIRMWARE AND BIOS INTERFACE

BIOS is able to communicate with IBMC FW via KCS interface over the LPC bus. The I/O base address is defined in system interface.

Table 2-15 BIOS and FW Interface

BIOS Function	Sub-function	IPMI CMD Implementation (HEX)
Send real time clock data during post	/	**Set SEL Time (0A, 49)**
IBMC initial health check and report status	/	**Get Self Test Results (06, 04)**
Show IBMC firmware information	/	**Get Device ID (06, 01)**
Maintain and control system GUID and provide it to IBMC during POST	/	**Set System GUID (2E, CC)** (OSA CMD)
BIOS POST phase: Log Failure Alerts for firmware/hardware error or event check	System firmware error/hang	**Platform Event (04, 02)** **PEF Table**
	Memory error/event	
	Processor error/event	
	PCI error/event	
Operating system running phase: log system event or error by SMI handler	Memory correctable or uncorrectable errors	
	PCI PERR/SERR errors	
	Processor correctable or uncorrectable machine check errors	
	System/platform specific event (Pecos cable fail-over, memory hot add, hot replace, and hot spare events and errors)	
System Event Log (SEL) Access	Log new SEL entry	**Add SEL Entry (0A, 44)**
	Get SEL enty	**Get SEL Entry (0A, 43)**
	Delete SEL entry	**Reserve SEL (0A, 42)** **Clear SEL (0A, 47)**
System VPD Access	/	**Master read-write (06, 52)**
IBMC LAN Configuration	IP Address(3)	**Get/Set LAN Configuration (0C, 01/02)**
	IP Source(4)	
	MAC Address(5)	
	Subnet Address(6)	
	Gateway Address(12)	
POST/OS Loader Watchdog Timer support	Start/Stop Watchdog Time	**Set Watchdog Timer (06, 24)**
	Reset Watchdog Timer	**Reset Watchdog Timer (06, 22)**
COM port sharing for serial redirection	Enable/Disable serial port sharing (Parameter 8)	**Get/Set Serial/modem configuration (0C, 10/11)**
	Destination COM Setting(19)	
	Set/Get serial channel access	**Set/Get Channel Access (06, 40/41)**
	MUX Switch Control	**Set Serial/modem MUX (0C, 12)**
System/Chassis boot control	/	**Get/Set System Boot Options (00, 08/09)**

CHAPTER 3. CUSTOMERS FEATURES

3.1.CUSTOMERS' FEATURE SUPPORT LIST

Table 3-1 Customers' Features

Items	Functions	Supported	Remark
Document:			
1			

3.2.BMC FIRMWARE NAMING

The BMC firmware name can be discovered by using the mandatory Get Device ID command and shown on WebUI.

Detail data is shown in **Appendix G.** For the Twins platform, the auxiliary firmware revision is shown below.

Table 3-2 Auxiliary firmware revision for the Twins platform

Phase	Auxiliary firmware revision
EVT	0xE6142**2**51D
DVT	0xE6142**2**51D
PVT	0xE6142**2**51D
Production	0xE6142**2**51D
Maintenance	0xE6142**2**51D

APPENDIX A IBMC HARDWRE: AST2500

AST2500 is the 6th generation of Integrated Remote Management Processor introduced by ASPEED Technology Inc. Its a vastly integrated SOC device playing as a service processor to support various functions required for highly manageable server platforms. Instead of supporting PCI bus, AST2500 is designed to dedicatedly support PCIE Gen2 1x bus interface, which can make PCB layout simpler and fit systems that are going without PCI bus support. The chip architecture is showed below:

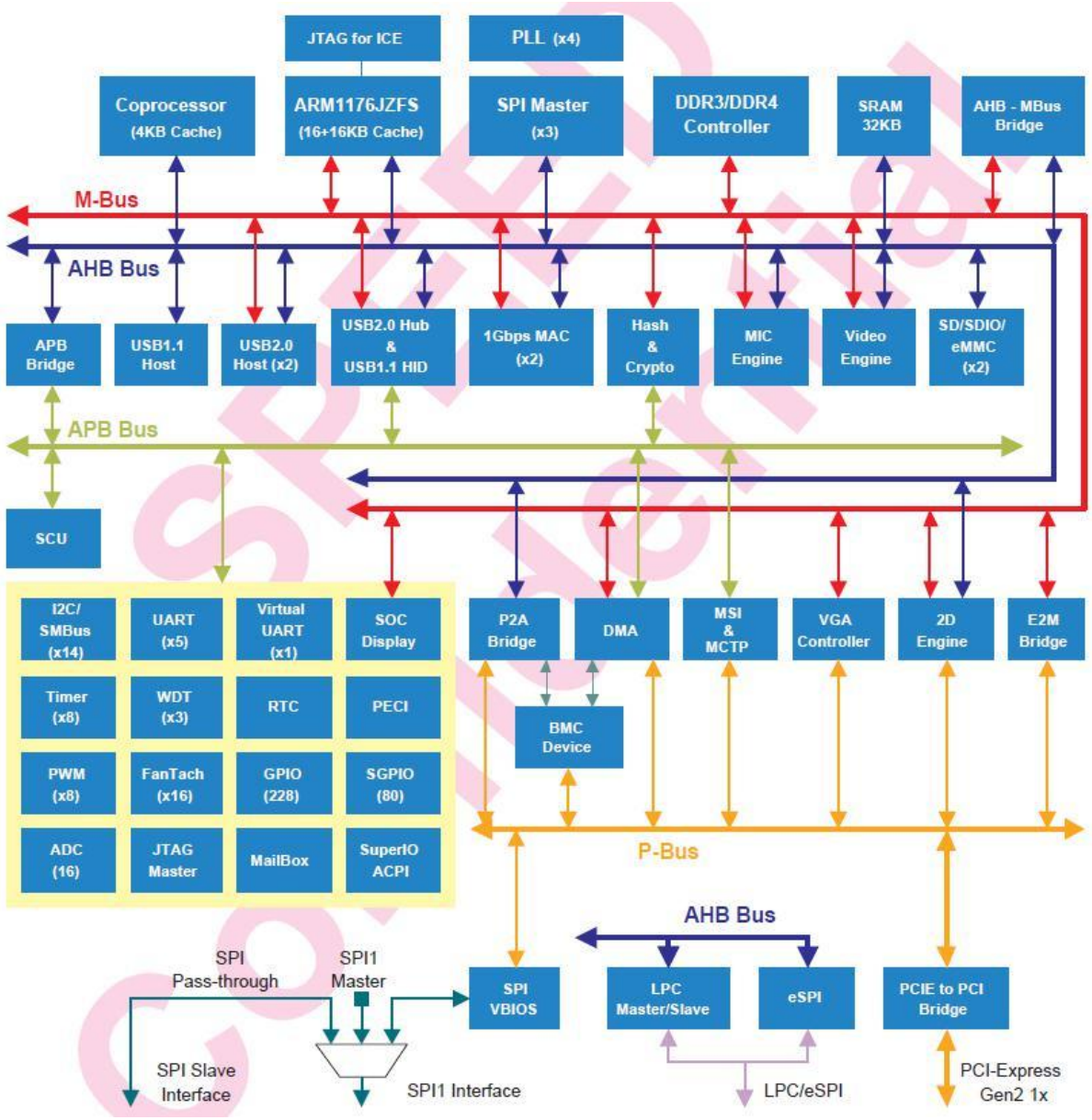

Figure A-1 AST2500 Chip architecture

The following list is a summary of the IBMC management hardware features utilized by the IBMC:

- 800-MHz ARM1176JZF-S 32-bit RISC CPU

- Embedded one more 32-bit Coprocessor RISC CPU except the ARM. Max. 200MHz.
- Built-in PCIE 2.0 Bridge Controller & PCIe Gen 2 PHY
- Built-in PCI-Express 2.0 Root Complex or End Point Controller & PCI-Express Gen 2 PHY
- VGA Display Controller
- Graphics Display Controller
- Video Compression Engine
- Two 10/100/1000 Ethernet controllers with NC-SI support
- 16-bit DDR3L/DDR4 800MHz interface
- 36KB internal SRAM
- System Control Unit
- AHB controller
- Interrupt Controller
- Firmware SPI Memory Controller
- SPI Master Controller
- SD/SDIO/eMMC Host controller
- USB2.0 Vitual Hub Controller
- 64-bit 2D Graphics Accelerator
- 14 sets of multi-function I2C/SMBus bus controller
- Support up to 228 GPIO pins
- Support up to 80 SGPIO input ports
- Slave serial GPIO monitor
- 16 fan tachometers
- 8 PWMs
- KCS interface
- 5 sets of 16550 UART controllers. 921.K baud-rate. Support Hardware UART debug
- Built-in 8 sets of 32-bit timer modules
- 2 sets of USB 2.0 for keyboard, mouse, and storage devices
- 3 sets of 32-bit Watchdog timer
- 64 bytes Battery backed SRAM
- LPC Bus Interface
- eSPI interface
- System SPI Flash Controller
- Super I/O controller
- Hash & Crypto Engine
- Memory Integrity Check(MIC)Engine
- 16 sets of 10 bits ADC channel pins

- Intel PECI 3.1 Compliant
- JTAG master
- MCTP controller
- MSI controller
- X-DMA controller

The more information can refer to the Datasheet of AST2500.

APPENDIX B IPMI COMMANDS SUPPORT TABLE

All option commands and all option parameters of mandatory commands in the command list below are not insured for supporting. Some mandatory commands may be not supported according to FW PRD.

Command	NetFn	CMD	M/O	Supported	Comments
IPMI Device "Global" Commands					
Get Device ID	App	01h	M	V	
Broadcast 'Get Device ID'[1]	App	01h	M		
Cold Reset	App	02h	O	V	
Warm Reset	App	03h	O	V	
Get Self Test Results	App	04h	M	V	
Manufacturing Test On	App	05h	O	V	need password
Set ACPI Power State	App	06h	O	V	
Get ACPI Power State	App	07h	O	V	
Get Device GUID	App	08h	O	V	
Get NetFn Support	App	09h	O	V	
Get Command Support	App	0Ah	O	V	
Get Command Sub-function Support	App	0Bh	O	V	
Get Configurable Commands	App	0Ch	O	V	
Get Configurable Command Sub-functions	App	0Dh	O	V	
Set Command Enables	App	60h	O		
Get Command Enables	App	61h	O	V	
Set Command Sub-function Enables	App	62h	O		
Get Command Sub-function Enables	App	63h	O		
Get OEM NetFn IANA Support	App	64h	O	V	
BMC Watchdog Timer Commands					
Reset Watchdog Timer	App	22h	M	V	
Set Watchdog Timer	App	24h	M	V	
Get Watchdog Timer	App	25h	M	V	
BMC Device and Messaging Commands					
Set BMC Global Enables	App	2Eh	M	V	"Only Supported: SEL Logging Enable / Disable, Event message buffer Enable/disable"
Get BMC Global Enables	App	2Fh	M	V	
Clear Message Flags	App	30h	M	V	
Get Message Flags	App	31h	M	V	
Enable Message Channel Receive	App	32h	O	V	
Get Message	App	33h	M	V	
Send Message	App	34h	M	V	not support Send Raw
Read Event Message Buffer	App	35h	O	V	
Get BT Interface Capabilities	App	36h	O	V	
Get System GUID	App	37h	O	V	
Get Channel Authentication Capabilities	App	38h	O	V	
Get Session Challenge	App	39h	O	V	
Activate Session	App	3Ah	O	V	
Set Session Privilege Level	App	3Bh	O	V	
Close Session	App	3Ch	O	V	
Get Session Info	App	3Dh	O	V	
Get AuthCode	App	3Fh	O	V	
Set Channel Access	App	40h	M	V	"Only support: disabled, always availible, shared mode"
Get Channel Access	App	41h	M	V	

Get Channel Info Command	App	42h	O	V	
Set User Access Command	App	43h	O	V	Not support user session limit
Get User Access Command	App	44h	O	V	
Set User Name	App	45h	O	V	
Get User Name Command	App	46h	O	V	
Set User Password Command	App	47h	O	V	
Activate Payload	App	48h	O	V	
Deactivate Payload	App	49h	O	V	
Get Payload Activation Status	App	4Ah	O	V	
Get Payload Instance Info	App	4Bh	O	V	
Set User Payload Access	App	4Ch	O	V	
Get User Payload Access	App	4Dh	O	V	
Get Channel Payload Support	App	4Eh	O	V	
Get Channel Payload Version	App	4Fh	O	V	
Get Channel OEM Payload Info	App	50h	O	V	
Master Write-Read	App	52h	M	V	
Get Channel Cipher Suites	App	54h	O	V	
Suspend/Resume Payload Encryption	App	55h	O	V	
Set Channel Security Keys	App	56h	O	V	
Get System Interface Capabilities	App	57h	O	V	Only 01h(KCS) is supported
Set System Info Parameters	App	58h	O	V	
Get System Info Parameters	App	59h	O	V	
Chassis Device Commands					
Get Chassis Capabilities	Chassis	00h	M	V	
Get Chassis Status	Chassis	01h	M	V	
ChassisControl	Chassis	02h	M	V	
Chassis Reset	Chassis	03h	O		This command is combined to Chassis Control command in IPMI v1.5
Chassis Identify	Chassis	04h	O	V	
Set Chassis Capabilities	Chassis	05h	O	V	
Set Power Restore Policy	Chassis	06h	O		
Get System Restart Cause	Chassis	07h	O	V	Only 01h (cycle,hardware reset), 04h,8h,9h supported
Set System Boot Options	Chassis	08h	O	V	
Get System Boot Options	Chassis	09h	O	V	
Set Front Panel Button Enables	Chassis	0Ah	O		
Set Power Cycle Interval	Chassis	0Bh	O	V	
Get POH Counter	Chassis	0Fh	O	V	
Event Commands					
Set Event Receiver	S/E	00h	M	V	
Get Event Receiver	S/E	01h	M	V	
Platform Event (a.k.a. “Event Message”)	S/E	02h	M	V	
PEF and Alerting Commands					
Get PEF Capabilities	S/E	10h	M	V	
Arm PEF Postpone Timer	S/E	11h	M	V	
Set PEF Configuration Parameters	S/E	12h	M	V	Does not support parameter 15.
Get PEF Configuration Parameters	S/E	13h	M	V	Does not support parameter 15.
Set Last Processed Event ID	S/E	14h	M	V	
Get Last Processed Event ID	S/E	15h	M	V	
Alert Immediate	S/E	16h	O	V	
PET Acknowledge	S/E	17h	O	V	
Sensor Device Commands					
Get Device SDR Info	S/E	20h	O	V	
Get Device SDR	S/E	21h	O	V	
Reserve Device SDR Repository	S/E	22h	O	V	

Get Sensor Reading Factors	S/E	23h	O	V	Support linear sensors only.
Set Sensor Hysteresis	S/E	24h	O	V	
Get Sensor Hysteresis	S/E	25h	O	V	
Set Sensor Threshold	S/E	26h	O	V	
Get Sensor Threshold	S/E	27h	O	V	
Set Sensor Event Enable	S/E	28h	O	V	
Get Sensor Event Enable	S/E	29h	O	V	
Re-arm Sensor Events	S/E	2Ah	O	V	
Get Sensor Event Status	S/E	2Bh	O	V	
Get Sensor Reading	S/E	2Dh	M	V	
Set Sensor Type	S/E	2Eh	O	V	
Get Sensor Type	S/E	2Fh	O	V	
Set Sensor Reading and Event Status	S/E	30h	O	V	Sensor should be settable (just for FW engineer debug purpose internally)
FRU Device Commands					
Get FRU Inventory Area Info	Storage	10h	M	V	
Read FRU Data	Storage	11h	M	V	
Write FRU Data	Storage	12h	M	V	
SDR Device Commands					
Get SDR Repository Info	Storage	20h	M	V	
Get SDR Repository Allocation	Storage	21h	O	V	
Reserve SDR Repository	Storage	22h	M	V	
Get SDR	Storage	23h	M	V	
Add SDR	Storage	24h	O	V	
Partial Add SDR	Storage	25h	M	V	
Delete SDR	Storage	26h	O		
Clear SDR Repository	Storage	27h	M	V	
Get SDR Repository Time	Storage	28h	O	V	
Set SDR Repository Time	Storage	29h	O		
Enter SDR Repository Update	Storage	2Ah	O		
Exit SDR Repository Update	Storage	2Bh	O		
Run Initialization Agent	Storage	2Ch	O	V	
SEL Device Commands					
Get SEL Info	Storage	40h	M	V	
Get SEL Allocation Info	Storage	41h	O	V	
Reserve SEL	Storage	42h	O	V	
Get SEL Entry	Storage	43h	M	V	
Add SEL Entry	Storage	44h	M	V	
Partial Add SEL Entry	Storage	45h	O	V	
Delete SEL Entry	Storage	46h	O	V	
Clear SEL	Storage	47h	M	V	
Get SEL Time	Storage	48h	M	V	
Set SEL Time	Storage	49h	M	V	
Get Auxiliary Log Status	Storage	5Ah	O		
Set Auxiliary Log Status	Storage	5Bh	O		
Get SEL Time UTC Offset	Storage	5Ch	O	V	
Set SEL Time UTC Offset	Storage	5Dh	O	V	
LAN Device Commands					
Set LAN Configuration Parameter	Transport	01h	M	V	param #9, 25 are not support
Get LAN Configuration Parameters	Transport	02h	M	V	param #9, 25 are not support
Suspend BMC ARPs	Transport	03h	O	V	
Get IP/UDP/RMCP Statistics	Transport	04h	O		
Serial/Modem Device Commands					
Set Serial/Modem Configuration	Transport	10h	M	V	
Get Serial/Modem Configuration	Transport	11h	M	V	
Set Serial/Modem Mux	Transport	12h	O	V	
Get TAP Response Codes	Transport	13h	O		

Set PPP UDP Proxy Transmit	Transport	14h	O		
Get PPP UDP Proxy Transmit	Transport	15h	O		
Send PPP UDP Proxy Packet	Transport	16h	O		
Get PPP UDP Proxy Receive	Transport	17h	O		
Callback	Transport	19h	O		
Set User Callback Options	Transport	1Ah	O		
Get User Callback Options	Transport	1Bh	O		
Set Serial Routing Mux Command	Transport	1Ch	O		
SOL Activating	Transport	20h	O		
Set SOL Configuration Parameters	Transport	21h	O	V	param #7 is not support
Get SOL Configuration Parameters	Transport	22h	O	V	param #7 is not support
Command Forwarding Commands					
Forwarded Command	Transport	30h	O		
Set Forwarded Commands	Transport	31h	O		
Get Forwarded Commands	Transport	32h	O		
Enable Forwarded Commands	Transport	33h	O		
Bridge Management Commands					
Get Bridge State	Bridge	00h	O		
Set Bridge State	Bridge	01h	O		
Get ICMB Address	Bridge	02h	O		
Set ICMB Address	Bridge	03h	O		
Set Bridge ProxyAddress	Bridge	04h	O		
Get Bridge Statistics	Bridge	05h	O		
Get ICMB Capabilities	Bridge	06h	O		
Clear Bridge Statistics	Bridge	08h	O		
Get Bridge Proxy Address	Bridge	09h	O		
Get ICMB Connector Info	Bridge	0Ah	O		
Get ICMB Connection ID	Bridge	0Bh	O		
Send ICMB Connection ID	Bridge	0Ch	O		
Discovery Commands (ICMB)					
PrepareForDiscovery	Bridge	10h	O		
GetAddresses	Bridge	11h	O		
SetDiscovered	Bridge	12h	O		
GetChassisDeviceId	Bridge	13h	O		
SetChassisDeviceId	Bridge	14h	O		
Bridging Commands (ICMB)					
BridgeRequest	Bridge	20h	O		
BridgeMessage	Bridge	21h	O		
Event Commands (ICMB)					
GetEventCount	Bridge	30h	O		
SetEventDestination	Bridge	31h	O		
SetEventReceptionState	Bridge	32h	O		
SendICMBEventMessage	Bridge	33h	O		
GetEventDestination (optional)	Bridge	34h	O		
GetEventReceptionState (optional)	Bridge	35h	O		
Other Bridge Commands					
Error Report (optional)	Bridge	FFh	O		
OEM Commands for Bridge NetFn					
OEM Commands	Bridge	C0h-FEh	O		

APPENDIX C IPMI OEM COMMANDS LIST

NetFun	CMD	Data Length	Request Data	Response Data	function Description
0x2e	0x82	120	Data1 ~ Data120: 120 bytes BIOS configuration data (as Appendix F)	1: Completion Code	Set BIOS Configuration
0x2e	0x83	0	NA	1: Completion Code 2 ~ 57: 56 bytes BIOS configuration data (as Appendix F)	Get BIOS Configuration
0x2e	0x84	0	NA	1: Completion Code 2: BIOS Configuration status. 0: Not Present 1: Sync to BIOS 2; Sync to Customer	Get BIOS Configuration Status
0x2e	0x85	8	Data1 = Data2 = Data3 = Data4 = Data5 = Data6 = Data7 = Data8 = 0x30	1: Completion Code	Set BIOS Configuration Lock
0x2e	0x81	2	Data1-0x00 Data2 set network interface 0x00 - PCH 0x01 - OCP	1: Completion Code Network will set as Normal mode with Port 1	Switch Network interface
0x2e	0x81	4	Data1-0x01 Data2-0X00 Data 3- 0x00 Data 4	1: Completion Code Auto mode ı network changed as OCP and Port 1	Setting network mode and port

			set network port 0x00 ı Port 1 0x01 ı Port 2 0x02 ı Port 3 0x03 ı Port 4		
~~0x2e~~	~~0x81~~	~~3~~	~~Data1-0x02~~ ~~Data2~~ ~~set network interface~~ ~~0x00 - OCP~~ ~~0x01 - PCH~~ ~~Data 3~~ ~~set network port~~ ~~0x00 ı Port 1~~ ~~0x01 ı Port 2~~ ~~0x02 ı Port 3~~ ~~0x03 ı Port 4~~	~~1: Completion Code~~ ~~2: interface~~ ~~3: port~~ ~~4: Status~~ ~~0x00 ı Link Down~~ ~~0x01 ı Link Up~~ ~~0x02 ı Unknown~~ ~~5: 0x00~~ ~~6: 0x01~~ ~~7: 0x02~~ ~~8: 0x03~~ ~~9: 0x04~~ ~~10: 0x05~~	~~Display link status~~
0x2e	0x81	4	Data1-0x03 Data2 set network option 0x00 - Normal mode 0x01 - Failover mode 0x02 - Auto mode Data3 set network interface 0x00 - OCP 0x01 - PCH Data4 set network port 0x00 ı Port 1	1: Completion Code	Network management

			~~0x01 ：Port 2~~ ~~0x02 ：Port 3~~ ~~0x03 ：Port 4~~		
0x2e	0x96	0	NA	1: Completion Code 2: PSU power 3: PSU power	Get PSU total power
0x2e	0x60	0	NA	1: Completion Code	手动截屏 wget https://<BMC IP>/manual_ capture.jpeg --no-check-certificate
0x2e	0x61	0	NA	1.Completion code	自动截屏 wget https://<BMC IP>/auto_ capture.jpeg --no-check-certificate
0x2e	0x41	2	Data1:0x00 Data2:PWM duty	1.Completion Code	手动设置风扇转速。
~~0x2e~~	~~0x31~~	~~5~~	~~Data1:~~ ~~0x05-serial info~~ ~~Data2-5:~~ ~~tftp IP~~	~~1.Completion Code~~	~~Down Serial Info file~~
~~0x2e~~	~~0x31~~	~~5~~	~~Data1:~~ ~~0x06-storelibinfo~~ ~~Data2-5:~~ ~~tftp IP~~	~~1.Completion Code~~	~~Down storelib Info file~~

0x2e	0x93	1	Data1: 0x00-disable serial session 0x01-enable serial session	1.Completion Code	StartStopSerialSession
0x2E	0x95	0	NA	1. Completion Code	Update PSU/DIMM FRU information
0x2E	0x96	0	NA	1. Completion Code 2. HOST NAME data length 3~N. HOST NAME data ASCII value	Get HOST NAME content
0x2E	0xB0	0	NA	1.Completion Code 2. BIOS SETUP Status 0 – No data 1 – No change 2 – changed 3:18 Table Version 19:22 Item Table checksum 23:26 Item Table timestamp 27:30 Partial Table timestamp	Get BIOS SETUP Status
0x2E	0xB1	N	Byte Data field 1:4 Offset 5:6 Data Length - MAX: 0x5000 (20K) - LS Byte First 7:N Data	Byte Data field 1 Completion Code	Set BIOS SETUP Data

0x2E	0xB2	N	Byte Data field 1 Data Type - 0 = Item Table - 1 = Option Table - 2 = String Table - 3 = Partial Table 2:5 Offset 6:N Data Length - MAX: 0x5000 (20K) - LS Byte First	Byte Data field 1 Completion Code 2:N Data	Get BIOS SETUP Data
0x2e	0xB5	0	NA	1.Completion Code 2.Update BIOS fw status 0x00-Normal 0x01-Asynchronous update waiting power off update FW 0x02-Upgrade FW 0x03-Finish update FW, waiting power on check FW version 0x04-Synchronization update waiting click start flash button in web. 0xff-Unkown status	Get BIOS FW update status
0x2e	0x96	1	Data1: 0x00-disable serial session 0x01-enable serial session	1. Completion Code	StartStopSerialSession
0x2e	0x93	NA	NA	1 Completion code	SetUserDefault
0x2e	0x97	2	Data1:0x01 Data2: 0x00-disable 0x01-enable	1 Completion code	Enable/Disable SNMP Trap

0x2e	0x0B	1	Data1: 0x00- Active-Active 0x01-Active-Standy	1 Completion code	SetPSUMode
0x2e	0x97	2	Data1:0x00 Data2: Lan Destination 1~15 Data3~N:Domain name ASCII	1 Completion code	Set SNMP destination domain name
0x2e	0x97	3	Data1:0x02 Data2:0x6f Data3: 0x6e- on 0x60-off	1 Completion code	Disable and Enable SNMP service
0x2e	0x94	2	Data1: 0x00-disable 0x01-enable Data2: Port Num Note: only disable and enable，port num is 00	1 Completion code	Set DHCP Client Port

APPENDIX D FRU DATA

D.1.FRU DATA TEMPLATE

For Example:

FRU Device Description: Builtin FRU Device (ID 0)
Chassis Type : Rack Mount Chassis
Chassis Part Number : 1A215K100-600-G
Chassis Serial : xxxx
Chassis Extra : .....
Chassis Extra : .....
Board Mfg Date : Thu Jun 13 09:10:00 2017
Board Mfg : FOXCONN
Board Product : TWINS
Board Serial : xxxx
Board Part Number : 1A2152S00-600-G
Product Manufacturer : FOXCONN
Product Name : TWINS
Product Part Number : 1A215K100-600-G
Product Version : C1
Product Serial : xxxx
Product Asset Tag : 7654321

D.2FRU BYTE DEFINITION

Area	item	Field Name	Offset	Length	Value	Description/Rule
Common Header (Base=0x00)	1	Comm Ver	0x00	0x01	0x01	
	2	Internal Use offset	0x01	0x01	0x00	00h - indicate that this area does not exist
	3	Chassis Info offset	0x02	0x01	0x01	corresponding area starting offset (in multiples of 8 bytes)
	4	Board Info offset	0x03	0x01	0x12	corresponding area starting offset (in multiples of 8 bytes)
	5	Product Info offset	0x04	0x01	0x27	corresponding area starting offset (in multiples of 8 bytes)
	6	MultiRecord area offset	0x05	0x01	0x00	00h - indicate that this area does not

						exist
	7	PAD	0x06	0x01	0x00	00h - any remaining unused space
	8	Checksum	0x07	0x01	0xC5	after updating the field above,utility should compute and update the checksum
Chassis Info (Base=0x08)	1	Version	0x08	0x01	0x01	Chassis Info Area Format Version Bit Fields
	2	Area length	0x09	0x01	0x11	Chassis Info Area Length (in multiples of 8 bytes)
	3	Chassis Type	0x0A	0x01	17h	Option value(01h-17h) 02h - Unknown 07h - Tower 17h- Rack Mount Chassis (01h ~ 17h) refer to "IPMI-Platform Management FRU Information Storage Definition"
	4	Chassis Part Number Type/Length	0x0B	0x01	0xDE	
	5	Chassis Part Number String	0x0C	0x1E	1A215K 100-600-G	Reserve size: 30 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	6	Chassis Serial Number Type/Length	0x2A	0x01	0xDE	
	7	Chassis Serial Number String	0x2B	0x1E	XXXX	Reserve size: 30 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	8	Chassis Extra 1 UUID Type/Length	0x49	0x01	0xE0	
	9	Chassis Extra 1 UUID String	0x4A	0x20	XXXX	Reserve size: 32 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	10	Custom information	0x6A	0x01	0xE0	

		Type/Length				
	11	Custom information	0x6B	0x20	0xFF	Reserve size: 32 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	12	End of Field Marker	0x8B	0x01	0xC1	
	13	PAD	0x8C	0x03	0x000000	
	14	Checksum	0x8F	0x01		after updating the field above,utility should compute and update the checksum
Board Info (Base=0x90)	1	Version	0x90	0x01	0X01	Board Info Area Format Version Bit Fields
	2	Area Length	0x91	0x01	0x15	Board Info Area Length (in multiples of 8 bytes)
	3	Board Info Language Code	0x92	0x01	00h	00h - English Refer to "IPMI-Platform Management FRU Information Storage Definition"
	4	Manufacturing Date/Time	0x93	0x03	XXXX	Number of minutes from 0:00 hrs 1/1/96. LSbyte first (little endian)
	5	Board Manufacturer Type/Length	0x96	0x01	0xD4	
	6	Board Manufacturer String	0x97	0x14	FOXCONN	Reserve size: 20 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	7	Board Product Name Type/Length	0xAB	0x01	0xD4	
	8	Board Product Name String	0xAC	0x14	TWINS	Reserve size: 20 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	9	Board Serial Number Type/Length	0xC0	0x01	0xDE	
	10	Board Serial Number String	0xC1	0x1E	XXXX	Reserve size: 30 Byte Left-aligned, right pad with NULL(0x00)

						if actual content size is less than reserved size
	11	Board Part Number Type/Length	0xDF	0x01	0xDE	
	12	Board Part Number String	0xE0	0x1E	1A2152 S00-600-G	Reserve size: 30 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	13	FRU File ID Type/Length	0xFE	0x01	0xD4	
	14	FRU File ID String	0xFF	0x14	FRU Ver 0.01	FRU content version, controled by project (Example: X.XX start from 0.01, 0.02 …) Reserve size: 20 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	15	Custom information Type/Length	0x113	0x01	0xE0	
	16	Custom information	0x114	0x20	0xFF	Reserve size: 32 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
	17	End of Field Marker	0x134	0x01	0xC1	
	18	PAD	0x135	0x02	0x0000	00h - any remaining unused space
	19	Checksum	0x137	0x01		after updating the field above,utility should compute and update the checksum
Product Info (Base=0x138)	1	Version	0x138	0x01	0x01	Product Info Area Format Version Bit Fields
	2	Area Length	0x139	0x01	0x24	Product Info Area Length (in multiples of 8 bytes)
	3	Product Info Language code	0x13A	0x01	00h	Option value 00h - English Refer to "IPMI-Platform Management FRU Information Storage Definition"

4	Manufacturer Name Type/Length	0x13B	0x01	0xD4	
5	Manufacturer Name String	0x13C	0x14	FOXCONN	Reserve size: 20 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
6	Product Name Type/Length	0x150	0x01	0xD4	
7	Product Name String	0x151	0x14	TWINS	Reserve size: 20 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
8	Part/Model Number Type/Length	0x165	0x01	0xDE	
9	Part/Model Number String	0x166	0x1E	1A215K 100-600-G	Reserve size: 30 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
10	Product Version Type/Length	0x184	0x01	0xD4	
11	Product Version String	0x185	0x14	Ver 0.01	Reserve size: 20 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
12	Product Serial Number Type/Length	0x199	0x01	0xDE	
13	Product Serial Number String	0x19A	0x1E	XXXX	Reserve size: 30 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
14	Asset Tag Type/Length	0x1B8	0x01	0XDE	
15	Asset Tag String	0x1B9	0x1E	XXXX	Reserve size: 30 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
16	FRU File ID Type/Length	0x1D7	0x01	0xD4	
17	FRU File ID String	0x1D8	0x14	FRU Ver 0.01	Reserve size: 20 Byte Left-aligned, right pad with NULL(0x00)

					if actual content size is less than reserved size
18	Product Extra Rack ID Type/Length	0x1EC	0x01	0xE0	
19	Product Extra Rack ID String	0x1ED	0x20	0xFF	Reserve size: 32 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
20	Product Extra Node ID Type/Length	0x20D	0x01	0xE0	
21	Product Extra Node ID String	0x20E	0x20	0xFF	Reserve size: 32 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
22	Custom information Type/Length	0x22E	0x01	0xE0	
23	Custom information	0x22F	0x20	0xFF	Foxconn template version (format) XX start from 01,02 ... Reserve size: 32 Byte Left-aligned, right pad with NULL(0x00) if actual content size is less than reserved size
24	End of Field Marker	0x24F	0x01	0xC1	
25	PAD	0x250	0x07	0x00000000000000	00h - any remaining unused space
26	Checksum	0x257	0x01		after updating the field above,utility should compute and update the checksum

Remark:

White	"Value" field marked with white color, the value is fixed, never to change if template format is not changed.
Yellow	"Value" field marked with yellow color, the value dependent on project.
Green	"Value" field marked with green color, the value will be computed and updated by utility

APPENDIX E SENSOR TABLE

IPMI provides a sixteen byte string identifier (Sensor ID) in each SDR. This ASCII based string will need to be interpreted by system management software (SMS) for display and alerting purposes. Sensors provided by BMC are listed in the following Table E-1

Table E-1 Analog Sensor

Sensor Number	Power State	Sensor String	Sensor Type	Reading Type	LNR	LC	LNC	UNC	UC	UNR	SEL Logged Assert/ De-assert	Remark
0x01	Not S5	CPU0_Temp	01h	01h							NA	
0x02	Not S5	CPU1_Temp	01h	01h							NA	
0x03	Not S5	CPU0_Margin_Temp	01h	01h		1	2				As and De	
0x04	Not S5	CPU1_Margin_Temp	01h	01h		1	2				As and De	
0x05	Not S5	DIMMG0_Temp	01h	01h				90	95		As and De	
0x06	Not S5	DIMMG1_Temp	01h	01h				90	95		As and De	
0x07	Not S5	PCH_Temp	01h	01h				90	95		As and De	
0x08	S Any	Inlet_Temp	01h	01h				42	46		As and De	
0x09	S Any	Outlet_Temp	01h	01h				70			NA	
0x17	Not S5	FPIO_CONN_Temp	01h	01h					**74**		As and De	
0x18	Not S5	Front_BP_Temp	01h	01h					**74**		As and De	
0x19	Not S5	Rear_BP_Temp	01h	01h					**74**		As and De	
0x1B	Not S5	PS1_Temp	01h	01h							NA	
0x1C	Not S5	PS2_Temp	01h	01h							NA	
0x1D	S Any	PS1_Ambient_Temp	01h	01h				65			NA	
0x1E	S Any	PS2_Ambient_Temp	01h	01h				65			NA	
0x20	Not S5	P3V3	02h	01h		3.118			**3.505**		As and De	
0x21	Not S5	P5V	02h	01h		4.464			**5.544**		As and De	
0x22	Not S5	P12V	02h	01h		10.752			13.356		As and De	
0x25	Not S5	P12V_STBY	02h	01h		10.752			13.356		As and De	
0x29	S Any	BAT_P3V	02h	01h		2.716			3.500		As and De	
0x3C	Not S5	PS1_Voltage	02h	01h		10			13		As and De	
0x3D	Not S5	PS2_Voltage	02h	01h		10			13		As and De	
0x48	Not S5	PS1_Current	03h	01h							NA	
0x49	Not S5	PS2_Current	03h	01h							NA	
0x58	S Any	Total_Power	0Bh	01h							NA	
0x59	Not S5	CPU0_VR_Pout	0Bh	01h							NA	

0x5A	Not S5	CPU1_VR_Pout	0Bh	01h							NA	
0x5B	Not S5	CPU0_ABC_VR_Pout	0Bh	01h							NA	
0x5C	Not S5	CPU0_DEF_VR_Pout	0Bh	01h							NA	
0x5D	Not S5	CPU1_ABC_VR_Pout	0Bh	01h							NA	
0x5E	Not S5	CPU1_DEF_VR_Pout	0Bh	01h							NA	
0x65	Not S5	PS1_IN_PWR	0Bh	01h							NA	
0x67	Not S5	PS2_IN_PWR	0Bh	01h							NA	
0x70	Not S5	FAN1_RPM	04h	01h		2656					As and De	
0x71	Not S5	FAN2_RPM	04h	01h		2656					As and De	
0x72	Not S5	FAN3_RPM	04h	01h		2656					As and De	
0x73	Not S5	FAN4_RPM	04h	01h		2656					As and De	
0x74	Not S5	FAN5_RPM	04h	01h		2656					As and De	
0x75	Not S5	FAN6_RPM	04h	01h		2656					As and De	
~~0x80~~	~~Not S5~~	~~Riser1_Temp~~	~~01h~~	~~01h~~					~~74~~		~~As and De~~	
~~0x81~~	~~Not S5~~	~~Riser2_Temp~~	~~01h~~	~~01h~~					~~74~~		~~As and De~~	
0x82	Not S5	Riser3_Temp	01h	01h					74		As and De	
0x8B	Not S5	OCP_LAN_Temp	01h	01h					74		As and De	
~~0x92~~	~~Not S5~~	~~Front_HDD_Temp~~	~~01h~~	~~01h~~					~~74~~		~~As and De~~	~~For Skew2/4~~
0x93	Not S5	Rear_HDD1_Temp	01h	01h					74		As and De	
0x94	Not S5	Rear_HDD2_Temp	01h	01h					74		As and De	
0x8C	Not S5	PCIE1_HBA_CTL	01h	01h				110	115		As and De	
~~0x96~~	~~Not S5~~	~~BBU_Temp~~	~~01h~~	~~01h~~				~~100~~	~~110~~		~~As and De~~	
~~0x97~~	~~Not S5~~	~~BBU_Vol~~	~~01h~~	~~01h~~							~~As and De~~	
0xCF	Not S5	PCIE_GPU0_Temp	01h	01h					85		As and De	
0xCE	Not S5	PCIE_GPU1_Temp	01h	01h					85		As and De	
0xD1	Not S5	PCIE_GPU2_Temp	01h	01h					85		As and De	
0xD0	Not S5	PCIE_GPU4_Temp	01h	01h					85		As and De	
0xD3	Not S5	PCIE_LAN0_Temp	01h	01h				100	105		As and De	
0xD4	Not S5	PCIE_LAN1_Temp	01h	01h				100	105		As and De	
0xD6	Not S5	PCIE_LAN2_Temp	01h	01h				100	105		As and De	
0xD5	Not S5	PCIE_LAN4_Temp	01h	01h				100	105		As and De	
0xD2	Not S5	PCIE_LAN3_Temp	01h	01h				100	105		As and De	
0x8A	Not S5	OCP Chip Temp	01h	01h				100	105		As and De	

Table E-2 Discrete Sensors

Sensor Number	Power State	Sensor Name	Sensor Type	Reading Type	Sensor offset	Event Data1	Event Data2	Event Data3	SEL Logged Assert/ De-assert	Remark
0xA0	Not S5	CPU0_Status	07h	6Fh	01h – Thermal Trip	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	0xFF	As	
0xA1	Not S5	CPU1_Status	07h	6Fh	01h – Thermal Trip	[7:6]=00b [5:4]= 00b	0xFF	0xFF	As	

						[3:0] Sensor offse				
0xA2	Not S5	CPU_CATERR	07h	6Fh	00h – IERR 0Ch – Correctable	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	0xFF	As	

					Machine Check Error					
0xA6	S Any	BMC_Boot_Up	16h	09h	01h - Device Enabled	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	0xFF	As	
0xA7	S Any	IPMI_Watchdog	23h	6Fh	00h – Timer Expired 01h – Hard Reset 02h – Power Down 03h – Power Cycle	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	0xFF	As	
0xA8	S Any	SEL_Status	10h	6Fh	02h – Log Area Reset/Cleared 04h – SEL Full 05h – SEL Almost full	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	0xFF	As	
0xA9	Not S5	PS1_Status	08h	6Fh	00h - Presence detected 03h – Power Supply input lost (AC/DC)	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	0xFF	As and De	
0xAA	Not S5	PS2_Status	08h	6Fh	00h - Presence detected 03h – Power Supply input lost (AC/DC)	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	0xFF	As and De	
0xAC	S Any	ACPI_PWR_Status	22h	6Fh	00h – S0 / G0 “working” 06h – S4 / S5 soft-off, particular S4 / S5 state cannot be determined	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	0xFF	As	
0xAD	S Any	Button_Pressed	14h	6Fh	00h – Power button pressed	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	00h = info	As	
0xB1	Not S5	CPU0_Hot	01h	03h	00h – State Deserted 01h – State Asserted	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	40h = warning	As and De	
0xB2	Not S5	CPU1_Hot	01h	03h	00h – State Deserted 01h – State Asserted	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	40h = warning	As and De	
0xB7	Not S5	DIMMG0_1_Hot	0Ch	6Fh	0Ah - Critical Over temperature	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	00h = info	As	
0xB8	Not S5	DIMMG0_2_Hot	0Ch	6Fh	0Ah - Critical Over temperature	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	00h = info	As	
0xB9	Not S5	DIMMG1_1_Hot	0Ch	6Fh	0Ah - Critical Over temperature	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	00h = info	As	
0xBA	Not S5	DIMMG1_2_Hot	0Ch	6Fh	0Ah - Critical Over temperature	[7:6]=00b [5:4]= 00b [3:0] Sensor offse	0xFF	00h = info	As	
0xBD	Not S5	DIMM_Alert	0Ch	03h	01h – State Asserted*	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xBF	Not S5	CPU0_VR_Hot	01h	03h	00h – State Deserted 01h – State Asserted	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xC0	Not S5	CPU1_VR_Hot	01h	03h	00h – State Deserted 01h – State Asserted	[7:6]=00b [5:4]=00b	0xFF	0xFF	As	

						[3:0] Sensor offse				
0xC2	S Any	CPU_Error	07h	03h	01h – State Asserted	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xC3	Not S5	SystemReset	1Dh	03h	01h – State Asserted	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xC4	S Any	PowerFault	09h	03h	01h – State Asserted	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xC6	Not S5	P0_ABC_VRHot	01h	03h	00h – State Deserted 01h – State Asserted	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xC7	Not S5	P0_DEF_VRHot	01h	03h	00h – State Deserted 01h – State Asserted	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xC8	Not S5	P1_ABC_VRHot	01h	03h	00h – State Deserted 01h – State Asserted	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xC9	Not S5	P1_DEF_VRHot	01h	03h	00h – State Deserted 01h – State Asserted	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xCB	S Any	CPU_MSMI	07h	6Fh	00h – IERR 0Ch – Correctable Machine Check Error	[7:6]=00b [5:4]=00b [3:0] Sensor offse	0xFF	0xFF	As	
0xCD	S Any	SystemEvent	12h	6Fh	04h – PEF action	[7:6]=11b [5:4]=00b [3:0] Sensor offse	[5]=1b Diagnostic interrupt [4]=1b OEM Action [3]=1b power cycle [2]=1b reset [1]=1b power off [0]=1b Alert	0xFF	As	

0xDB	S Any	CPU0 A0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	NA	
0XDC	S Any	CPU0 A1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	NA	
0xDD	S Any	CPU0 B0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	NA	
0xDE	S Any	CPU0 B1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	NA	
0xDF	S Any	CPU0 C0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	NA	
0xED	S Any	CPU0 C1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	NA	
0xEE	S Any	CPU0 D0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	NA	
0xEF	S Any	CPU0 D1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit 06h-Presence detected reached	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	NA	

0xF0	S Any	CPU0 E0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	NA	
0xF1	S Any	CPU0 E1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xF2	S Any	CPU0 F0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xF3	S Any	CPU0 F1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xF4	S Any	CPU1 A0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xF5	S Any	CPU1 A1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xF6	S Any	CPU1 B0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xF7	S Any	CPU1 B1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xF8	S Any	CPU1 C0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xF9	S Any	CPU1 C1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]=00b [3:0] Sensor offset	0xFF	0xFF	As and De	

0xFA	S Any	CPU1 D0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xFB	S Any	CPU1 D1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xFC	S Any	CPU1 E0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xFD	S Any	CPU1 E1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xFE	S Any	CPU1 F0	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	As and De	
0xFF	S Any	CPU1 F1	Ch	6fh	01h –Uncorrectable ECC / other uncorrectable memory erro 05h- Correctable ECC / other correctable memory error logging limit reached 06h-Presence detected	[7:6]=00b [5:4]= 00b [3:0] Sensor offset	0xFF	0xFF	As and De	

able E-3 Event Only Sensor

Sensor Number	Power State	Sensor Name	Sensor Type	Reading Type	Sensor offset	Event Data1	Event Data2	Event Data3	SEL Logged Assert/ De-assert	Remark

Table E-4 BIOS Owned Sensor

Sensor Number	Power State	Sensor Name	Sensor Type	Reading Type	Sensor offset	Event Data1	Event Data2	Event Data3	SEL Logged Assert/ De-assert
0xe0	Not S5	BIOS_Boot_Up	1Dh	6Fh	00h – Initiated by power up 02h – Initiated by warm	[7:6]=00b [5:4]= 00b	0xFF	00h = info l	As

					reset	[3:0] Sensor offse			
0xe2	Not S5	Memory_Status	0Ch	6Fh	00h - Correctable ECC/other correctable memory error 01h - uncorrectable ECC/other uncorrectable memory error 04h - Memory Device Disabled	[7-6] = 10b OEM code in byte 2 [1-0] = 00h Correctable ECC/other correctable memory error [1-0] = 01h uncorrectable ECC/other uncorrectable memory error [1-0] = 04h Memory device disabled [1-0] = 05h correctable ECC/other correctable memory error	[7:6] – CPU offset 00b = CPU0 01b = CPU1 [5:3] – channel index [2:0] – offset in given channel	NA	As

						logging limit reached			

[Note]

1. Thresholds for threshold based sensors are noted as shown below.

- UNC = Upper Non-Critical
- UC = Upper Critical
- UNR = Upper Non-Recoverable
- LNC = Lower Non-Critical
- LC = Lower Critical
- LNR = Lower Non-Recoverable
- NR = Non-Redundant

2. Power State Requirement

It represents that the sensor will be probed in what kind of ACPI mode:

a) **"Not S5"** means BMC FW will not probe the sensor when system is powered down.

b) **"S Any"** means BMC FW will probe the sensor in any ACPI power states.

APPENDIX F DEFAULT CONFIGURATION

A host based utility will be available to configure the BMC. This utility can be used to set parameters such as IP address and other LAN parameters, and/or SEL and SDR time. The utilities include BIOS and IPMI utility. The host based utility has high priority to send command to BMC.

Table F-1 Default Configuration (TBD)

Parameter Name	Default Value
User IDs	**(User/Password/Privilege/Channels)**
USER ID 1:	NULL/NULL/User/LAN
USER ID 2:	root/root/Administrator/LAN
LAN Channel	
IP Address Source	DHCP
IP Address	0.0.0.0
Subnet Mask	0.0.0.0
PEF Alerting	Disable
Per-message Authentication	Disable
User Level Authentication	Disable
Access Mode	Always Available
Privilege Level Limit	Administrator
SOL	
SOL Enable	Disable SOL payload
Payload Authentication/Authentication	Force encryption/ Authentication controlled by remote software
SOL Privilege Level Limit	Administrator
SOL non-volatile bit rate	115200 bps
SOL volatile bit rate	115200 bps
IPMB Slave Address	**20h**
KCS Base Address	**CA2h/CA3h for SMS**
Power Restore Policy	chassis always powers up after AC/mains is applied or returns
Power Cycle Interval	**10 Secs**
Maximum Session number	**16**
Maximum user number	**TBD**

APPENDIX G PRODUCT IDENTIFICATION

The BMC firmware name can be discovered by using the mandatory Get Device ID command and shown on WebUI.

Detail data is shown in **Table G.1**.

Table G-1 Product Identification

Field	Offset	Response Data(Hex)
Firmware Revision(Major)	04	Dynamic 00 – 99
Firmware Revision(Minor)	05	Dynamic 00 - 99
Manufacturer ID (LSB first)	08:10	0056DEh
Product ID (LSB first)	11:12	TBD
Auxiliary Firmware Revision	13	Bit[7:4] Server Type Eh = Cloud Line Bit[3:0] Processor 6h = Intel-2P-SkyLake
Auxiliary Firmware Revision	14	Project Tag 14h = Twins
Auxiliary Firmware Revision	15	Bit[7:4] MB Version 1h = EVT 2h = DVT 3h = PVT 4h = Production 5h = Maintenance Bit[3:0] SOC Type 5h = AST2500
Auxiliary Firmware Revision	16	SKU 00h = Foxconn general

APPENDIX H REFERENCES

[1] Intelligent Platform Management Interface Specification v2.0, Rev 1.1, Errata Rev 7, Intel, Hewlett-Packard, NEC, Dell, 2015.

[2] AST2500/AST2520 Integrated Remote Management Processor A2 Datasheet, Rev1.31, ASPEED Technology Inc, 2016.

[3] IPMI Platform Management FRU Information Storage Definition v1.0, Rev1.3, Intel, Hewlett-Packard, NEC, Dell, 2015.

[4] Hawk_Eye_X2_SCH_20161118.pdf

[5] Redfish Scalable Platforms Management API Specification v1.1.0, DPTF, 2016.