

UC20 MUX User Guide

UMTS/HSPA Module Series

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About the Document

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1 Introduction

This document mainly introduces the technical details of Quectel MUX (Multiplexer Protocol) and provides examples on how to develop MUX on devices.





2 The Design Purpose of MUX

As to a non-multiplexer device, it is so inefficient to deal with only one kind or one channel of data steam during a period of time. Therefore, Quectel multiplexer is designed to create 4 virtual channels on a physical port in order to transmit data simultaneously. It looks like four real physical channels for the application. They could operate the logical action on every virtual channel, such as using the SMS service or PPP dialing.

All the data from APP is packed as the frames, and the frames consist of the data and protocol field which clearly indicate the channel No., the length of the information and the FCS and so on. The frames are transmitted as one stream via the serial port. After arriving at the other peer, they are unpacked as four streams by the MUX protocol stack and transmitted to the application. Besides the information data, the control signals are also simulated.

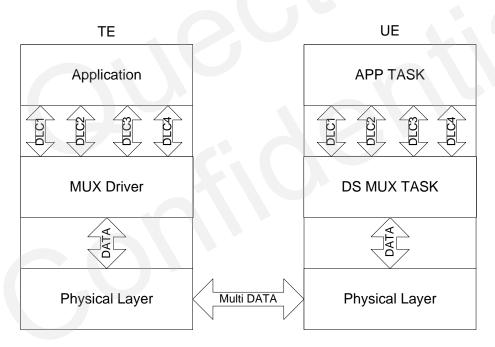


Figure 1: MUX Architecture

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3 MUX AT Command

3.1. AT+CMUX Enable/disable MUX Control Channel

This command is used to enable/disable the MUX control channel. The AT command sets parameters for the control channel. If the parameters are left out, the default value will be used.

AT+CMUX Enable/disable MUX (Control Channel
Test Command AT+CMUX=?	Response +CMUX: (list of supported <mode>)[,(list of supported <subset>)[,(list of supported <portspeed>)[,(list of supported <t1>)[,(list of supported <t1>)[,(list of supported <t2>)[,(list of supported <t2>)[,(list of supported <t2>)[,(list of supported <k2)]]]]]]]]< td=""></k2)]]]]]]]]<></t2></t2></t2></t1></t1></portspeed></subset></mode>
	ок
Read Command AT+CMUX?	Response +CMUX: <mode>[,<subset>[,<portspeed>[,<n1>[,<t1>[,<n2>[,<t2 >[,<t3>[,<k>]]]]]]]] OK</k></t3></t2 </n2></t1></n1></portspeed></subset></mode>
Write Command	Response
AT+CMUX= <mode>[,<subset>[,<port speed="">[,<n1>[,<t1>[,<n2>[,<t2>[,<t3>[,<k>]]]]]]]]</k></t3></t2></n2></t1></n1></port></subset></mode>	ок

Parameter

<mode></mode>	0 Basic option.				
<subset></subset>	This parameter defines the way in which the MUX control channel is set up.				
Virtual channel may subsequently be set up differently, but in the absorber					
	negotiation for the settings of a virtual channel, it shall be set up according to the				
	control channel <subset> setting.</subset>				
	0 UIH frames used only.				
	1 UI frames used only.				

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	2 I frames used only.
<portspeed></portspeed>	1 9600bit/s
	2 19200bit/s
	3 38400bit/s
	4 57600bit/s
	<u>5</u> 115200bit/s
	6 230400bit/s
	7 460800bit/s
<n1></n1>	Maximum frame size, the range is 1-32768, 127 is the default value for basic
	option (see <mode>).</mode>
<t1></t1>	The time UE waits for an acknowledgement before resorting to other action (e.g.
	transmitting a frame). The step size is ten milliseconds, the range is 1-255. The
	default value is 100ms.
<n2></n2>	Maximum number of re-transmissions, the range is 0-255, the default value is 3.
<t2></t2>	Response timer for MUX control channel, the step size is ten milliseconds, the
	range is 2-255, 30 is the default value.
<t3></t3>	Wake up response timer in seconds. The range is 1-255, 10 is the default value.
<k></k>	Window size (It is not supported for UC20).

Example

AT+CMUX=0

OK

AT+CMUX?

+CMUX: 0,0,5,127,10,3,30,10,2

OK

NOTE

AT+CMUX can only be executed on UART1 since UC20 only supports MUX function via UART1.



4 The Multiplexer Protocol

This chapter explains the technical details of the multiplexer protocol.

4.1. Frame Structure

Table 1: MUX Frame Structure

FLAG	Address	Control	Length	Information	FCS	FLAG
1 octet	1 octet	1 octet	1~2 octet	Multiple octets	1 octet	1 octet

4.1.1. Flag Field

Each frame begins and ends with a flag octet (0xF9).

4.1.2. Address Field

Table 2: Address Field

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
EA	C/R	DLCI					

4.1.2.1. EA

EA is always set to 1.

4.1.2.2. C/R

C means the command and R means the response. TE sends a command to the module with C/R=1, and the module responses with C/R=1. The module sends a command with C/R=0, and the TE responses with C/R=0.

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Table 3: C/R

Command/Response	Direction	C/R Value			
Command	TE→UE	1			
Command	UE→TE	1			
Deepense	UE→TE	0			
Response	TE→UE	0			

The DLCI identifies the virtual channel between TE and UE. Multiple DLCIs shall be supported but the number is implementation-specific. The DLCIs are dynamically assigned.

4.1.3. Control Field

Table 4: The Coding of Control Field

Frame Type	HEX (P/F=0)	1	2	3	4	5	6	7	8
SABM (Set Asynchronous Balanced Mode)	0x2F	1	1	1	1	P/F	1	0	0
UA (Unnumbered Acknowledgement)	0x63	1	1	0	0	P/F	1	1	0
DM (Disconnected Mode)	0x0F	1	1	1	1	P/F	0	0	0
DISC (Disconnect)	0x43	1	1	0	0	P/F	0	1	0
UIH (Unnumbered Information with Header Check)	0xEF	1	1	1	1	P/F	1	1	1
UI (Unnumbered)	0x03	1	1	0	0	P/F	0	0	0

P/F is the Poll/Final bit. The poll (P) bit set to 1 shall be used by a station to solicit (poll) a response or sequence of responses from the other station.

The final (F) bit set to 1 shall be used by a station to indicate the response frame transmitted as the result of a soliciting (poll) command.

The poll/final (P/F) bit shall serve a function in both command frames and response frames (In command frames, the P/F bit refers to the P bit. In response frames, it refers to the F bit). Following is detailed rules:

- When DCE sends message frame, P/F is set to 0.
- When DCE receives message frame from DLC0, whose P/F is set to 1, DCE will give priority to response it and set response frame's P/F to 1.
- When DCE sends control frame, P/F is set to 1.



- When DCE sends UIH frame NOT by DLC0, P/F is set to 0.
- DCE only process SABM, DISC frame, whose P/F is set to 1.

4.1.4. Length Field

Table 5: The Structure of Length Field

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
E/A	L1	L2	L3	L4	L5	L6	L7

The L1 to L7 bits indicates the length of the following data field for the information field less than 128.

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
0	L1	L2	L3	L4	L5	L6	L7
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
L8	L9	L10	L11	L12	L13	L14	L15

The range of the length field may be extended using the EA bit. When the EA bit is set to 1 in an octet, it is signifies that this octet is the last octet of the length field. When the EA bit is set to 0, it signifies that a second octet of the length field follows. The total length of the length field is 15 bits in that case.

4.1.5. Information Field

The information field is the payload of the frame and carries the user data and any convergence layer information. The field is octet structured. The information field only presents in I frames, UI frames and UIH frames.

4.1.6. FCS Field

In the case of the UIH frame, the contents of the I-field shall not be included in the FCS calculation. FCS is calculated on the contents of the address, control and length fields only. This means that only the delivery to the correct DLCI is protected, but not the information.

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4.2. Frame Type

4.2.1. SAMB

SABM is command frame and shall be used to establish DLC between TE and MS.

4.2.2. UA

UA frame is the response to SABM or DISC frame. Please refer to following diagram.

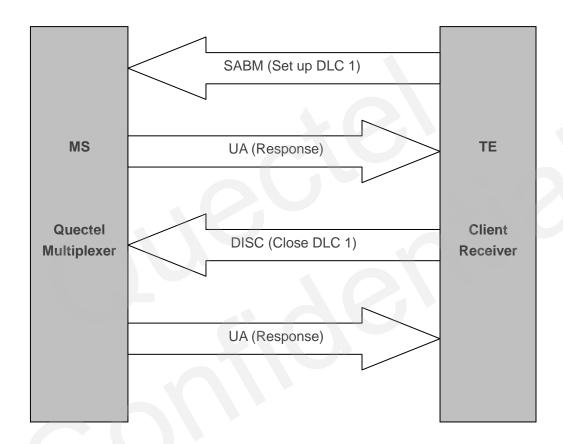


Figure 2: UA Frame (Response)

4.2.3. DISC

DISC is command frame and shall be used to close down DLC. Prior to acting the command, the receiving station shall confirm the acceptance of the DISC command by the transmission of a UA response. Please see the diagram above.



4.2.4. DM

The DM response frame shall be used to report a status whether the station is logically disconnected from the data link. When in disconnected mode, no commands are accepted until the disconnected mode is terminated by the receipt of a SABM command. If a DISC command is received while in disconnected mode, a DM response should be sent.

4.2.5. UIH

The UIH command/response shall be used to send user data at either station.

4.3. Control Channel

At the initiation of communication between the TE and UE, a control channel is set up with DLCI 0. This channel is used to convey information between the two multiplexers.

4.3.1. Message Format

Multiplexer control channel is the basic channel which is used to establish DLC, launch power saving, wake up from power saving and implement flow control mechanism.

Control channel is the first channel established at the initiation of the multiplexer between the TE and MS and it has the DLCI value 0.

UIH message frame is transmitted through control channel. All UIH message frames conform to the following format.

Туре	Length	Value 1	Value 2	 Value n	

Each box in the table represents a field of minimum size in one octet.

The first type field octet has the following format:

1	2	3	4	5	6	7	8
EA	C/R	T1	T2	Т3	T4	T5	T6

The EA bit is an extension bit. It is set to 1 in the last octet of the sequence. In other octets, EA is set to 0. Quectel multiplexer only supports to transmit one octet. So EA is always set to 1.



The C/R bit indicates whether the message is a command or a response.

The T bits indicate the type coding. Each command has a unique pattern of bit sequence. This means that a single-octet type field can encode 63 different message types. Only single octet message types are defined in this document.

The length field octet has the following structure:

1	2	3	4	5	6	7	8
EA	L1	L2	L3	L4	L6	L6	L7

The EA bit is an extension bit. It is set to 1 in the last octet of the sequence. In other octets EA is set to 0. Quectel multiplexer only supports to transmit one octet. So EA is always set to 1.

The L bits define the number of value octets that follows. L1 is the LSB and L7 is the MSB; this permits to construct messages with up to 127 value octets.

4.3.2. Message Type and Actions

4.3.2.1. Power Saving Control (PSC)

The power saving control messages use the following type field octet:

1	2	3	4	5	6	7	8
EA	C/R	0	0	0	0	1	0

The length byte contains the value 0 and there are no value octets.

If a station wants to enter a low-power state, it transmits a power saving control command; the other station replies with a power saving control response.

Please refer to document "Quectel_UC20_Power_Management_Application_Note" to get details about power saving mode.

4.3.2.2. Multiplexer Close Down

The multiplexer close down command is used to reset the link into normal AT command mode without multiplexing. The multiplexer closes down messages by the following type field octet:

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1	2	3	4	5	6	7	8
EA	C/R	0	0	0	0	1	1

The length byte contains the value 0 and there are no value octets.

4.3.2.3. Flow Control on Command (FCon)

The flow control command is used to handle the aggregate flow. When either entity is able to receive new information, it will transmit this command.

The length byte contains the value 0 and there are no value octets.

The type field octet has the following format:

1	2	3	4	5	6	7	8
EA	C/R	0	0	0	1	0	1

4.3.2.4. Flow Control off Command (FCoff)

The flow control command is used to handle the aggregate flow. When either entity is not able to receive information, it transmits the FCoff command. The opposite entity is not allowed to transmit frames except on the control channel (DLC=0).

The length byte contains the value 0 and there are no value octets.

The type field octet has the following format:

1	2	3	4	5	6	7	8
EA	C/R	0	0	0	1	1	0

4.3.2.5. Modem Status Command (MSC)

It is desired to convey virtual V.24 control signals to a data stream, this is done by sending the MSC command. The MSC command has one mandatory control signal byte and an optional break signal byte. This command is only relevant when the basic option is chosen.

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This command shall be sent prior to any user data after a creation of a DLC.

Command	Length	DLCI	V.24 Signals	Break Signals(optional)
Communa	Longin	520.	VIZ I Olgilalo	Broak Orginalo(optional)

The length byte contains the value 2 or 3 and there are 2 or 3 value octets.

Both the DTE and DCE use this command to notify each other of the status of their own V.24 control signals. The length of the modern status command is either 4 or 5 bytes depending on the break signal.

UC20 does not support break signals.

The command field octet has the following format:

1	2	3	4	5	6	7	8
EA	C/R	0	0	0	1	1	1

The C/R bit is used to indicate if it is a modem status command or modem status response.

Every time the signals change, the DTE or DCE sends this command to indicate the current status of each signal. When a DTE or DCE receives a modern command, it always sends a response back. The mappings of the V.24 signals to the bits in the control signal octet for the receiver and sender are given in Tables 6 and 7, respectively.

In a modem status command, it is the status of the sender's own V.24 signals that shall be sent, but in a response, it is copy of the V.24 signals that are received from the command frame that shall be returned. The DLCI field identifies the specific DLC to which the command applies. Bit 2 is always set to 1.

1	2	3	4	5	6	7	8
EA	1	DLCI					

The DLC I field is followed by the control signals field which contains a representation of the state of the signals. The use of the extension bit allows other octets to be added to cater for other circumstances. At present, an optional second octet is defined for handling the transmission of break signals.

Bit No.	1	2	3	4	5	6	7	8
Signal	EA	EC	RTC	RTR	Reserved (0)	Reserved (0)	IC	DV



Description of the control signal byte:

- **Bit 1:** The EA bit is set to 1 in the last octet of the sequence; in other octets EA is set to 0. If only one octet is transmitted, EA is set to 1.
- Bit 2: Flow Control (FC). The bit is set to 1(one) when the device is unable to accept frames.
- Bit 3: Ready to Communicate (RTC). The bit is set to 1 when the device is ready to communicate.
- Bit 4: Ready to Receive (RTR). The bit is set to 1 when the device is ready to receive data.
- Bit 5: Reserved for future use. Set to zero by the sender, ignored by the receiver.
- **Bit 6:** Reserved for future use. Set to zero by the sender, ignored by the receiver.
- Bit 7: Incoming call indicator (IC). The bit is set to 1 to indicate an incoming call.
- Bit 8: Data Valid (DV). The bit is set to 1 to indicate that valid data is being sent.

The control byte is mapped to V.24 signals according to the tables below:

Table 6: Mapping from the Control Signal Octet by a Receiving Entity

Control Signal Byte	DTE Receiving	DCE Receiving
Bit number, name	Signal, V.24 circuit	Signal, V.24 circuit
3, RTC	DSR, 107	DTR, 108/2
4, RTR	CTS, 106	RFR (note), 133
7, IC	RI,125	-ignored, -
8, DV	DCD, 109	-ignored, -

NOTE

Circuit 133, RFR (Ready for Receiving) is commonly assigned to the connector pin which is alternatively used for circuit 105, RTS.

Table 7: Mapping to the Control Signal Octet by a Sending Entity

Control Signal Byte	DTE Receiving	DCE Receiving
Bit number, name	Signal, V.24 circuit	Signal, V.24 circuit
3, RTC	DTR , 108/2	DSR, 107



4, RTR	RFR(note), 133	CTS, 106
7, IC	Always 0, -	RI, 125
8, DV	Always 1, -	DCD, 109

NOTE

Circuit 133, RFR (Ready for Receiving) is commonly assigned to the connector pin which is alternatively used for circuit 105, RS.

If a station is unable to transmit frames because of flow control, but wishes to stop accepting further frames itself, it may still send frames containing no user data (i.e. Only the control signal octet and, optionally, the break signal octet) in order to control signal flow.

4.4. Procedure

4.4.1. MUX Establishment

In most cases the establishment of a DLC will be initiated by the TE, however, the protocol is balanced and the initiation may come from the UE. The action taken by the higher layers of the TE upon the initiation of the establishment of a DLC from the UE is outside the scope of this document.

The station wishing to establish a DLC transmits a SABM frame with the P-bit set to 1. The address field contains the DLCI value associated with the desired connection. If the responding station is ready to establish the connection, it will reply with a UA frame with the F-bit set to 1. If the responding station is not ready or unwilling to establish the particular DLC, it will reply with a DM frame with the F-bit set to 1.

Once a DLC has been established, the stations are both said to be in a connected mode, for the particular DLC and transfer of information may commence.

If no UA or DM response has been received after T1, the initiating station may retransmit the SABM. This action may be repeated until a response is obtained or action is taken by a higher layer.

If no negotiation procedure is used, DLC parameters are the default.

4.4.2. MUX Release

The release of a DLC may be initiated by either station transmitting a DISC frame with the P-bit set to 1. Confirmation of the DLC release is signaled by the other station sending a UA frame with the F-bit set to 1. Once the DLC has been released, the stations enter disconnected mode for that particular DLC.

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If the station receiving the DISC command is already in a disconnected mode, it will send a DM response. If no UA or DM response has been received after T1, the initiating station may retransmit the DISC. This action may be repeated until a response is obtained or action is taken by a higher layer.

4.4.3. Data Transfer

4.4.3.1. Information Data

Information is conveyed by using UI or UIH frames. Support of UIH frames is mandatory and support of UI frames is optional. UI frames are used when it is important to know that the data received is correct. An example using of UI frames carries IP (Internet Protocol) traffic where error recovery procedures are performed, if necessary, by a higher layer. The use of UIH frames is appropriate if the link is not subject to errors. UI or UIH frames may also be used for data in situations where the delays inherent in error-recovery procedures are unacceptable, such as transmission of voice data.

The transmitter takes information from the convergence layer for the particular DLC and places it in the I-field of the transmitted frame. Once a UI or UIH frame has been correctly received, the contents of its I-field are passed to the convergence layer.

The frames sent by the initiating station have the C/R bit set to 1 and those sent by the responding station have the C/R bit set to 0. Both stations set the P-bit to 0.

The maximum length of the information field in UI or UIH frames shall be parameter N1.

4.4.3.2. Time-out Considerations

In order to detect a no-reply or lost-reply condition, each station shall provide a response time-out function (T1). The expiry of the time-out function shall be used to initiate appropriate error recovery procedures.

The duration of the time-out function in the two stations shall be unequal in order to resolve contention situations.

The time-out function shall be started whenever a station has transmitted a frame for which a reply is required. When the expected reply is received, the time-out function shall be stopped. If, during the interval that the time-out function is running, other frames are sent for which acknowledgements are required, the time-out function may have to be restarted.

If the response time-out function runs out, a command with the P bit set to 1 may be (re)transmitted, and the response time-out function restarted.



4.4.3.3. Flow Control

Quectel multiplexer supports software flow control mechanism. Software flow control is implemented by GSM 0710 MSC, FCoff and FCon message frame.

TE will send MSC message to MS with FC bit set to 1 in V.24 control signals when TE refuses to accept frames. Whereas, set to 0 to inform recovery of receiving frames. When receiving MSC, MS will feed back MSC response to indicate recover of data transmission.

TE can also send FCoff message to MS when refuses to accept anything except control messages on DLC 0. After this, MS will stop sending any frames through all the data channels except control channels. Control channel is still alive and free to send any control message. Whereas, sends FCon to recover transmission. When receiving FCoff or FCon message, MS will feed back FCoff or FCon response.

The difference between MSC and FCon is that the former only controls one of the data channels, and the latter controls all the data channels except controls channel.



5 Power Saving Mode Under MUX

Quectel module supports sleep mode under MUX. In actual application, there are two solutions for the module to enter into or exit from power saving mode. One is to use physical DTR pin only to control the power saving mode under MUX. The other is to use PSC frame and DTR pin cooperatively. And these two solutions have the same effect on power saving. For more details, please refer to the following part.

If you used both UART and USB port, please refer to "Quectel_UC20_Power_Management_ Application_Note". This document elaborates how to set and operate Host USB and module USB under power saving mode. This chapter only describes power saving function of MUX.

5.1. Power Saving Mode Based on DTR Pin Only

In this solution, you only need to control DTR pin to let the module enter into or exit from power saving mode. Additionally, you need to add the following AT commands during the initialization process.

Table 8: AT Command Configuration Based on DTR Pin

No.	Command Configuration	Description
1	AT+QSCLK=1	
2	AT+QURCCFG="URCPORT","UART1"	Specify URC output port as the UART1 port.
3	AT+QCFG="APREADY"	Configure AP Ready function. For details, please refer to "Quectel_UC20_Power_Management_Application _Note"
4	AT+QINDCFG=	Enable or disable corresponding URC according to the actual needs, to avoid the module being waked up by unnecessary URC. For details, please refer to "UC20_AT_Commands_Manual".
5	AT+QCFG="PWRSAVEDTR",1	Enable DTR pin to control the module to enter into or exit from power saving mode.
6	AT+QCFG="PWRSAVEMODE",1	Enable pulling up DTR pin to let the module enter into power saving mode under MUX.

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When USB is not in use, and the above AT commands are configured, you can pull down DTR to let the module exit from power saving mode, and pull up DTR to enter into power saving mode. If module is in sleep mode, and it receives incoming call, short messages or URC data, physical RI pin will be pulled to wake up the Host, and then the module sends the data to MUX virtual port. If AP READY function is enabled, module will not send the data until AP READY pin is in READY mode, this can effectively avoid data loss when Host is not ready and data interaction occurs during the process of exiting from power saving mode.

In the solution, if Host does not send data to module within 10s after pulling down DTR pin, module will re-enter into power saving mode automatically. In this way, it can prevent the module accidentally exiting from power saving mode because of the unstable DTR external level. The flow chart is shown as below.

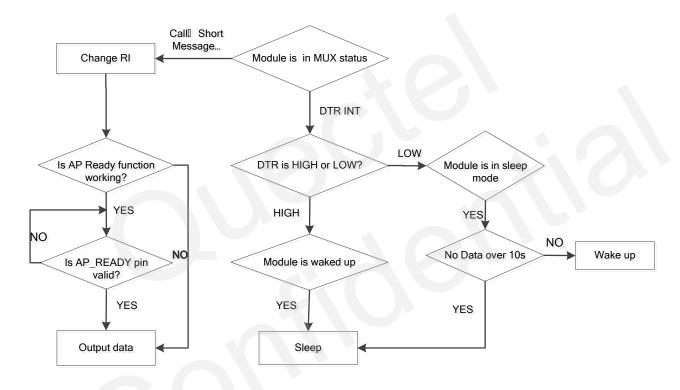


Figure 3: Power Saving Flow Chart (1)

5.1.1. Host Enables Module to Enter into Power Saving Mode

If the module is not in power saving mode, Host can trigger it into power saving mode through the following procedure:

- 1. Configure the AT commands mentioned in Table 8.
- 2. Ensure the module is not in the following state:
 - There is command waiting for execution or reply.
 - Module is still in service, e.g., in data connection, message sending, call incoming or online call.



- 3. Set hardware flow control. Set the Host RTS to disable data receiving. If hardware flow control is disabled, then ignore this step.
- 4. Set AP_READY pin as invalid. If it is disabled, then ignore this step.
- 5. Pull DTR pin from LOW to HIGH, and trigger the module to enter into power saving mode.

5.1.2. Host Enables Module to Exit from Power Saving Mode

If module is in power saving mode, then Host can trigger module to exit from power saving mode through the following procedure:

- 1. Host pulls DTR pin from HIGH to LOW, and triggers module to exit from power saving mode
- 2. Set hardware flow control. Set the Host RTS to enable data receiving. If hardware flow control is disabled, then ignore this step.
- 3. Set AP_READY pin as valid. If it is disabled, then ignore this step.

5.1.3. Module Enables Host to Exit from Power Saving Mode

When module is in power saving mode, if it receives incoming call, short message, network data or necessary URC, RI pin will be pulled to wake up Host to receive the data. Please refer to the procedure below:

- 1. Host receives the change of RI pin, then exits from power saving mode and enters into normal mode.
- 2. After Host exits from power saving mode successfully, pull down DTR pin to let the module exit from power saving mode.
- 3. Set hardware flow control. Set the RTS to enable data receiving. If hardware flow control is disabled, then ignore this step.
- 4. Set AP READY pin as valid. If it is disabled, then ignore this step.
- 5. After the data has been processed, if you need to re-enter into power save mode, please refer to chapter 5.1.1.

NOTE

In this solution, if module is in power saving mode, Host must operate data interaction with module MUX within 10s after DTR has been pulled down, otherwise module will re-enter into power saving mode automatically.

5.2. Power Saving Mode Based on PSC Frame and DTR Pin



In this solution, you need to use both PSC frame and DTR pin to control the module to enter into or exit from power saving mode. In addition, you need to add the following AT commands during the initialization process.

Table 9: AT Command Configuration Based on PSC Frame and DTR Pin

No	Command Configuration	Description
1	AT+QSCLK=1	
2	AT+QURCCFG="URCPORT","UART1"	Specify URC output port as the UART1 port.
3	AT+QCFG="APREADY",	Configure AP Ready function. For details, please refer to "Quectel_UC20_Power_Management_Application_Note"
4	AT+QINDCFG=	Enable or disable corresponding URC according to the actual needs, to avoid the module being waked up by unnecessary URC. For details, please refer to "UC20_AT_Commands_Manual".
5	AT+QCFG="PWRSAVEDTR",1	Enable DTR pin to control the module to enter into or exit from power saving mode.
6	AT+QCFG="PWRSAVEMODE",0	Disable pulling up DTR pin to let the module enter into power saving mode under MUX.

When USB is not in use, and the above AT commands are configured, Host can send PSC frame to let the module enter into power saving mode, and pull down DTR to exit from power saving mode. If module is in sleep mode, and it receives incoming call, short messages or URC data, physical RI pin will be pulled to wake up the Host, and then the module sends the data to MUX virtual port. If AP READY function is enabled, module will not send the data to MUX virtual port until AP READY pin is in READY mode, this can effectively avoid data loss when Host is not ready and data interaction occurs during the process of exiting from power saving mode.

In the solution, there is no requirement on sending data within 10s. The flow chart is shown as below.



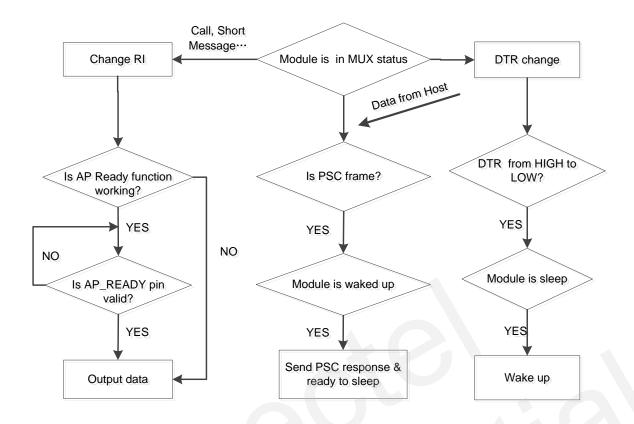


Figure 4: Power Saving Flow Chart (2)

5.2.1. Host Enables Module to Enter into Power Saving Mode

If the module is not in power saving mode, Host can trigger it into power saving mode through the following procedure:

- 1. Configure the AT commands mentioned in Table 9.
- 2. Ensure the module is not in the following sate:
 - There is command waiting for execution or reply.
 - Module is still in service, e.g., in data connection, messaging sending, call incoming or online call.
- 3. Send PSC frame to module, and wait for response.
- 4. Set hardware flow control. Set the Host RTS to disable data receiving. If hardware flow control is disabled, then ignore this step.
- 5. Set AP_READY pin as invalid. If it is disabled, then ignore this step.



5.2.2. Host Enables Module to Exit from Power Saving Mode

If module is in power saving mode, then Host can trigger module to exit from power saving mode through the following procedure:

- 1. Host pulls DTR pin from HIGH to LOW, and triggers module to exit from power saving mode
- 2. Set hardware flow control. Set the Host RTS to enable data receiving. If hardware flow control is disabled, then ignore this step.
- 3. Set AP_READY pin as valid. If it is disabled, then ignore this step.

5.2.3. Module Enables Host to Exit from Power Saving Mode

When module is in power saving mode, if it receives incoming call, short message, network data or necessary URC, RI pin will be pulled to wake up Host to receive the data. Please refer to the procedure below:

- 1. Host receives the change of RI pin, then exits from power saving mode and enters into normal mode.
- 2. After Host exits from power saving mode successfully, pull down DTR pin to let the module exit from power saving mode.
- 3. Set hardware flow control. Set the RTS to enable data receiving. If hardware flow control is disabled, then ignore this step.
- 4. Set AP_READY pin as valid. If it is disabled, then ignore this step.
- 5. After the data has been processed, if you need to re-enter into power save mode, please refer to chapter 5.2.1.

NOTE

In this solution, after Host pulls down DTR, the module will exit from power saving mode, and there is no requirement on data interaction within 10s.



6 Example

6.1. Samples for Frame Structure

Sample 1:

F9	03	3F	01	1C	F9
Opening Flag	Address Field	Control Field	Length Field	FCS	Closing Flag
Header	DLCI 0	SABM Frame	0, No Information Filed		Tail

This sample is a SABM frame to open DLCI 0.

Sample 2:

F9	05	EF	09	41 54 49 0D	58	F9
Opening Flag	Address Field	Control Field	Length Field	Information Field	FCS	Closing Flag
Header	DLC 1	UIH Frame	4	AT Command "ATI <cr>"</cr>		Tail

This sample is a UIH frame to transmit AT command "ATI<CR>".

Sample 3:

F9	01	EF	0B	E3 07 07 0D 01	79	F9
Opening Flag	Address Field	Control Field	Length Field	Information Field	FCS	Closing Flag
Header	DLC 0	UIH Frame	5	MSC Message, Length 3		Tail

This sample is a MSC message carried in UIH frame to transmit V2.4 signal 0x0D.



6.2. Establish Channels

Step 1: Launch Multiplexer

No	Step	Data Direction	Hex	Comment
	TE launches MS multiplexer function by AT command	TE→MS	61 74 2B 63 6D 75 78 3D 30 0D 0D 0A 4F 4B 0D 0A 0D 0A	AT+CMUX=0 <cr><lf></lf></cr>
ı	MS feeds back response	TE←MS	61 74 2B 63 6D 75 78 3D 30 0D 0D 0A 4F 4B 0D 0A 0D 0A	AT+CMUX=0 <cr><lf>O K<cr><lf><cr><lf></lf></cr></lf></cr></lf></cr>

Step 2: Establish DLC 0

No	Step	Data Direction	Hex	Comment
1	TE requests to establish control channel DLCI 0 by SABM frame	TE→MS	F9 03 3F 01 1C F9	SABM Frame
1	MS feeds back UA for receiving SABM and accepts to create DLCI 0	TE←MS	F9 03 73 01 D7 F9	UA Frame

Step 3: Establish DLC 1, 2

No	Step	Data Direction	Hex	Comment
	TE requests to establish DLCI9 by SABM frame	TE→MS	F9 27 3F 01 0B F9	
1	MS feeds back DM for receiving SABM but refuses to create DLCI 9	TE←MS	F9 27 1F 01 21 F9	
	TE requests to establish DLCI1 by SABM frame	TE→MS	F9 07 3F 01 DE F9	
2	MS feeds back UA for receiving SABM and accepts to create DLCI 1	TE←MS	F9 07 73 01 15 F9	
	MS sends MSC message frame	TE←MS	F9 01 EF 0B E3 07 07 0D 01 79 F9	
	MS sends OK	TE←MS	F9 05 EF 0D 0D 0A 4F 4B 0D 0A 5F F9	



	TE sends MSC message	TE→MS	F9 01 EF 0B E3 07
	frames	T LIVIO	07 0D 01 79 F9
	MS feeds back MSC response	TE←MS	F9 01 EF 0B E1 07
	MS feeds back MSC response	T L←IVIS	07 0D 01 79 F9
	TE requests to establish DLCI2	TE→MS	F9 0B 3F 01 59 F9
	by SABM frame		
	MS feeds back UA for		
	receiving SABM and accepts to	TE←MS	F9 0B 73 01 92 F9
	create DLCI 2		
3	MS sends MSC message	TE←MS	F9 01 EF 0B E3 07
	frame	T L←IVIS	0B 0D 01 79 F9
	TE sends MSC message	TE→MS	F9 01 EF 0B E3 07
	frames	I E→IVIS	0B 0D 01 79 F9
	MS foods book MSC response	TE←MS	F9 01 EF 0B E1 07
	MS feeds back MSC response	T E←IVIS	0B 0D 01 79 F9
4	Establish DLC 3, 4, same as above		
	By now, 4 channels have come into		
5	existence. Multiplexer can work		
	normally		

This sample is a MSC message carried in UIH frame to transmit V2.4 signal 0x0D.

6.3. Frame Transmission

After establishing control channel and data channels, TE and MS can transmit data to each other through UIH frames.

E sends AT ommand "ATI <cr>" rough DLC 1</cr>	TE→MS	F9 05 EF 09 41 54 49 0D 58 F9	
•		1000 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 -	UIH Frame
S feeds back rough DLC 1	TE←MS	F9 05 EF 09 41 54 49 0D 58 F9 F9 05 EF 9B 0D 0A 53 49 4D 43 4F 4D 5F 4C 74 64 0D 0A 53 49 4D 43 4F 4D 5F 53 49 4D 33 30 30 0D 0A 52 65 76 69 73 69 6F 6E 3A 53 49 4D 33 30 30 4D 33 32 28 53 50 41 4E 53 49 4F 4E 29 5F 56 31 30 2E 30 2E 38 5F 42 55 49	UIH Frame
S	feeds back	rfeeds back TE←MS	F9 05 EF 09 41 54 49 0D 58 F9 F9 05 EF 9B 0D 0A 53 49 4D 43 4F 4D 5F 4C 74 64 0D 0A 53 49 4D 43 4F 4D 5F 53 49 4D 33 30 4D 43 4F 4D 5F 53 49 4D 33 30 30 0D 0A 52 65 76 69 73 69 6F 6E 3A 53 49 4D 33 30 30 4D 33 32 28 53 50 41 4E 53 49 4F 4E 29 5F 56



			F9 05 EF 09 4F 4B 0D 0A 58 F9	
0	TE sends AT command "AT <cr>" through DLC 2"</cr>	TE→MS	F9 09 EF 07 41 54 0D 35 F9	UIH Frame
2	MS feeds back through DLC 2	TE←MS	F9 09 EF 07 41 54 0D 35 F9 F9 09 EF 0D 0D 0A 4F 4B 0D 0A D8 F9	UIH Frame
3	DLC 3, 4 are the same as above			

6.4. Power Saving Mode and Wake Up

Power saving:

No	Step	Data Direction	Hex	Comment
1	TE sends PSC message through DLC 0	TE→MS	F9 03 EF 05 43 01 F2 F9	PSC Command Frame
1	MS feeds back PSC message through DLC 0	TE←MS	F9 03 EF 05 41 01 F2 F9	PSC Response Frame
	MS enters power saving			
2	mode, TE sends F9 continuously	TE→MS	F9 F9 F9 F9	

Wake up:

No	Step	Data Direction	Hex	Comment
1	TE sends wake up flags	TE→MS	F9 F9 F9 F9	
1	MS feeds back	TE←MS	F9 F9 F9 F9	
2	MS is waked up, and data transmission is recovered			

6.5. Flow Control

No	Step	Data Direction	Hex	Comment
1	MS sends MSC message with FC	TE MC	F9 01 EF 0B E3	
ı	bit set to 1 through control channel	I E←IVIS	07 07 8F 01 79	

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2 DL 1 c TE bit DL	LC 0, to indicate refusing to ccept anything on DLC 1 S sends MSC message with FC t set to 0 through control channel LC 0, to indicate recovery of DLC	TE←MS	F9 01 EF 0B E3
2 DL 1 c TE bit DL	S sends MSC message with FC t set to 0 through control channel LC 0, to indicate recovery of DLC	TE←MS	F9 01 EF 0B E3
2 bit DL 1 c TE bit DL	t set to 0 through control channel LC 0, to indicate recovery of DLC	TE←MS	F9 01 EF 0B E3
3 bit	data transmission		07 07 8D 01 79 F9
ao	E sends MSC message with FC t set to 1 through control channel LC 0, to indicate refusing to eccept anything on DLC 1	TE→MS	F9 01 EF 0B E3 07 07 8F 01 79 F9
4 bit	E sends MSC message with FC t set to 0 through control channel LC, to indicate recovery of DLC 1 ata transmission	TE→MS	F9 01 EF 0B E3 07 07 8D 01 79 F9
5 DL acc	E sends FCoff message through LC 0, to indicate refusing to eccept anything on all DLC except LC 0	TE→MS	F9 01 EF 05 63 01 93 F9
TE 6 DL tra	E sends FCon message through		

6.6. Synchronization

After successful establishment of data channels, TE and MS are synchronized and data transmission is normal. Every transmission is implemented by frames which begins with a starting flag (0xF9) and ends with a closing flag (0xF9). So it is called that multiplexer is synchronized with flag 0xF9. Transmitting bytes other than 0xF9 between frames is considered as faulty or synchronization lost and needs re-sync.

No	Step	Data Direction	Hex	Comment
1	TE receives error frame	TE←MS	F9 01 EF 05	
2	TE sends sync flag to re-sync with MS	TE→MS	F9 F9 F9	
3	MS feeds back four hex value F9 to indicate illegal bytes received and needs re-sync	TE←MS	F9 F9 F9	
4	TE tests AT command transmission through DLC 1 after re-sync	TE→MS	F9 05 EF 07 41 54 0D 06 F9	
	MS feeds back response and	TE←MS	F9 05 EF 07 41 54	

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synchronization has been reset	0D 67 F9 F9 25 EF
to normal	0D 0D 0A 4F 4B
	0D 0A 8A F9

NOTES

- 1. UC20 does not initiative to send sync flags (F9), even though MS receives error frames.
- 2. While UC20 module is not in power saving mode and receives more than 2 sync flag, module will send only 3 sync flags to TE, even if it receives more than 3 sync flags.
- 3. While UC20 module is in power saving mode, module will send the number of sync flags (F9) received from TE.

6.7. Closing Down Multiplexers

No	Step	Data Direction	Hex	Comment
1	TE sends DISC frame to request for closing down DLC 1	TE→MS	F9 07 53 01 3f F9	
	MS feeds back UA frame to accept	TE←MS	F9 07 73 01 15 F9	
2	TE sends DISC frame to request for closing down DLC 2	TE→MS	F9 0b 53 01 B8 F9	
	MS feeds back UA frame to accept	TE←MS	F9 0b 73 01 92 F9	
3	TE sends DISC frame to request for closing down DLC 3	TE→MS	F9 0f 53 01 3f F9	
	MS feeds back UA frame to accept	TE←MS	F9 0f 73 01 15 F9	
4	TE sends DISC frame to request for closing down DLC 4	TE→MS	F9 13 53 01 3f F9	
	MS feeds back UA frame to accept	TE←MS	F9 13 73 01 15 F9	
5	TE sends CLD message frame to request for closing down multiplexer through DLC 0	TE→MS	F9 03 EF 05 C3 01 F2 F9	
	MS feeds back CLD response to accept	TE←MS	F9 03 EF 05 C1 01 F2 F9	
6	By now, closing down procedure is over			



7 Appendix A Reference

Table 10: Related Documents

SN	Document Name	Remark
[1]	3GPP TS 27.010 V9.0.0	3rd Generation Partnership Project; Technical Specification Group Terminals; Terminal Equipment to User Equipment (TE-UE) multiplexer protocol
[2]	Quectel_UC20_AT_Commands_Manual	UC20 AT commands manual
[3]	Quectel_UC20_Power_Management_Application_Note	UC20 power management application note

Table 11: Terms and Abbreviations

Abbreviation	Description
MUX	Multiplexer Protocol
ABM	Asynchronous Balanced Mode
DLC	Data Link Connection
FCS	Frame Check Sequence
SABM	Set Asynchronous Balanced Mode
DM	Disconnected Mode
UIH	Unnumbered Information with Header Check
UI	Unnumbered Information
PSC	Power Saving Control
MSC	Modem Status Command

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