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| Tool Version : Vivado v.2018.2.2 (lin64) Build 2348494 Mon Oct 1 18:25:39 MDT 2018

| Date : Thu May 16 04:56:29 2019

| Host : t620-PowerEdge-T620 running 64-bit Ubuntu 18.04.2 LTS

| Command : report\_utilization -hierarchical -file util\_1024\_v2

| Design : RTAD\_ML

| Device : 7z045ffg900-2

| Design State : Routed

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Utilization Design Information

Table of Contents

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1. Utilization by Hierarchy

1. Utilization by Hierarchy

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| Instance | Module | Total LUTs | Logic LUTs | LUTRAMs | SRLs | FFs | RAMB36 | RAMB18 | DSP48 Blocks |

+------------------------------------------------------------+----------------------------------------------+------------+------------+---------+------+------+--------+--------+--------------+

| RTAD\_ML | (top) | 22432 | 22432 | 0 | 0 | 4464 | 89 | 17 | 10 |

| (RTAD\_ML) | (top) | 239 | 239 | 0 | 0 | 0 | 0 | 0 | 0 |

| addr\_fifo | ADDR\_FIFO\_13x64 | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| U0 | fifo\_generator\_v13\_2\_2\_\_parameterized1 | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| inst\_fifo\_gen | fifo\_generator\_v13\_2\_2\_synth\_\_parameterized0 | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| gconvfifo.rf | fifo\_generator\_top\_\_parameterized0 | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| grf.rf | fifo\_generator\_ramfifo\_\_parameterized0 | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| gntv\_or\_sync\_fifo.gl0.rd | rd\_logic\_241 | 17 | 17 | 0 | 0 | 14 | 0 | 0 | 0 |

| grss.rsts | rd\_status\_flags\_ss\_245 | 2 | 2 | 0 | 0 | 2 | 0 | 0 | 0 |

| rpntr | rd\_bin\_cntr\_246 | 15 | 15 | 0 | 0 | 12 | 0 | 0 | 0 |

| gntv\_or\_sync\_fifo.gl0.wr | wr\_logic\_242 | 8 | 8 | 0 | 0 | 14 | 0 | 0 | 0 |

| gwss.wsts | wr\_status\_flags\_ss\_243 | 4 | 4 | 0 | 0 | 2 | 0 | 0 | 0 |

| wpntr | wr\_bin\_cntr\_244 | 4 | 4 | 0 | 0 | 12 | 0 | 0 | 0 |

| gntv\_or\_sync\_fifo.mem | memory\_\_parameterized0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gbm.gbmg.gbmga.ngecc.bmg | blk\_mem\_gen\_v8\_4\_1\_\_parameterized5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| embedding | RTAD\_EMBEDDING | 368 | 368 | 0 | 0 | 3 | 64 | 2 | 0 |

| (embedding) | RTAD\_EMBEDDING | 300 | 300 | 0 | 0 | 1 | 0 | 0 | 0 |

| genblk3[0].sys\_embed | Syscall\_Embedding\_32x283\_\_1 | 2 | 2 | 0 | 0 | 2 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized7\_\_1 | 2 | 2 | 0 | 0 | 2 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized3\_236 | 2 | 2 | 0 | 0 | 2 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized0\_237 | 2 | 2 | 0 | 0 | 2 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized0\_238 | 2 | 2 | 0 | 0 | 2 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized0\_239 | 2 | 2 | 0 | 0 | 2 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized0\_240 | 2 | 2 | 0 | 0 | 2 | 0 | 1 | 0 |

| genblk3[1].sys\_embed | Syscall\_Embedding\_32x283 | 2 | 2 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized7 | 2 | 2 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized3 | 2 | 2 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized0\_232 | 2 | 2 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized0\_233 | 2 | 2 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized0\_234 | 2 | 2 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized0\_235 | 2 | 2 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk4[0].branch\_embed | Branch\_Embedding\_32x4096\_\_1 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_1 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_221 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_222 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_223 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_224 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_231 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_225 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_230 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_226 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_229 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_227 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_228 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[10].branch\_embed | Branch\_Embedding\_32x4096\_\_11 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_11 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_111 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_112 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_113 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_114 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_121 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_115 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_120 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_116 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_119 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_117 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_118 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[11].branch\_embed | Branch\_Embedding\_32x4096\_\_12 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_12 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_100 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_101 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_102 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_103 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_110 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_104 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_109 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_105 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_108 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_106 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_107 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[12].branch\_embed | Branch\_Embedding\_32x4096\_\_13 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_13 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_89 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_90 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_91 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_92 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_99 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_93 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_98 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_94 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_97 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_95 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_96 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[13].branch\_embed | Branch\_Embedding\_32x4096\_\_14 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_14 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_78 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_79 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_80 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_81 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_88 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_82 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_87 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_83 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_86 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_84 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_85 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[14].branch\_embed | Branch\_Embedding\_32x4096\_\_15 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_15 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_67 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_68 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_69 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_70 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_77 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_71 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_76 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_72 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_75 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_73 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_74 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[15].branch\_embed | Branch\_Embedding\_32x4096 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[1].branch\_embed | Branch\_Embedding\_32x4096\_\_2 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_2 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_210 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_211 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_212 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_213 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_220 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_214 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_219 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_215 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_218 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_216 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_217 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[2].branch\_embed | Branch\_Embedding\_32x4096\_\_3 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_3 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_199 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_200 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_201 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_202 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_209 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_203 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_208 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_204 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_207 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_205 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_206 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[3].branch\_embed | Branch\_Embedding\_32x4096\_\_4 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_4 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_188 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_189 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_190 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_191 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_198 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_192 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_197 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_193 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_196 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_194 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_195 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[4].branch\_embed | Branch\_Embedding\_32x4096\_\_5 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_5 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_177 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_178 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_179 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_180 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_187 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_181 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_186 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_182 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_185 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_183 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_184 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[5].branch\_embed | Branch\_Embedding\_32x4096\_\_6 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_6 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_166 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_167 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_168 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_169 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_176 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_170 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_175 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_171 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_174 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_172 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_173 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[6].branch\_embed | Branch\_Embedding\_32x4096\_\_7 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_7 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_155 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_156 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_157 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_158 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_165 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_159 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_164 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_160 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_163 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_161 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_162 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[7].branch\_embed | Branch\_Embedding\_32x4096\_\_8 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_8 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_144 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_145 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_146 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_147 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_154 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_148 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_153 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_149 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_152 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_150 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_151 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[8].branch\_embed | Branch\_Embedding\_32x4096\_\_9 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_9 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_133 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_134 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_135 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_136 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_143 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_137 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_142 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_138 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_141 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_139 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_140 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| genblk4[9].branch\_embed | Branch\_Embedding\_32x4096\_\_10 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized9\_\_10 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized4\_122 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized3\_123 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized3\_124 | 4 | 4 | 0 | 0 | 0 | 4 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized3\_125 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized3\_132 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized4\_126 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized4\_131 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized5\_127 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized5\_130 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized6\_128 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized6\_129 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| igm | RTAD\_IGM | 12872 | 12872 | 0 | 0 | 1499 | 0 | 10 | 0 |

| A\_IVG | RTAD\_IGM\_IVG | 199 | 199 | 0 | 0 | 75 | 0 | 10 | 0 |

| (A\_IVG) | RTAD\_IGM\_IVG | 174 | 174 | 0 | 0 | 47 | 0 | 0 | 0 |

| Syscallfilter | SyscallFilter\_32x283 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| addr\_fifo | ADDR\_FIFO\_33x64 | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| U0 | fifo\_generator\_v13\_2\_2 | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| inst\_fifo\_gen | fifo\_generator\_v13\_2\_2\_synth | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| gconvfifo.rf | fifo\_generator\_top | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| grf.rf | fifo\_generator\_ramfifo | 25 | 25 | 0 | 0 | 28 | 0 | 1 | 0 |

| gntv\_or\_sync\_fifo.gl0.rd | rd\_logic | 17 | 17 | 0 | 0 | 14 | 0 | 0 | 0 |

| grss.rsts | rd\_status\_flags\_ss | 2 | 2 | 0 | 0 | 2 | 0 | 0 | 0 |

| rpntr | rd\_bin\_cntr | 15 | 15 | 0 | 0 | 12 | 0 | 0 | 0 |

| gntv\_or\_sync\_fifo.gl0.wr | wr\_logic | 8 | 8 | 0 | 0 | 14 | 0 | 0 | 0 |

| gwss.wsts | wr\_status\_flags\_ss | 4 | 4 | 0 | 0 | 2 | 0 | 0 | 0 |

| wpntr | wr\_bin\_cntr | 4 | 4 | 0 | 0 | 12 | 0 | 0 | 0 |

| gntv\_or\_sync\_fifo.mem | memory | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gbm.gbmg.gbmga.ngecc.bmg | blk\_mem\_gen\_v8\_4\_1\_\_parameterized3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk1[0].branch\_filter | BranchFilter\_32x512\_\_1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_62 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_63 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_64 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_65 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_66 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk1[1].branch\_filter | BranchFilter\_32x512\_\_2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_57 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_58 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_59 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_60 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_61 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk1[2].branch\_filter | BranchFilter\_32x512\_\_3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_52 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_53 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_54 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_55 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_56 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk1[3].branch\_filter | BranchFilter\_32x512\_\_4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_47 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_48 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_49 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_50 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_51 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk1[4].branch\_filter | BranchFilter\_32x512\_\_5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_42 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_43 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_44 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_45 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_46 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk1[5].branch\_filter | BranchFilter\_32x512\_\_6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_37 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_38 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_39 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_40 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_41 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk1[6].branch\_filter | BranchFilter\_32x512\_\_7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_32 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_33 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_34 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_35 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_36 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| genblk1[7].branch\_filter | BranchFilter\_32x512 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_29 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_30 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_31 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| A\_P2S | RTAD\_IGM\_P2S | 485 | 485 | 0 | 0 | 1107 | 0 | 0 | 0 |

| A\_TA | RTAD\_IGM\_TA | 12188 | 12188 | 0 | 0 | 317 | 0 | 0 | 0 |

| lstm | LSTM | 8529 | 8529 | 0 | 0 | 2282 | 14 | 3 | 6 |

| (lstm) | LSTM | 2146 | 2146 | 0 | 0 | 2282 | 0 | 0 | 3 |

| BIAS\_BRAM | SRAM\_32x512 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized13 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| B\_BQS\_1 | B\_BQS | 95 | 95 | 0 | 0 | 0 | 0 | 0 | 0 |

| B\_BQT\_1 | B\_BQT | 87 | 87 | 0 | 0 | 0 | 0 | 0 | 0 |

| B\_MAQ\_1 | B\_MAQ | 120 | 120 | 0 | 0 | 0 | 0 | 0 | 0 |

| B\_TMQ\_1 | B\_TMQ | 31 | 31 | 0 | 0 | 0 | 0 | 0 | 1 |

| CONVERT\_Ct\_1 | CONVERT\_Ct | 300 | 300 | 0 | 0 | 0 | 0 | 0 | 0 |

| CONVERT\_Ct\_2 | CONVERT\_Ct\_0 | 4 | 4 | 0 | 0 | 0 | 0 | 0 | 0 |

| CONVERT\_Ht\_1 | CONVERT\_Ht | 428 | 428 | 0 | 0 | 0 | 0 | 0 | 0 |

| CONVERT\_Ht\_2 | CONVERT\_Ht\_1 | 5 | 5 | 0 | 0 | 0 | 0 | 0 | 0 |

| S\_BQS\_1 | S\_BQS | 106 | 106 | 0 | 0 | 0 | 0 | 0 | 0 |

| S\_BQS\_2 | S\_BQS\_2 | 104 | 104 | 0 | 0 | 0 | 0 | 0 | 0 |

| S\_BQT\_1 | S\_BQT | 120 | 120 | 0 | 0 | 0 | 0 | 0 | 0 |

| S\_BQT\_2 | S\_BQT\_3 | 116 | 116 | 0 | 0 | 0 | 0 | 0 | 0 |

| S\_MAQ\_1 | S\_MAQ | 110 | 110 | 0 | 0 | 0 | 0 | 0 | 0 |

| S\_MAQ\_2 | S\_MAQ\_4 | 136 | 136 | 0 | 0 | 0 | 0 | 0 | 0 |

| S\_TMQ\_1 | S\_TMQ | 50 | 50 | 0 | 0 | 0 | 0 | 0 | 1 |

| S\_TMQ\_2 | S\_TMQ\_5 | 53 | 53 | 0 | 0 | 0 | 0 | 0 | 1 |

| WEIGHT\_BRAM1 | SRAM\_128x2048\_\_1 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized11\_\_1 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized5\_9 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized4\_10 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized4\_11 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized7\_12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized7\_27 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized8\_13 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized8\_26 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized9\_14 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized9\_25 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized10\_15 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized10\_24 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[4].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized11\_16 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized11\_23 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[5].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized12\_17 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized12\_22 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[6].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized13\_18 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized13\_21 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[7].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized14\_19 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized14\_20 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| WEIGHT\_BRAM2 | SRAM\_128x2048 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized11 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized5 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized4 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized4 | 0 | 0 | 0 | 0 | 0 | 7 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized8 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized8 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized9 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized9 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized10 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized10 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[4].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized11 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized11 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[5].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized12 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized12 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[6].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized13 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized13 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[7].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized14 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized14 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| u\_inpdt\_1 | inpdt\_16\_mid | 2129 | 2129 | 0 | 0 | 0 | 0 | 0 | 0 |

| u\_inpdt\_2 | inpdt\_16\_mid\_6 | 2280 | 2280 | 0 | 0 | 0 | 0 | 0 | 0 |

| u\_sig\_LUT1 | sigmoid\_LUT | 24 | 24 | 0 | 0 | 0 | 0 | 0 | 0 |

| u\_sig\_LUT2 | sigmoid\_LUT\_7 | 24 | 24 | 0 | 0 | 0 | 0 | 0 | 0 |

| u\_tanh\_LUT1 | tanh\_LUT | 33 | 33 | 0 | 0 | 0 | 0 | 0 | 0 |

| u\_tanh\_LUT2 | tanh\_LUT\_8 | 33 | 33 | 0 | 0 | 0 | 0 | 0 | 0 |

| ml\_ctrl | RTAD\_ML\_CTRL | 8 | 8 | 0 | 0 | 3 | 0 | 0 | 0 |

| softmax | softmax | 397 | 397 | 0 | 0 | 649 | 11 | 1 | 4 |

| (softmax) | softmax | 397 | 397 | 0 | 0 | 649 | 0 | 0 | 4 |

| BR\_BIAS\_BRAM | SRAM\_8x4096 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized17 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized8 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized6 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized6 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized72 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized72 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| BR\_WEIGHT\_BRAM | SRAM\_512x4096 | 0 | 0 | 0 | 0 | 0 | 9 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized15 | 0 | 0 | 0 | 0 | 0 | 9 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized7 | 0 | 0 | 0 | 0 | 0 | 9 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized5 | 0 | 0 | 0 | 0 | 0 | 9 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized5 | 0 | 0 | 0 | 0 | 0 | 9 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized15 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized15 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[1].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized16 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized16 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[2].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized17 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized17 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[3].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized18 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized18 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[4].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized19 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized19 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[5].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized20 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized20 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[6].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized21 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized21 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[7].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized22 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized22 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[8].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized23 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized23 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| SYS\_BIAS\_BRAM | SRAM\_8x243 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized21 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized10 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized8 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized8 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized74 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized74 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| SYS\_WEIGHT\_BRAM | SRAM\_64x243 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| U0 | blk\_mem\_gen\_v8\_4\_1\_\_parameterized19 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| inst\_blk\_mem\_gen | blk\_mem\_gen\_v8\_4\_1\_synth\_\_parameterized9 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| gnbram.gnativebmg.native\_blk\_mem\_gen | blk\_mem\_gen\_top\_\_parameterized7 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| valid.cstr | blk\_mem\_gen\_generic\_cstr\_\_parameterized7 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| ramloop[0].ram.r | blk\_mem\_gen\_prim\_width\_\_parameterized73 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| prim\_noinit.ram | blk\_mem\_gen\_prim\_wrapper\_\_parameterized73 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

+------------------------------------------------------------+----------------------------------------------+------------+------------+---------+------+------+--------+--------+--------------+

\* Note: The sum of lower-level cells may be larger than their parent cells total, due to cross-hierarchy LUT combining