MICHAEL JAEMIN KIM

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NATIONALITY

Republic of Korea & United States of America (Dual Nationality)

EDUCATION

B.S.E. in Electrical and Computer Engineering, Seoul National University — Aug 2019
Ph.D Candidate, Seoul National University (Professor Jung Ho Ahn) — Aug 2019 - Now
Visiting Research, University of Illinois Urbana-Champaign (Professor Nam Sung Kim) — Mar 2023 - Mar 2024

PUBLICATION

- [ISCA 2024] (to appear) "DRAMScope: Uncovering DRAM Microarchitecture and Characteristics by Issuing Memory Commands",
  Hwayong Nam, Seungmin Baek, Minbok Wi, **M. J. Kim**, Jaehyun Park, Chihun Song, N. S. Kim, J. Ahn, in Proceedings of the 51st annual international symposium on computer architecture, 2024,
- [ASPLOS 2024] "TAROT: A CXL SmartNIC-Based Defense Against Multi-bit Errors by Row-Hammer Attacks",
  C. Park, **M. J. Kim**, Tianchen Wang, Houxiang Ji, Jinghan Huang, Ipoom Jeong, Jaehyun Park, Hwayong Nam, Minbok Wi, J. Ahn, N. S. Kim, in ACM International Conference on Architectural Support for Programming Languages and Operating Systems, 2024,
- [ASPLOS 2024] "AttAcc! Unleashing the Power of PIM for Batched Transformer-based Generative Model Inference",
  J. Park, J. Choi, K. Kyung, **M. J. Kim**, Y. Kwon, N. S. Kim, J. Ahn, in ACM International Conference on Architectural Support for Programming Languages and Operating Systems, 2024,
- [MICRO 2023] "How to Kill the Second Bird with One ECC: The Pursuit of Rowhammer Resilient DRAM",
  M. J. Kim, J. Park, M. Wi, S. Ko, J. Park, H. Nam, N. S. Kim, E. Lee, J. Ahn, in IEEE/ACM International Symposium on Microarchitecture, 2023, DOI:10.1145/3613424.3623777
- [CAL 2023] "X-ray: Discovering DRAM internal structure and error characteristics by issuing memory commands.",
  H. Nam, S. Baek, M. Wi, **M. J. Kim**, J. Park, C. Song, N. S. Kim, J. Ahn, in IEEE Computer Architecture Letters, 2023. DOI:10.1109/LCA.2023.3296153
- [HPCA 2023] "SHADOW: Preventing Row Hammer in DRAM with Intra-Subarray Row Shuffling",
  M. Wi, J. Park, **M. J. Kim**, S. Ko, N. S. Kim, E. Lee, J. Ahn, in Proceeding of 29th IEEE International Symposium on High Performance Computer Architecture, 2023. DOI:10.1109/HPCA56546.2023.10070966
- (arXiv) "AESPA: Accuracy Preserving Low-degree Polynomial Activation for Fast Private Inference",
  J. Park, **M. J. Kim**, W. Jung, J. Ahn, 2022. arXiv
- [TC 2022] "Future Scaling of Memory Hierarchy for Tensor Cores and Eliminating Redundant Shared Memory Traffic Using Inter-Warp Multicasting",
  S. Lee, S. Hwang, **M. J. Kim**, J. Choi, and J. Ahn, IEEE Transactions on Computers, Early Access, 2022. DOI:10.1109/TC.2022.3207134
- [ISCA 2022] "BTS: An Accelerator for Bootstrappable Fully Homomorphic Encryption",
  S. Kim, J. Kim, **M. J. Kim**, W. Jung, M. Rhu, J. Kim, J. Ahn, in Proceedings of the 49th annual international symposium on computer architecture, 2022. DOI:10.1145/3470496.3527415
- [HPCA 2022] "Mithril: Cooperative Row Hammer Protection on Commodity DRAM Leveraging Managed Refresh",

M. J. Kim, J. Park, Y. Park, W. Doh, N. Kim, T. Ham, J. Lee, and J. Ahn, in Proceeding of 28th IEEE International Symposium on High Performance Computer Architecture, 2022. DOI:10.1109/HPCA53966.2022.00088

EXPERIENCE

- SNU MMS Lab Internship (Professor Dongsuk Jeon) — Dec 2018 - Feb 2019
  - Verilog design project for spike neural network accelerator.
- SK Hynix Internship — Dec 2017
  - Verilog design project for toy memory controller.
- Mandatory military service for ROK army, at Korea Military Academy — Nov 2014 - Aug 2016
  - Key Resolve ROK-US Combined Exercise at Ministry of National Defense. — Mar 2016

SKILLS

Languages C/C++, Verilog, Python
Tools McSimA+, Pintool Pinpoint, SPEC2006/2017, SPLASH-2/3, GoogleTest, Python Pandas, Docker