

Jiayuan He

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RESEARCH INTERESTS

Parallel Computing, GPU Computing, Graph Analytics, Placement and Routing in EDA

EDUCATION

University of Texas at Austin

Austin, TX

PhD student, Computer Science

Sep. 2014 – Present

Advisor: Keshav Pingali

Tsinghua University

Beijing, China

Bachelor, Electrical Engineering

Sep. 2010 – Aug. 2014

Second Bachelor, Economics

PROFESSIONAL EXPERIENCE

University of Texas at Austin

Austin, TX

Graduate Research Assistant

Sep. 2014 – Present

- **Graph analytics on multicore CPUs and GPUs:** Designed microbenchmarks to identify parallelization bottlenecks. Optimized classic graph applications, including BFS, PageRank, Connected Component and Independent Set.
- **Parallelization of EDA algorithms:** Proposed a hybrid parallel algorithm which exploits net-level parallelism and fine-grain parallelism. Implemented *SPRoute* which achieves significant speedup over state-of-the-art academic global router.

VMware

Palo Alto, CA

Research Intern

May – Aug. 2018

Manager: Josh Simons

- **Characterization and prediction of performance interference on virtual GPUs:** Designed microbenchmarks to study the interference of multiple workloads on virtual GPUs. Characterized deep learning workload by low level features, which are further used to generate an interference prediction model. The work is published in HotCloud19.
- **Investigation of P2P communication malfunction on passthrough GPU in virtual environment**

Tsinghua University

Beijing, China

Research Assistant

Oct. 2012 – Aug. 2014

Advisor: Yangdong Deng

- **FastLanes, An FPGA Accelerated GPU Microarchitecture Simulator:** Introduced a comprehensive FPGA-based GPU simulation framework. Built a simulator for GPU cache and memory.
- **de Bruijn Graph (bioinformatics) Construction on GPUs:** Implemented the first de Bruijn graph construction program on GPU with a speedup of 200X over CPU.

PUBLICATIONS

- **He, Jiayuan**, Martin Burtscher, Rajit Manohar, and Keshav Pingali. "SPRoute: A Scalable Parallel Negotiation-based Global Router." In 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1-8. IEEE, 2019.
- Xu, Xin, Na Zhang, Michael Cui, **Jiayuan He**, and Ridhi Surana. "Characterization and prediction of performance interference on mediated passthrough GPUs for interference-aware scheduler." In 11th {USENIX} Workshop on Hot Topics in Cloud Computing (HotCloud 19). 2019.
- Ataei, Samira, **Jiayuan He**, Wenmian Hua, Yi-Shan Lu, Sepideh Maleki, Yihang Yang, Keshav Pingali, and Rajit Manohar. "Toward a digital flow for asynchronous VLSI systems." In 2nd Workshop on Open-Source EDA Technology (WOSET), Westminster, CO, November 9, 2019.
- Lu, Yi-Shan, Samira Ataei, **Jiayuan He**, Wenmian Hua, Sepideh Maleki, Yihang Yang, Martin Burtscher, Keshav Pingali, and Rajit Manohar. "Parallel Tools for Asynchronous VLSI Systems." In 1st Workshop on Open-Source EDA Technology (WOSET), San Diego, CA, November 8, 2018.
- Fang, Kuan, Yufei Ni, **Jiayuan He**, Zonghui Li, Shuai Mu, and Yangdong Deng. "FastLanes: An FPGA accelerated GPU microarchitecture simulator." In Computer Design (ICCD), 2013 IEEE 31st International Conference on, pp. 241-248. IEEE, 2013. **(Best paper award)**

AWARDS AND HONORS

<i>2nd place of ICCAD 2019 Cadthlon Programming Contest</i>	<i>2019</i>
<i>Calhoun Fellowship</i>	<i>2014-2017</i>
<i>Outstanding Graduate</i>	<i>2014</i>
<i>Hengda Scholarship</i>	<i>2013</i>
<i>National Scholarship</i>	<i>2012</i>

TECHNICAL SKILLS

C\C++, CUDA, Verilog, Python