Jiayuan He

Website: https://michael-jy-he.github.io/
Phone: +1-(512)-838-1423
Email: hejy@cs.utexas.edu

RESEARCH INTERESTS

Parallel Computing, GPU Computing, Graph Analytics, Placement and Routing in EDA

EDUCATION

University of Texas at Austin **Austin, TX**
PhD student, Computer Science *Sep. 2014 – Present*
Advisor: Keshav Pingali

Tsinghua University **Beijing, China**
Bachelor, Electrical Engineering *Sep. 2010 – Aug.2014*
Second Bachelor, Economics

PROFESSIONAL EXPERIENCE

University of Texas at Austin **Austin, TX**
Graduate Research Assistant *Sep. 2014 – Present*
Graph analytics on multicore CPUs and GPUs: Designed microbenchmarks to identify parallelization bottlenecks. Optimized classic graph applications, including BFS, PageRank, Connected Component and Independent Set.
Parallelization of EDA algorithms: Proposed a hybrid parallel algorithm which exploits net-level parallelism and fine-grain parallelism. Implemented ***SPRoute*** which achieves significant speedup over state-of-the-art academic global router.

Facebook **Remote**
Software Engineer Intern *May – Aug.2020*
Manager: George Meng, Mentor: Lukasz Wesolowski
Performance bottleneck investigation and optimization for ML Built a pipleline to analyze and aggregate the performance bottleneck of GPU clusters. Identified and optimized a performance bottleneck in PyTorch and saved millions of dollars worth of computing power

VMware **Palo Alto, CA**
Research Intern *May – Aug.2018*
Manager: Josh Simons, Mentor: Xin Xu

- **Characterization and prediction of performance interference on virtual GPUs:** Designed microbenchmarks to study the interference of multiple workloads on virtual GPUs. Characterized deep learning workload by low level features, which are further used to generate an interference prediction model. The work is published in HotCloud19.
- **Investigation of P2P communication malfunction on passthrough GPU in virtual environment**

Tsinghua University **Beijing, China**
Research Assistant *Oct. 2012 – Aug.2014*
Advisor: Yangdong Deng

- **FastLanes, An FPGA Accelerated GPU Microarchitecture Simulator:** Introduced a comprehensive FPGA-based GPU simulation framework. Built a simulator for GPU cache and memory.
- **de Bruijn Graph Construction on GPUs:** Implemented the first de Bruijn graph construction program on GPU with a speedup of 200X over CPU.

PUBLICATIONS

- **Jiayuan He**, Udit Agarwal, Yihang Yang, Rajit Manohar, Keshav Pingali. "SPRoute 2.0: A detailed-routability-driven deterministic parallel global router with soft capacity." IEEE Asia and South Pacific Design Automation Conference (ASPDAC), 2022
- **Jiayuan He**, Wenmian Hua, Yi-Shan Lu, Sepideh Maleki, Yihang Yang, Keshav Pingali, and Rajit Manohar. "Interact: An Interactive Design Environment for Asynchronous Logic." Workshop on Open-Source EDA Technology (WOSET), November 2021.
- Samira Ataei, Wenmian Hua, Yihang Yang, Rajit Manohar, Yi-Shan Lu, **Jiayuan He**, Sepideh Maleki, and Keshav Pingali. "An Open-Source EDA Flow for Asynchronous Logic." IEEE Design & Test 38, no. 2 (2021): 27-37.
- Udit Agarwal, Samira Ataei, **Jiayuan He**, Wenmian Hua, Yi-Shan Lu, Sepideh Maleki, Yihang Yang, Keshav Pingali, Rajit Manohar. "A Digital Flow for Asynchronous VLSI Systems: Status Update. " Workshop on Open-Source EDA Technology (WOSET), November 2020.
- **Jiayuan He**, Yihang Yang, Rajit Manohar. "A power router for gridded cell placement." Workshop on Open-Source EDA Technology (WOSET), November 2020.
- Yihang Yang, **Jiayuan He**, and Rajit Manohar. "Dali: A gridded cell placement flow." Workshop on Open-Source EDA Technology (WOSET), November, 2020.
- **Jiayuan He**, Martin Burtscher, Rajit Manohar, and Keshav Pingali. "SPRoute: A Scalable Parallel Negotiation-based Global Router." In 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1-8. IEEE, 2019.
- **Jiayuan He**, Martin Burtscher, Rajit Manohar, Keshav Pingali. "SPRoute: A Scalable Parallel Negotiation-based Global Router. " Work-in-progress session, Design Automation Conference, June 2019.
- Xin Xu, Na Zhang, Michael Cui, **Jiayuan He**, and Ridhi Surana. "Characterization and prediction of performance interference on mediated passthrough GPUs for interference-

aware scheduler." In 11th {USENIX} Workshop on Hot Topics in Cloud Computing (HotCloud 19). 2019.

- Samira Ataei, **Jiayuan He**, Wenmian Hua, Yi-Shan Lu, Sepideh Maleki, Yihang Yang, Keshav Pingali, and Rajit Manohar. "Toward a digital flow for asynchronous VLSI systems." In 2nd Workshop on Open-Source EDA Technology (WOSET), Westminster, CO, November 9, 2019.
- Yi-Shan Lu, Samira Ataei, **Jiayuan He**, Wenmian Hua, Sepideh Maleki, Yihang Yang, Martin Burtscher, Keshav Pingali, and Rajit Manohar. "Parallel Tools for Asynchronous VLSI Systems." In 1st Workshop on Open-Source EDA Technology (WOSET), San Diego, CA, November 8, 2018.
- Kuan Fang, Yufei Ni, **Jiayuan He**, Zonghui Li, Shuai Mu, and Yangdong Deng. "FastLanes: An FPGA accelerated GPU microarchitecture simulator." In Computer Design (ICCD), 2013 IEEE 31st International Conference on, pp. 241-248. IEEE, 2013. (**Best paper award**)

PATENTS

- Xin Xu, Na Zhang, C. U. I. Xiaolong, **Jiayuan He**, and Ridhi Surana. "Interference-aware scheduling service for virtual GPU enabled systems." U.S. Patent 11,113,093, issued September 7, 2021.

AWARDS AND HONORS

2nd place of ICCAD 2019 Cadthlon Programming Contest — *2019*
Calhoun Fellowship — *2014-2017*
Outstanding Graduate — *2014*
Hengda Scholarship — *2013*
National Scholarship — *2012*
Tongfang Scholarship — *2010*

TECHNICAL SKILLS

C\C++, CUDA, Verilog, Python