DIGITAL DESIGN

ASSIGNMENT 4

Deadline: *22:30, Wednesday 29 December 2021*

Lab sessions & Location:

1. **Lychee Garden 6, Room 409 (Wednesday 14:00-15:50 pm)**
2. **Lychee Garden 6, Room 404 (Thursday 10:10-12:10 am)**
3. **Teaching Building 2, Room 205 (Friday 10:10-12:10 am)**
4. **Lychee Garden 6, Room 402 (Friday 14:00~15:50 pm)**

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Write down the characteristic tables of both JK flip-flop and T flip-flop. Based on the characteristic table, write down their characteristic equations. (Use character T, J, K, Q, Q_{t+1})

2. A sequential circuit has two JK flip-flops A and B, and one input x. The circuit is described by the following flip-flop input equations:

$$J_A = x', \quad K_A = B$$

$$J_B = x, \quad K_B = A'$$

   a. Derive the state equations A(t+1) and B(t+1) by substituting the input equations for the J and K variables.
   b. Draw the state diagram of the circuit.

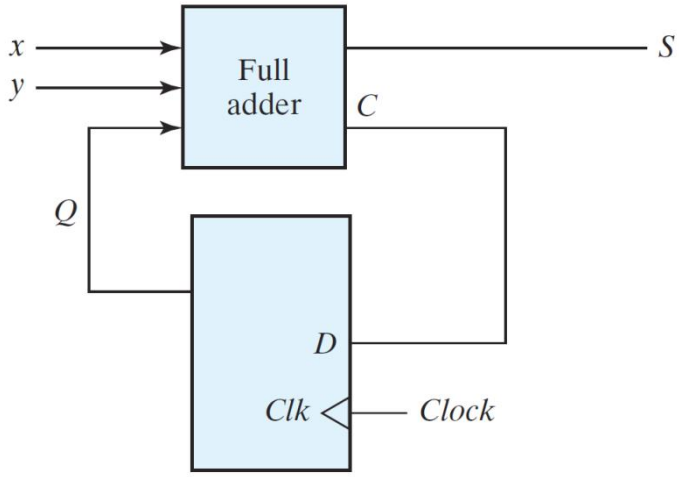
3. Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 4, 6, 7, 3, 1. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design.

   Requirements: please show your process, including the state table, the input equation of each T flip-flop, and the circuit diagram. Then explain why the counter may not operate properly.

   For the correction, please explain your idea by showing the state diagrams before and after correction.

4. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in the figure. For the full adder, x and y are the addend and augend, Q is the carry in, S is the

sum, C is the carry out. Write the Boolean equations for S, C, D and Q. Derive the state table and state diagram of the sequential circuit.



5. Design a serial 2's complementer with a shift register and a D flip-flop. The binary number is shifted out from one side and its 2's complement shifted into the other side of the shift register.
   Please first write the state diagram of the complementer. Derive the state table where each state is coded using binary values. Then write the input equation and output equation of the D flip-flop. Finally draw the circuit diagram.
   Hint: - 2's complement of a number can be obtained by keeping the least significant bits as such until the first 1, and then complementing all bits
   eg: 001010 → 110110

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys Practice platform (xilinx FPGA chip artix 7 inside) to design sequential circuits and test them.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1. 'CH5-Synchronous Sequential Logic-SUSTC.ppt' in BlackBoard site.
2. 'Digital design lab10', 'Digital design lab11','Digital design lab12' , 'Digital design lab13','Digital design lab14' in BlackBoard site.
3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1: A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations:

$$J_A = x', \ K_A = B$$
$$J_B = x, \ K_B = A'$$

Implement the sequential circuit in verilog.

- Do the design.
  - i. Step1: Implement the JK flip-flop (sensitive to positive edge of clock. an asynchronous reset signal which is low level active)
  - ii. Step2: Implement the sequential circuit in Task1 by using the JK flip-flop which is asked at the step1 in this task.
- Write testbench to verify the function of your design.
  - i. Verify the function of JK flip-flop
  - ii. Verify the function of the sequential circuit in Task1-step2.

TASK2:

Use one 74195 to implement a 4-bits JOHNSON-COUNTER which is described on "Digital design lab14.pdf".

Implement the sequential circuit in verilog.

- Do the design.
  - i. Step1: Implement 74195 which is described in lab13 slides.
  - ii. Step2: Implement a 4-bits JOHNSON-COUNTER by using one chip of 74195 which is asked at the step1 in this task.

- Write testbench to verify the function of your design.
    i. Verify the function of 74195
    ii. Verify the function of the sequential circuit in Task2-step2.

TASK3:

Implement a subtitles interchanging displaying 'CS207' and '2021F' on the tubes of Minisys board. It is asked to use a switch to control the showing on the tubes: while the switch is on, showing 'CS207', while the switch is off, showing '2021F'.

- Do the design by using structure design:
    - There MUST be 3 modules: 1st one is used to generate a special clock(frequency divider), 2nd one which using the clock generated by the 1nd module to control the showing on the tubes. 3rd one is the top module which instance two modules and do the connection.
- Create the constraint file.
- Do the synthetic and implementation, generate the bitstream file and program the device, then test the circuit on the Minisys board.

SUBMISSION

Submit your assignment report to the BlackBoard on *Corresponding site* ("Digital Logic Fall 2021(Lab)" by the deadline. NOTE: There is ONLY 1 DDL on BlackBoard.

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 40%

Question 1	8
Question 2	8
Question 3	10
Question 4	10

Question 5	10
Total	46 marks

Lab: 60%

Task 1: Design of JK flip-flop in Verilog	5 marks
Task 1: Design of task1-step2 in Verilog(using JK flip-flop is asked)	5 marks
Task 1: Test bench in Verilog, simulation result and its description on JK flip-flop and task1-step2.	4*2 marks
Task 2: Design of 74195 in Verilog	5 marks
Task 2: Design of task2-step2 in Verilog(using 74195 is asked)	5 marks
Task 2: Test bench in Verilog, simulation result and its description on 74195 and task2-step2.	4*2 marks
Task 3: Design of module 1, 2 and 3 in task3.	10 marks
Task 3: Constrains file, the photos and description of the test result on Minisys practice board.	4*2 marks
Total	54 marks

The template for the report could be found on blackboard site “Digital Logic Fall 2021(Lab)”.