

# 1. JK flip-flop

characteristic table

J	K	$Q_{t+1}$	
0	0	$Q_t$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q_t'$	Complement

characteristic equation

$$Q_{t+1} = JQ_t' + K'Q_t$$

# T flip-flop

characteristic table

T	$Q_{t+1}$	
0	$Q_t$	No change
1	$Q_t'$	Complement

$$Q_{t+1} = T \oplus Q_t$$

$$Q_{t+1} = JQ_t' + K'Q_t$$

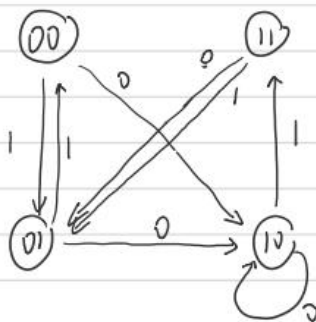
$$J_A = X' \quad K_A = B$$

$$2. \quad a. \quad A_{t+1} = X'A_t' + B'A_t$$

$$J_B = X \quad K_B = A'$$

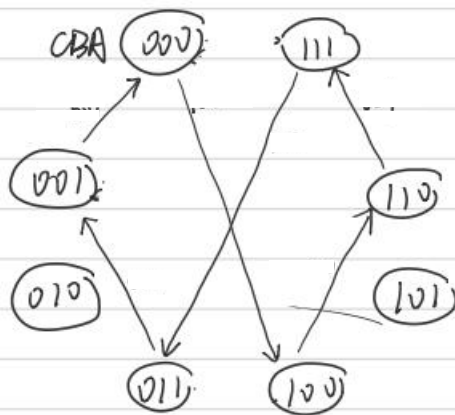
$$B_{t+1} = X B_t' + A_t B_t$$

b	Present		Input	Next		FF inputs			
	A	B	X	A	B	$J_A$	$K_A$	$J_B$	$K_B$
	0	0	0	1	0	1	0	0	1
	0	0	1	0	1	0	0	1	1
	0	1	0	1	0	1	1	0	1
	0	1	1	0	0	0	1	1	1
	1	0	0	1	0	1	0	0	0
	1	0	1	1	1	0	0	1	0
	1	1	0	0	1	1	1	0	0
	1	1	1	0	1	0	1	1	0



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Present State			Next State			Flip-Flop Inputs		
C(t)	B(t)	A(t)	C(t+1)	B(t+1)	A(t+1)	TC	TB	TA
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	0	0	1
0	1	0	x	x	x	x	x	x
0	1	1	0	0	1	0	1	0
1	0	0	1	1	0	0	1	0
1	0	1	x	x	x	x	x	x
1	1	0	1	1	1	0	0	1
1	1	1	0	1	1	1	0	0



	TC		BA	
	00	01	11	10
C	0	1	0	0
	1	0	x	1

$$T_C = A'C' + AC$$

	TB		BA	
	00	01	11	10
C	0	0	0	1
	1	1	x	0

$$T_B = B'C + BC'$$

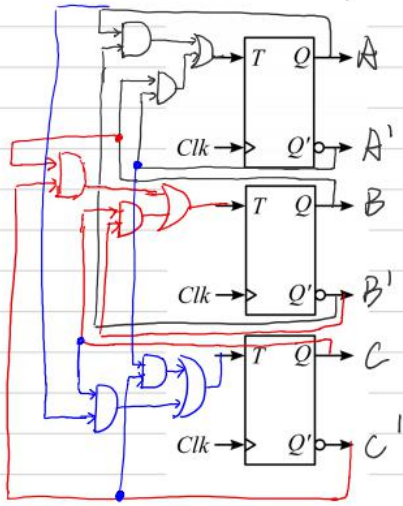
	TA		BA	
	00	01	11	10
C	0	0	1	0
	1	0	x	1

$$T_A = AB' + A'B$$

Explanation of why the counter may not operate properly.

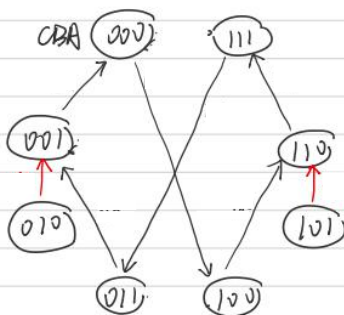
Because when 010 the  $\{T_C, T_B, T_A\} = 3'b111$ , then the output is 101.

When 101, the  $\{T_C, T_B, T_A\} = 3'b111$ , then the output is 010. It goes the cycle.



After

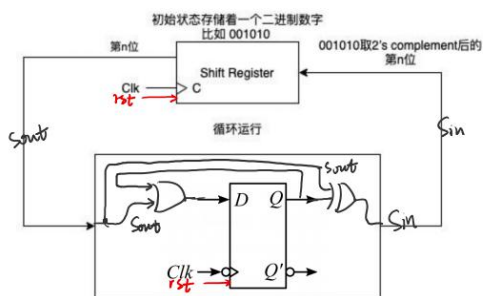
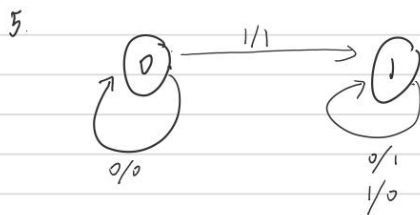
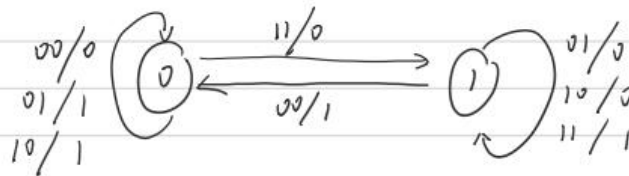
Present State			Next State			Flip-Flop Inputs		
C(t)	B(t)	A(t)	C(t+1)	B(t+1)	A(t+1)	TC	TB	TA
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	0	0	1
0	1	0	x 0	x 0	x 1	x 0	x 1	x 1
0	1	1	0	0	1	0	1	0
1	0	0	1	1	0	0	1	0
1	0	1	x 1	x 1	x 0	x 0	x 1	x 1
1	1	0	1	1	1	0	0	1
1	1	1	0	1	1	1	0	0



Explanation of idea: When the counter reaches 010 or 101, let them go into the correct cycle.

4.

Present	Input		Next	Output		
$k_t$	$x$	$y$	$k_{t+1}$	$S$	$C$	
0	0	0	0	0	0	$S = x \oplus y \oplus k$
0	0	1	0	1	0	$C = xy + \bar{x}y + kx$
0	1	0	0	1	0	$D = xy + \bar{x}y + kx$
0	1	1	1	0	1	$k_{t+1} = xy + \bar{x}y + kx$
1	0	0	0	1	0	
1	0	1	1	0	1	
1	1	0	1	0	1	
1	1	1	1	1	1	



The initial stored in D flip-flop is 0

$S_{out}$  is the output of the shift register.

$S_{in}$  is the input of the shift register

$k_t$	$S_{out}$	$S_{in}$	$k_{t+1}$
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	1

input equation

$$D = S_{out} + k_t$$

output equation

$$S_{in} = S_{out} \oplus k_t$$

## Task 1: Design of JK flip-flop in Verilog