DIGITAL DESIGN

ASSIGNMENT REPORT

ASSIGNMENT ID: 2

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PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

1. a) Consider four midterms: m_i, m_j, m_k, m_l.

   Suppose both F1 and F2 contains m_i, then F1+F2 also contains the m_i.

   Suppose F1 contains m_j but F2 doesn't contain m_j, then F1+F2 contains m_j.

   Suppose F2 contains m_k but F1 doesn't contain m_k, then F1+F2 contains m_k.

   Suppose both F1 and F2 doesn't contain m_l, then F1+F2 doesn't contain m_l.

   In conclusion, E=F1+F2 contains the sum of the minterms of F1 and F2.

   b) Consider four midterms: m_i, m_j, m_k, m_l.

   Suppose both F1 and F2 contains m_i, then F1·F2 also contains the m_i.

   Suppose F1 contains m_j but F2 doesn't contain m_j, then F1·F2 doesn't contains m_j.

   Suppose F2 contains m_k but F1 doesn't contain m_k, then F1·F2 doesn't contains m_k.

   Suppose both F1 and F2 doesn't contain m_l, then F1·F2 doesn't contain m_l.

   In conclusion, E=F1·F2 contains the common of the minterms of F1 and F2.

2. a) $F(x,y,z)=\Pi(0,1,2,4,6)$

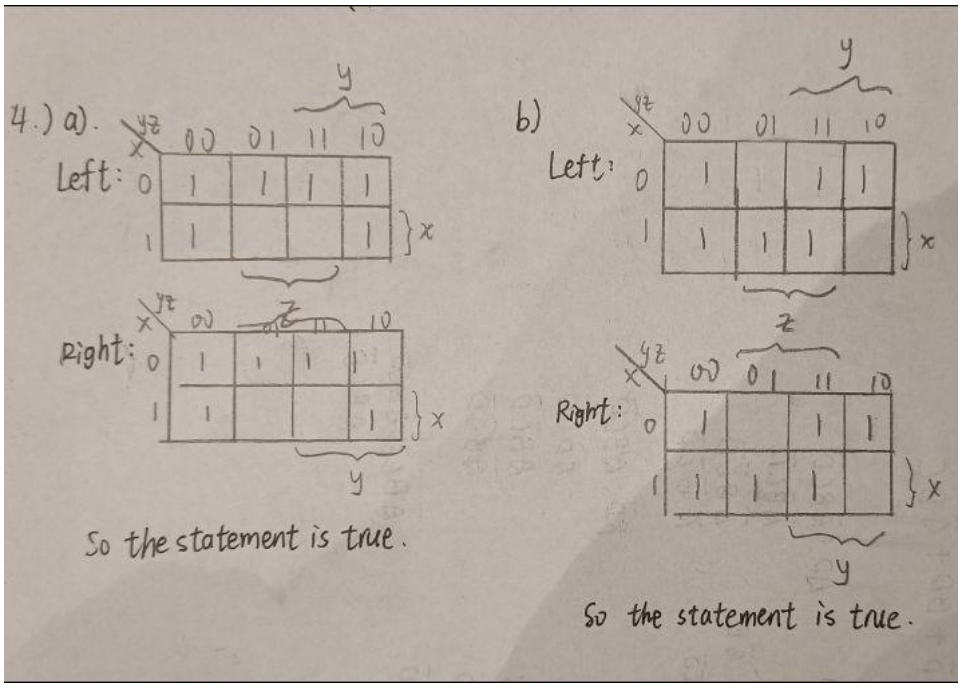
   b) $F(A,B,C,D)=\Sigma(0,1,2,4,6,7,9,10,13,14)$

3. a)

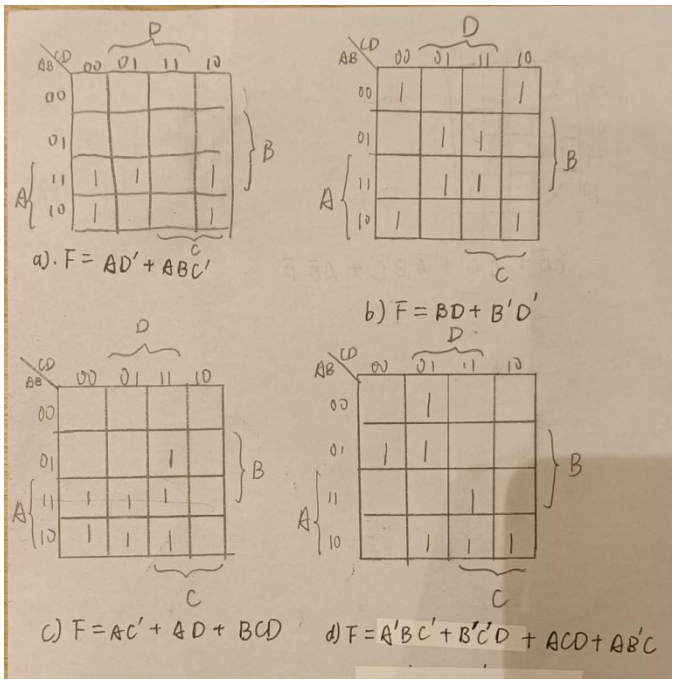
   a'b'c'd'+a'b'c'd+a'b'cd+a'b'cd'+a'bc'd+a'bcd+abcd+ab'cd+ab'cd'=a'b'+cd+a'd

   b) (x'+y+z)(x'+y+z')(x+y+z')=(x'+y)(y'+z)

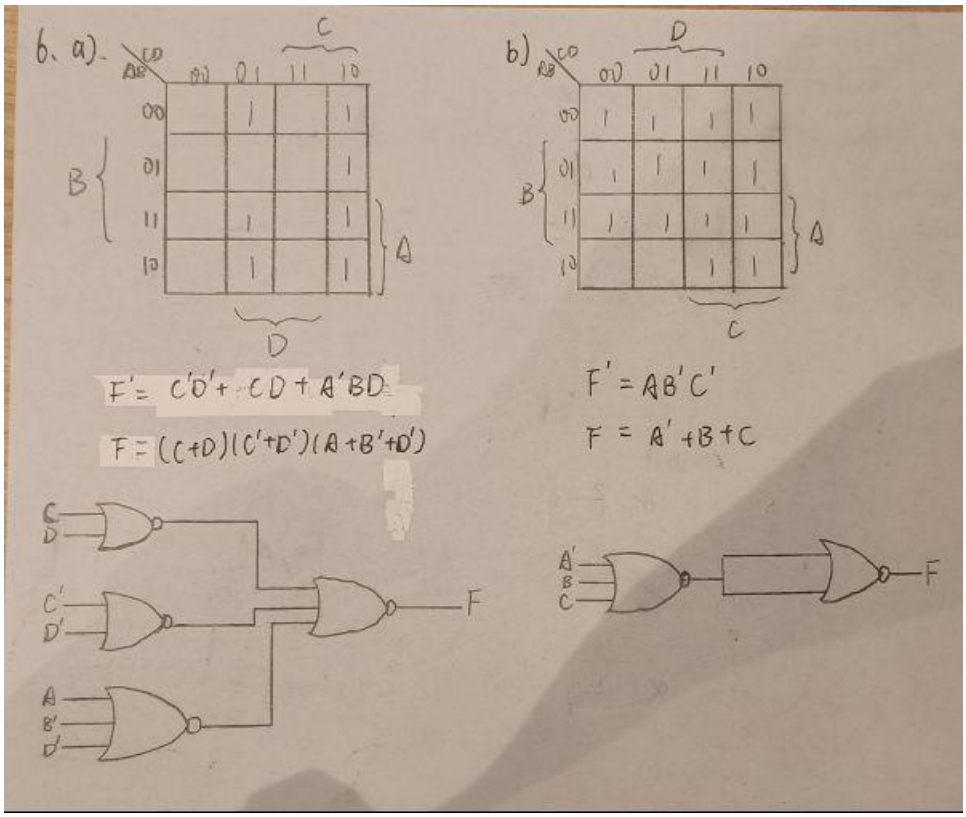
4.


4.) a).
Left:
Right:
So the statement is true.
b)
Left:
Right:
So the statement is true.

5.


a). F = AD' + ABC'
b) F = BD + B'D'
c) F = AC' + AD + BCD
d) F = A'BC' + B'C'D + ACD + AB'C

6.



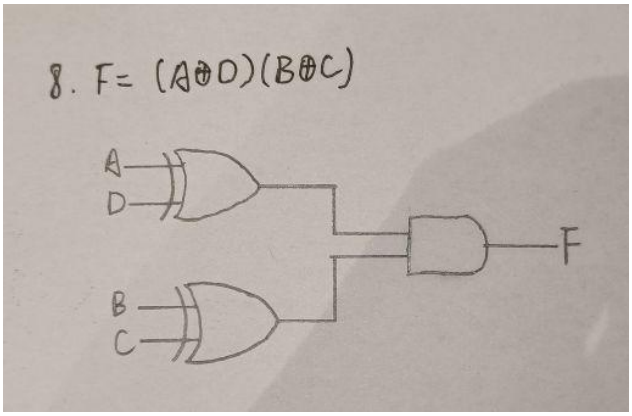
7. a)

F=C’D’+A’BC+B’D’=A’B’C’D’+A’BC’D’+ABC’D’+AB’C’D’+A’B’CD’+A’BCD+A’BCD’+AB’CD’

b)

F=A’C’+AD’+B’D’=A’B’C’D’+A’B’C’D+A’B’CD’+A’BC’D’+A’BC’D+ABC’D’+ABCD’+AB’C’D’+AB’CD’

8.



PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2021/11/15 21:22:03
// Design Name:
// Module Name: t1
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module t1(
input sw,
input[0:3] bell,
output reg [7:0] seg_out,
output    [7:0] seg_en
```

```
    );
assign seg_en=8'b1111_1110;
always @*
begin
    casez(sw)
        1'b1:
            casez(bell)
                4'bzzz1: seg_out=8'b1011_0000;   // 3
                4'bzz10: seg_out=8'b1010_0100;   // 2
                4'bz100: seg_out=8'b1111_1001;   // 1
                4'b1000: seg_out=8'b1100_0000;   // 0
                default: seg_out=8'b1111_1111;   //none
            endcase

        1'b0:
            casez(bell)
                4'b1zzz: seg_out=8'b1100_0000;   // 0
                4'b01zz: seg_out=8'b1111_1001;   // 1
                4'b001z: seg_out=8'b1010_0100;   // 2
                4'b0001: seg_out=8'b1011_0000;   // 3
                default: seg_out=8'b1111_1111;
            endcase
    endcase
end
endmodule
```

CONSTRAINT FILE AND THE TESTING

```
set_property IOSTANDARD LVCMOS33 [get_ports {seg_out[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_out[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_out[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_out[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_out[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_out[5]}]
```

```
set_property IOSTANDARD LVCMOS33 [get_ports {seg_out[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_out[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_en[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_en[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_en[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_en[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_en[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_en[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_en[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_en[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw}]
set_property IOSTANDARD LVCMOS33 [get_ports {bell[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {bell[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {bell[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {bell[3]}]
set_property PACKAGE_PIN Y9 [get_ports {sw}]
set_property PACKAGE_PIN W9 [get_ports {bell[0]}]
set_property PACKAGE_PIN Y7 [get_ports {bell[1]}]
set_property PACKAGE_PIN Y8 [get_ports {bell[2]}]
set_property PACKAGE_PIN AB8 [get_ports {bell[3]}]
set_property PACKAGE_PIN E13 [get_ports {seg_out[7]}]
set_property PACKAGE_PIN C15 [get_ports {seg_out[6]}]
set_property PACKAGE_PIN C14 [get_ports {seg_out[5]}]
set_property PACKAGE_PIN E17 [get_ports {seg_out[4]}]
set_property PACKAGE_PIN F16 [get_ports {seg_out[3]}]
set_property PACKAGE_PIN F14 [get_ports {seg_out[2]}]
set_property PACKAGE_PIN F13 [get_ports {seg_out[1]}]
set_property PACKAGE_PIN F15 [get_ports {seg_out[0]}]
set_property PACKAGE_PIN A18 [get_ports {seg_en[7]}]
set_property PACKAGE_PIN A20 [get_ports {seg_en[6]}]
set_property PACKAGE_PIN B20 [get_ports {seg_en[5]}]
set_property PACKAGE_PIN E18 [get_ports {seg_en[4]}]
set_property PACKAGE_PIN F18 [get_ports {seg_en[3]}]
```

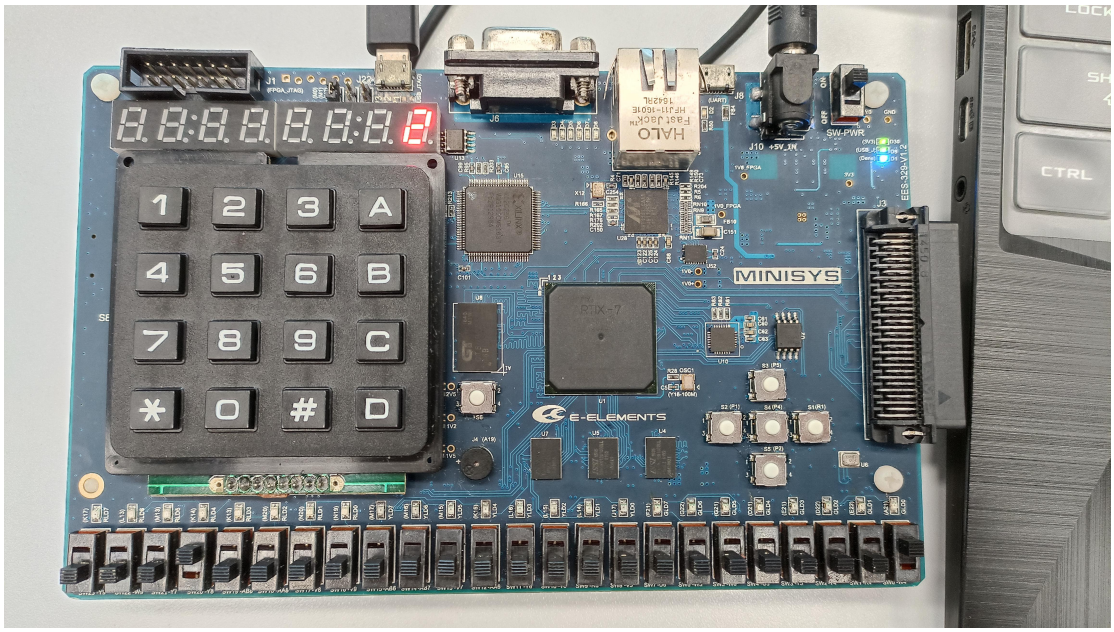
set_property PACKAGE_PIN D19 [get_ports {seg_en[2]}]

set_property PACKAGE_PIN E19 [get_ports {seg_en[1]}]

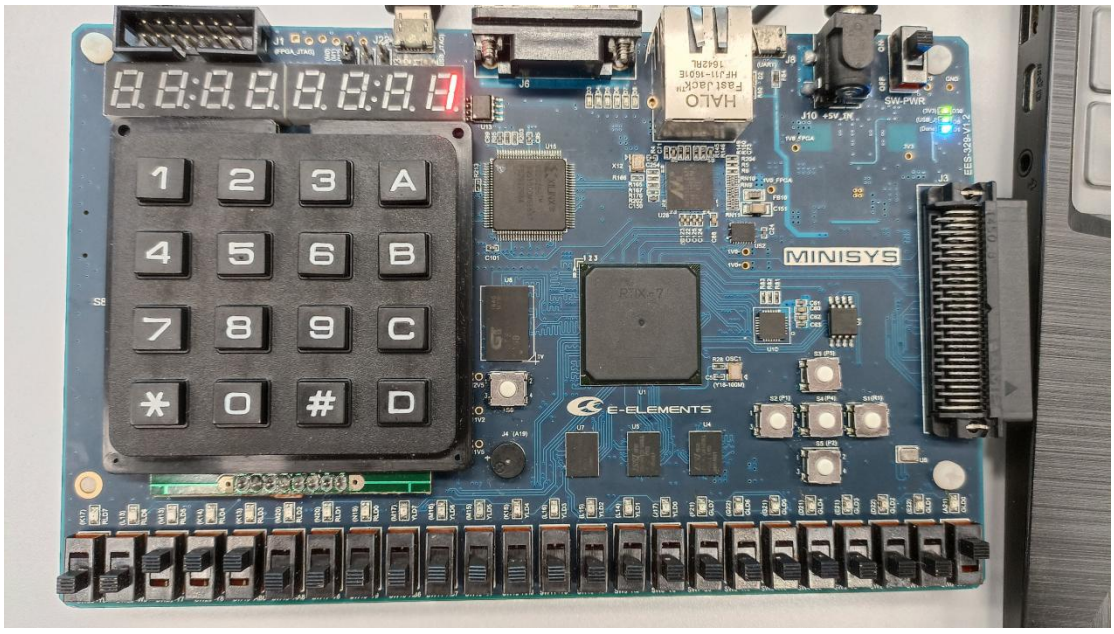
set_property PACKAGE_PIN C19 [get_ports {seg_en[0]}]

THE DESCRIPTION OF OPERATION

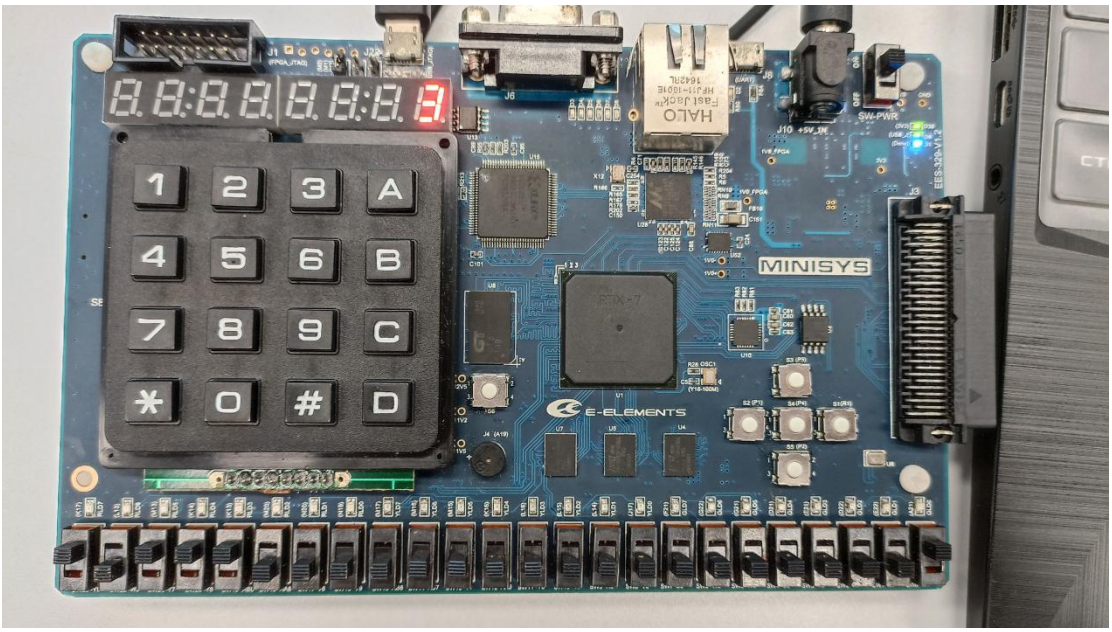
Test 1: Only bell 2 is turned on, then 7-seg tube shows 2.



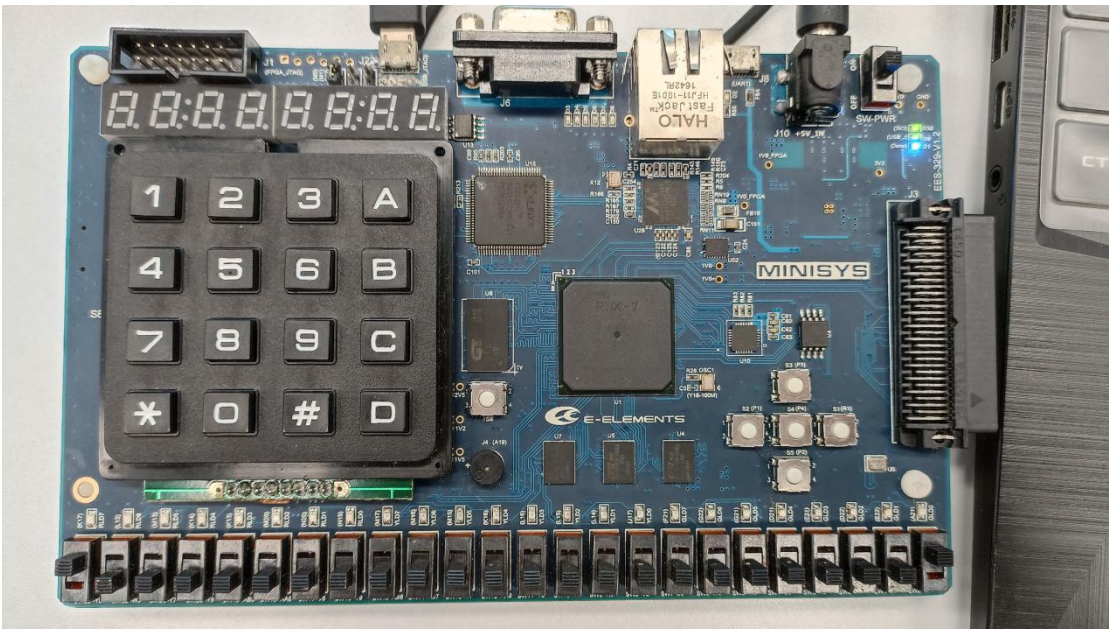
Test 2: Both bell 1,2,3 are turned on while the priority order is set as priority increases as the number decreases. The 7-seg tubes shows 1.



Test 3: Both bell 1,2,3 are turned on while the priority order is set as priority increases as the number decreases. The 7-seg tubes shows 3.



Test 4: None of bell is turned on. The 7-seg tubes shows nothing.



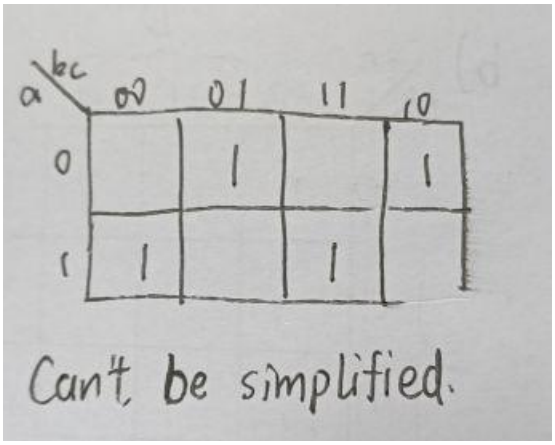
PART 2: DIGITAL DESIGN LAB (TASK2)

TRUTH TABLE AND K-MAP

Truth table:

a	b	a^b	c	a^b^c
T	T	F	T	T
T	T	F	F	F
T	F	T	T	F
T	F	T	F	T
F	T	T	T	F
F	T	T	F	T
F	F	F	T	T
F	F	F	F	F

K-map:



DESIGN

`timescale 1ns / 1ps

```
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2021/11/16 11:50:56
// Design Name:
// Module Name: t2
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module t2(
    input a,
    input b,
    input c,
    output reg o1,
    output reg o2
    );
    always@* begin
        o1 = (a & ~b & ~c) | (a & b & c) | (~a & ~b & c) | (~a & b & ~c);
        o2 = (a | b | c) & (a | ~b | ~c) & (~a | b | ~c) & (~a | ~b | c);
    end
endmodule
```

SIMULATION

The code of simulation file is below:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2021/11/16 11:55:51
// Design Name:
// Module Name: t2_sim
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module t2_sim(

    );
    reg a,b,c;
    wire o1,o2;

    t2 u2(a,b,c,o1,o2);
```

```
    initial begin
        {a,b,c} = 3'b000;
        repeat(8) begin
            #10;
            {a,b,c} = {a,b,c} + 1;
        end
        $finish;
    end
endmodule
```

The simulation result is below:

From 0 to 10ns, the value of a,b,c is 0,0,0 respectively, and the truth of output are both 0.

From 10 to 20ns, the value of a,b,c is 0,0,1 respectively, and the truth of output are both 1.

From 20 to 30ns, the value of a,b,c is 0,1,0 respectively, and the truth of output are both 1.

From 30 to 40ns, the value of a,b,c is 0,1,1 respectively, and the truth of output are both 0.

From 40 to 50ns, the value of a,b,c is 1,0,0 respectively, and the truth of output are both 1.

From 50 to 60ns, the value of a,b,c is 1,0,1 respectively, and the truth of output are both 0.

From 60 to 70ns, the value of a,b,c is 1,1,0 respectively, and the truth of output are both 0.

From 70 to 80ns, the value of a,b,c is 1,1,1 respectively, and the truth of output are both 1.

The total result of simulation satisfy the truth-table above.

THE DESCRIPTION OF OPERATION

(This part is always REQUIRED unless you can get full marks for this lab task)

Forget the meaning of the symbol “^” in verilog language and how to use K-map to simplify the functions. So I turn back to textbook and check the previous PPT. Then figure it out easily.