DIGITAL DESIGN

ASSIGNMENT 3

Deadline: *22:30, Wednesday 15 December 2021*

Lab sessions & Location:

1. **Lychee Garden 6, Room 409 (Wednesday 14:00-15:50 pm)**
2. **Lychee Garden 6, Room 404 (Thursday 10:10-12:10 am)**
3. **Teaching Building 2, Room 205 (Friday 10:10-12:10 am)**
4. **Lychee Garden 6, Room 402 (Friday 14:00~15:50 pm)**

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Implement the following Boolean function F, using the two-level forms of logic: (a) AND-OR, (b) NOR-OR, (c) NAND-NAND, (d) OR-AND, (e) NOR-NOR, and (f) NAND-AND: F(A, B, C, D) = ∑ (0, 1, 5, 8, 9, 10, 11, 13, 15)

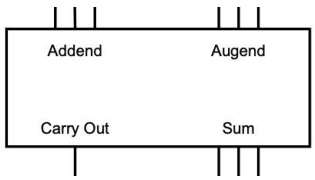
Notice that you only need to write the logic equation, no drawing needed.
Tips: It may be much easier to first use Karnaugh maps to minimise the Boolean function, but using Karnaugh maps is not compulsory.

2. Derive the circuits for a four-bit parity generator and a three-bit parity checker using an odd parity bit. Write the truth table, simplify your logic equation and draw circuit diagram using minimal number of gates. The parity generator has 4 inputs, A, B, C, and D. The parity checker has also 4 inputs, A, B, C and P.

3. Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. When the binary input is 0, 1, 2 or 3, the binary output is two greater than the input. Write the truth table and logic formula for each output, then draw the circuit diagram.

4. For a binary multiplier that multiplies two unsigned **three-bit** numbers, use AND gates and adders, design the circuit. Briefly describe your design and list the logic formulas. Draw the circuit diagram. For the adder, you can just use a block diagram with ports to represent them, as the figure below.

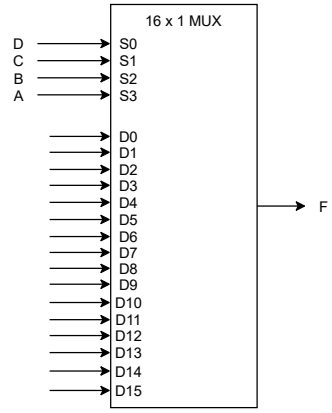
Tips: You can write the signal name next to ports of gates/adders, to avoid drawing long wires.



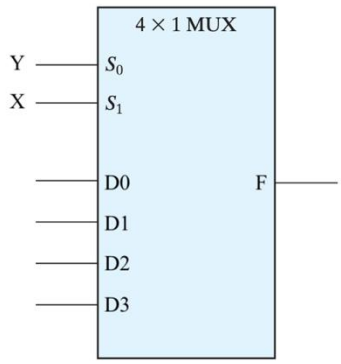
A 3-bit adder

5. Implement the following Boolean function with a 16x1 multiplexer: (a) F(A, B, C, D) =∑ (1, 3, 5, 8, 10, 14)， (b) F(A, B, C, D) = Π (4, 7, 11)

Suppose we use the multiplexer shown below, and connect the selection inputs as: S3=A, S2=B, S1=C, S0=D. If ABCD=0001, then F=D1. You only need to specify what signals should be connected to input ports D0 through D15. No drawings needed.



6. Implement a full subtractor circuit with two **4x1 multiplexers**. A full subtractor has three inputs X, Y, B_{in}, and two outputs $Diff$ and B_{out}. The circuit subtracts $X - Y - B_{in}$, where B_{in} is the input borrow, B_{out} is the output borrow, and $Diff$ is the difference. The 4x1 multiplexer is shown below. If $S_1S_0 = 01$, then $F = D1$. You should connect the selection ports as $S_1 = X$ and $S_0 = Y$. The outputs of the two multiplexers are $F = B_{out}$ and $F = Diff$ respectively. Write down the truth table and draw the circuit diagram.



PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys develop platform (xilinx FPGA chip artix 7 inside) to design a combinational logic circuit and do the testing.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1.'CH3-Minimisation-SUSTC-new.ppt' and 'CH4-COMBINATIONAL LOGiC.ppt' in Blackboard site.

2. 'Digital design lab8', 'Digital design lab9' in Blackboard site.

3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1:

Implement a 4-16 decoder with two 74138 decoders.

- Do the design.
    i. Implement a 74138 decoder 1st
    ii. Implement a 4-16 decoder using 74138 decoder which is asked at the 1st step
- Write test bench to verify the function of your design.
    i. Verify the function of 74138 decoder
    ii. Verify the function of 4-16 decoder
- Create the constraint file about 4-16 decoder.
- Do the synthesis and implementation, generate the bitstream file and program the device, then test on the Minisys develop board.

TASK2:

Use 74151(8-to-1-line multiplexer) realize the following logic function: Y = A'B'C'D' + BD + AC + B'CD' + A'B'D' .

- Do the design.
  - Implement 74151 in verilog module named mux74151
  - Realize the logic function:

    Y = A'B'C'D' + BD + AC + B'CD' + A'B'D' in two ways:

    a) Using data flow in verilog module named func_df

    b) Using one 74151 in verilog module named func_1mux

    c) Using two 74151 in verilog module named func_2mux
- Write testbench to verify the function of your design.
  - Verify the function of 74151
  - Verify the function of module func_df, func_1mux and func_2mux (build one testbench, instance 3 modules: func_df, func_1mux and func_2mux, these 3 modules share the same inputs)

SUBMISSION

Submit your assignment report to the BlackBoard on *Corresponding site* ("Digital Logic Fall 2021(Lab)" by the deadline. NOTE: There is ONLY 1 DDL on BlackBoard.

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 40%

Question 1	12
Question 2	8
Question 3	4
Question 4	8
Question 5	4
Question 6	4
Total	40 marks

Lab: 60%

Task 1: Design in Verilog	5 *2 marks
Task 1: Test bench in Verilog,simulation result and its description	5 *2 marks
Task 1: Constrains file	5 marks
Task 1: Photos about test result on Minisys develop board and description on inputs and outputs. 4 test at least	5 marks
Task 2: Design in Verilog	5*4 marks
Task 2: Test bench in Verilog, simulation result and its description	5*2 marks
Total	60 marks