PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

1.

AB \ CD	00	01	11	10
00	m_0 1	m_1 1	m_3	m_2
01	m_4	m_5 1	m_7	m_6
11	m_{12}	m_{13} 1	m_{15} 1	m_{14}
10	m_8 1	m_9 1	m_{11} 1	m_{10} 1

According to K-map:

$m_0 + m_1 + m_8 + m_9 = B'C'$

$m_1 + m_5 + m_{13} + m_9 = C'D$

$m_{13} + m_{15} + m_9 + m_{11} = AD$

$m_8 + m_9 + m_{11} + m_{10} = AB'$

$\therefore$

(a) $F(A,B,C,D) = AB' + C'D + AD + B'C'$

由 $\bar{A} \cap \bar{B} = \overline{(A \cup B)}$

(b) $F(A,B,C,D) = (A'+B)' + (C+D')' + (A'+D')' + (B+C)'$

(c) $F(A,B,C,D) = [(AB')'(C'D)'(AD)'(B'C')']'$

(d) $F(A,B,C,D) = A(B'+D) + C'(B'+D)$

$= (A+C')(B'+D)$

(e) $F(A,B,C,D) = [(A+C')' + (B'+D)']'$

(f) $F(A,B,C,D) = (A'C)'(BD')'$

2. four-bit parity generator:

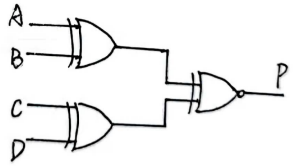
A	B	C	D	P
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

According to the truth-table, we can gain its K-map:

AB \ CD	00	01	11	10
00	m_0 1	m_1	m_3 1	m_2
01	m_4	m_5 1	m_7	m_6 1
11	m_{12} 1	m_{13}	m_{15} 1	m_{14}
10	m_8	m_9 1	m_{11}	m_{10} 1

$\therefore P = (A \oplus B \oplus C \oplus D)'$

$\therefore$ the circuit diagram:



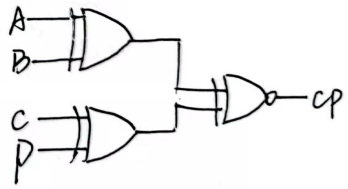
three-bit parity checker:

A	B	C	P	CP
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

like four-bit parity generator:

$CP = (A \oplus B \oplus C \oplus P)'$

the circuit diagram:

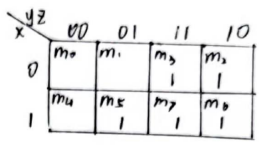


3. the truth table:

x	y	z	A	B	C
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

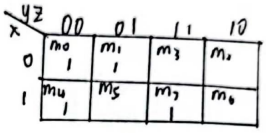
the K-map:

A:



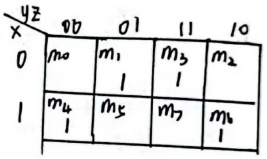
$A = y + xz$

B:



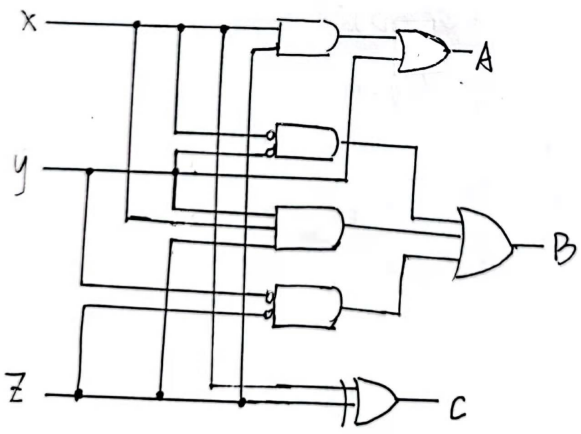
$B = yz' + xy' + xyz$

C:



$C = x'z + xz'$

the circuit diagram



4. 3-bit × 3-bit:

logic formulas:

$B_2\ B_1\ B_0$

$A_2\ A_1\ A_0$

$A_0B_2\ \ A_0B_1\ \ A_0B_0$

$A_1B_2\ \ A_1B_1\ \ A_1B_0$

$A_2B_2\ \ A_2B_1\ \ A_2B_0$

$C_5\ C_4\ C_3\ C_2\ C_1\ C_0$

description:

from the logic formula:

we know.

C_0 just needs AND, doesn't need an adder

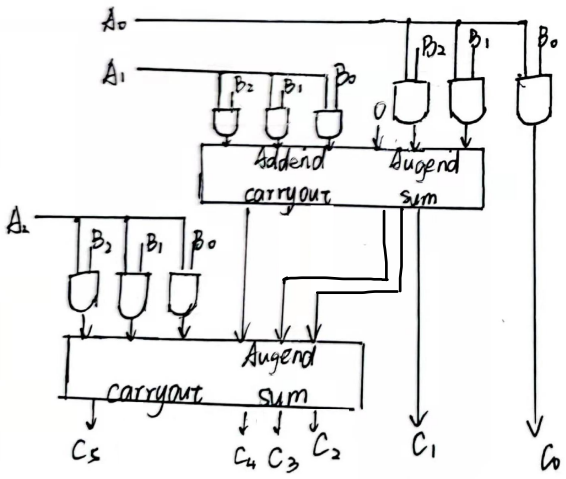
and to get $C_5\ C_4\ C_3\ C_2\ C_1$. we need two adders

one is for A_0B_2 A_0B_1 and A_1B_2 A_1B_1, A_1B_0

another is for A_2B_2 A_2B_1 A_2B_0 and the carryout from the first adder.

then. we can get the circuit diagram

the circuit diagram:



5. (a) $F(A,B,C,D) = \sum(1,3,5,8,10,14)$

1 should be connected to input ports $D_1, D_3, D_5, D_8, D_{10}, D_{14}$

0 should be connected to input ports $D_0, D_2, D_4, D_6, D_7, D_9, D_{11}, D_{12}, D_{13}, D_{15}$

(b) $F(A,B,C,D) = \prod(4,7,11)$

$= \sum(0,1,2,3,5,6,8,9,10,12,13,14,15)$

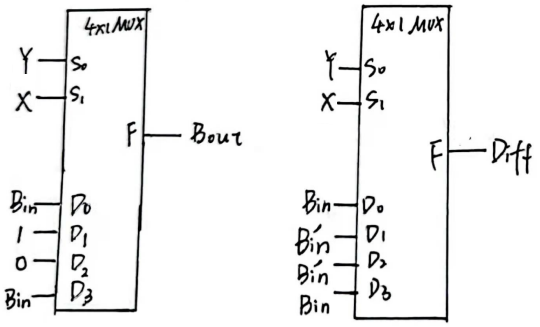
1 Should be connected to input ports $D_0\ D_1\ D_2\ D_3\ D_5\ D_6\ D_8\ D_9\ D_{10}\ D_{12}\ D_{13}\ D_{14}\ D_{15}$

0 Should be connected to input ports $D_4\ D_7\ D_{11}$

b.

X	Y	Bin	Bout	Diff
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

∴ the circuit diagram



PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*

```
module decoder_74138(A,B,C,G1,G2A_n,G2B_n,Y_n);
input A,B,C,G1,G2A_n,G2B_n;
output reg[7:0] Y_n;
always@(*) begin
if(G1==1 && G2A_n==0 && G2B_n==0)
   begin
   case({C,B,A})
   3'b000: Y_n= 8'b1111_1110;
   3'b001: Y_n= 8'b1111_1101;
```