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EECS 3201

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Prof. Allison

Video Link: https://www.youtube.com/watch?v=oSEsfG8Qtpk

Note: This Project was done by myself

Project: FPGA Digital Alarm Clock

The FPGA Digital Alarm Clock is a device that utilizes the features of the DE-10 Lite Board to create the best possible design for a clock on that form factor. The Clock contains many features such as, an adjustable and accurate clock, an alarm system complemented by a speaker, a timer that works alongside the clock, an easy to understand user interface/clock display, time zone selection (only supports UTC and all North American Time Zones), and a 12 hour time display option that work flawlessly.

Using the ten switch array, the user has the options to pause the clock, swap between display types (12 or 24 hour display), set an alarm, start/set a timer, modify current seconds, minutes, hours, or change the correct time zone selected. The other type of input is the two buttons (denoted as Key 0 and 1 on the board), which is used to either reset the clock, stop the speaker sound, or increment/decrement the values chosen.

Using the 50 MHz clock, the clock cycle was divided to send a signal every second which helps synchronize the clock with an accurate clock. In addition, the clock is used to create noise with the speaker using the arduino IO port (port 11).

Lastly, the outputs include, the six individual seven-segment displays, the LED array made of ten LEDs located above the ten switches, and the speaker mentioned prior.

References:

1-Second Long Clock:
https://www.fpga4student.com/2017/08/verilog-code-for-clock-divider-on-fpga.html

Speaker Sounds (music module):
https://www.fpga4fun.com/MusicBox2.html