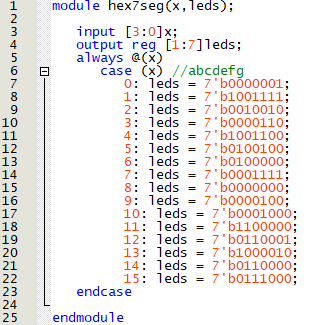
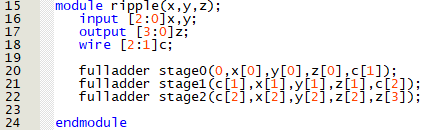
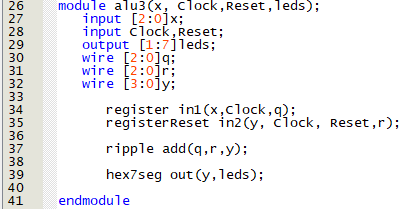
Verilog Code for 4a (The 7 seg display)



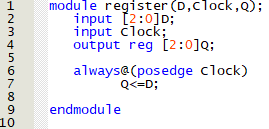
Verilog Code for 5b (3-bit ripple carry adder)



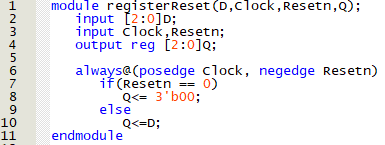
Verilog Code for 5c (alu3 – the top level file)



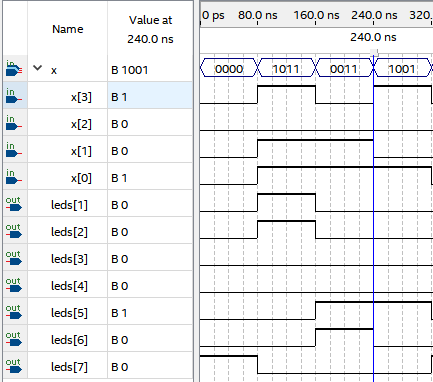
Verilog Code for 5c (register without reset)

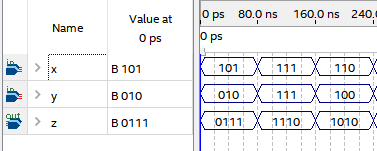


Verilog Code for 5c (register with reset)

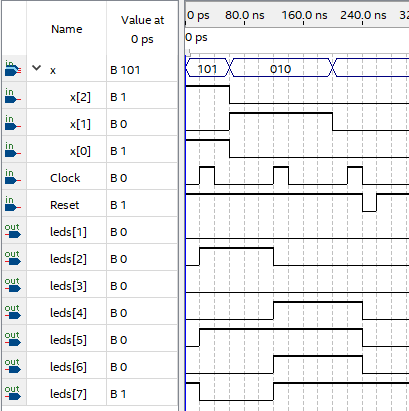


4a: hex7seg Simulation (Showing correct output for inputs 0, 11, 3, and 9)



5b: 3-bit ripple adder simulation (first 5 + 3, then 7 + 7, then 6 + 4)

5c: Alu3 Simulation (adding 5 + 2 then clearing the 7-seg display, note that the 7-seg display starts at 0)



----------------------------------Hand written simulation for 5a on the back of this page -------------------------------