

[illegible]

Input DIP

418121270808
Alt: 76SBO8T

The image displays three circuit diagrams for the RP2040 board, each showing a different configuration for a specific function. All diagrams are powered by a +3.3V supply and connected to ground (GND).

- Manual Project Clock:** This diagram shows a switch (SW1) connected to the +3.3V supply. The switch is controlled by a 1kΩ resistor (R12) connected to a signal source labeled "project_clk". The switch's other terminal is connected to a 10kΩ resistor (R7) which is then connected to GND. A 100nF capacitor (C1) is connected between the +3.3V supply and the switch's output terminal.
- Project Reset:** This diagram shows a switch (SW2) connected to the +3.3V supply. The switch is controlled by a 1kΩ resistor (R13) connected to a signal source labeled "project_rst". The switch's other terminal is connected to a 10kΩ resistor (R8) which is then connected to GND. A 100nF capacitor (C2) is connected between the +3.3V supply and the switch's output terminal.
- RP Boot Mode:** This diagram shows a switch (SW3) connected to the +3.3V supply. The switch is controlled by a 1kΩ resistor (R14) connected to a signal source labeled "boot_mode". The switch's other terminal is connected to a 10kΩ resistor (R9) which is then connected to GND. A 100nF capacitor (C3) is connected between the +3.3V supply and the switch's output terminal.

TT Carrier Power

Place C close to relevant supply

Optional "bulk"

Note: All this decoupling should be amply handled by the carrier. Would rather DNP than regret.

The diagram shows two pin headers, J4C and J4B, with their respective connections to the carrier board.

J4C Connections:

- mpr_io0 to JTAG/mio[0]
- HK_SDO to SDO/mio[1]
- HK_SDI to SDI/mio[2]
- HK_CSB to CSB/mio[3]
- HK_SCK to SCK/mio[4]
- usrclk2 to usrclk2/mio[5]
- project_clk to clk/mio[6]
- project_rst to rst/mio[7]
- in0 to ui_in[0]/mio[8]
- in1 to ui_in[1]/mio[9]
- in2 to ui_in[2]/mio[10]
- in3 to ui_in[3]/mio[11]
- in4 to ui_in[4]/mio[12]
- in5 to ui_in[5]/mio[13]
- in6 to ui_in[6]/mio[14]
- in7 to ui_in[7]/mio[15]
- out0 to uo_out[0]/mio[16]
- out1 to uo_out[1]/mio[17]
- out2 to uo_out[2]/mio[18]
- mio[37] to mio[37]
- mio[36]/ctrl_sel_rst to ctrl_sel_rst
- mio[35] to mio[35]
- mio[34]/ctrl_sel_inc to ctrl_sel_inc
- mio[33] to mio[33]
- ctrl_ena to ctrl_ena
- ui07 to ui07
- ui06 to ui06
- ui05 to ui05
- ui04 to ui04
- ui03 to ui03
- ui02 to ui02
- ui01 to ui01
- ui00 to ui00
- out7 to out7
- out6 to out6
- out5 to out5
- out4 to out4
- out3 to out3

J4B Connections:

- xcclk to XCLK CARAVEL_SCK
- TP1 to RST CARAVEL_D1
- gpio to GPIO CARAVEL_CSB
- CARAVEL_SCK to Caravel_SCK
- CARAVEL_D1 to Caravel_D1
- CARAVEL_D0 to Caravel_D0
- CARAVEL_CSB to Caravel_CSB

TT04_BREAKOUT is indicated below both headers.

Possible Comms

Pinout follows non-numerical ordering in order to support various standard communications methods between IC and projects.

In yellow, possible mappings for SPI, I2C and UART, from RP2040 perspective. See in sheet for full mapping.

Jumpers allow manual disable/reassign of output -> segments (see footprint)

PMOD host (female) headers, using digilent's numbering.

Mounting holes

MT1 MT2 MT3 MT4

GND GND GND GND

Panel-level fids for prod but included for one-offs and testing.

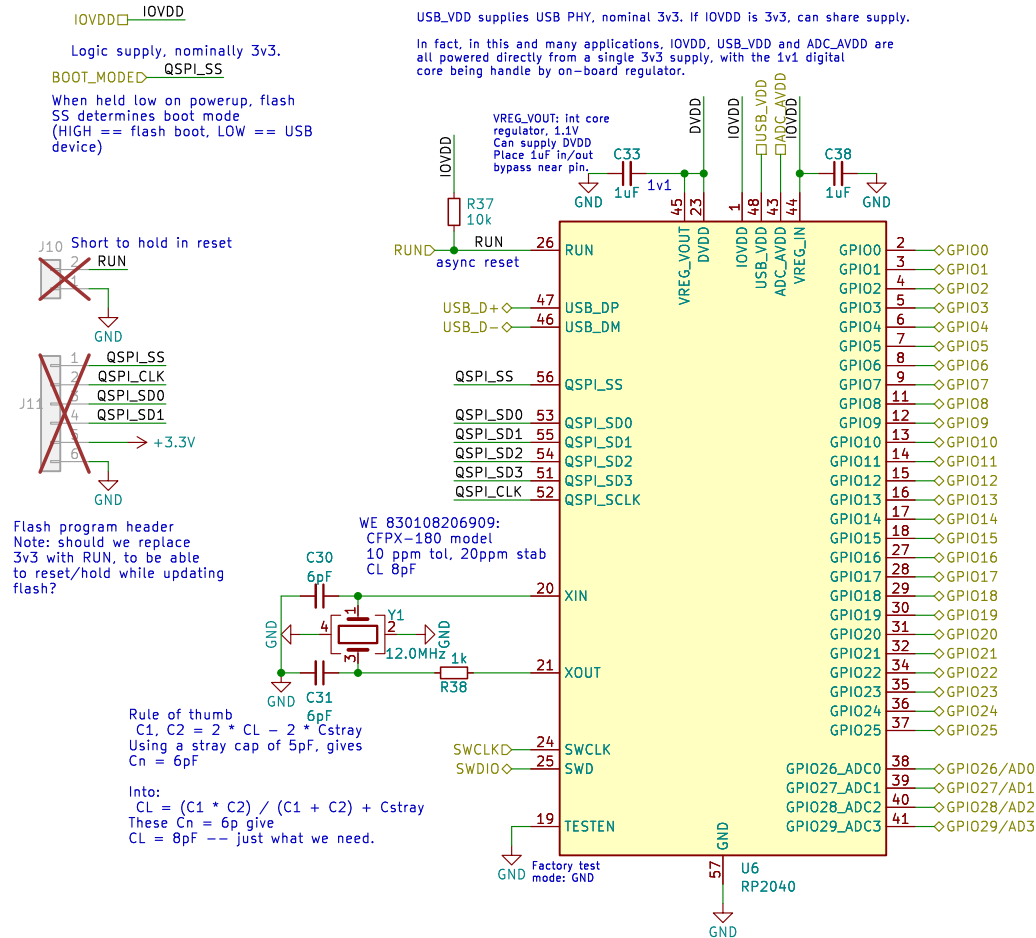
Std 4-pin 2.5x2.0mm osc

The oscillator is selected using the J5 jumper (short pins 1-2). To use an external clock, short pins 2-3 instead and feed ext_clk pin on J11.

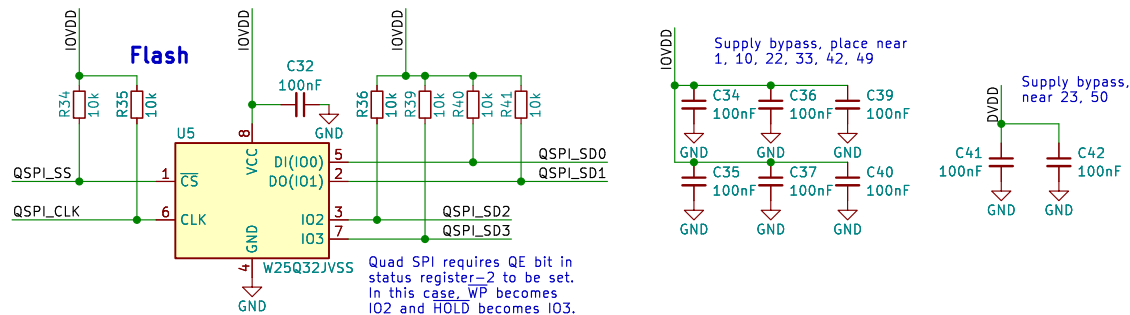
NOTE: This is the "caravel" clock.

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RP2040 Basic Support



	Function								
GPIO	F1	F2	F3	F4	F5	F6	F7	F8	F9
0	SPI0 RX	UART0 TX	I2C0 SDA	PWM0 A	SIO	PI00	PI01		USB OVCUR DET
1	SPI0 CSn	UART0 RX	I2C0 SCL	PWM0 B	SIO	PI00	PI01		USB VBUS DET
2	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PI00	PI01		USB VBUS EN
3	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PI00	PI01		USB OVCUR DET
4	SPI0 RX	UART1 TX	I2C0 SDA	PWM2 A	SIO	PI00	PI01		USB VBUS DET
5	SPI0 CSn	UART1 RX	I2C0 SCL	PWM2 B	SIO	PI00	PI01		USB VBUS EN
6	SPI0 SCK	UART1 CTS	I2C1 SDA	PWM3 A	SIO	PI00	PI01		USB OVCUR DET
7	SPI0 TX	UART1 RTS	I2C1 SCL	PWM3 B	SIO	PI00	PI01		USB VBUS DET
8	SPI1 RX	UART1 TX	I2C0 SDA	PWM4 A	SIO	PI00	PI01		USB VBUS EN
9	SPI1 CSn	UART1 RX	I2C0 SCL	PWM4 B	SIO	PI00	PI01		USB OVCUR DET
10	SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PI00	PI01		USB VBUS DET
11	SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PI00	PI01		USB VBUS EN
12	SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PI00	PI01		USB OVCUR DET
13	SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PI00	PI01		USB VBUS DET
14	SPI1 SCK	UART0 CTS	I2C1 SDA	PWM7 A	SIO	PI00	PI01		USB VBUS EN
15	SPI1 TX	UART0 RTS	I2C1 SCL	PWM7 B	SIO	PI00	PI01		USB OVCUR DET
16	SPI0 RX	UART0 TX	I2C0 SDA	PWM0 A	SIO	PI00	PI01		USB VBUS DET
17	SPI0 CSn	UART0 RX	I2C0 SCL	PWM0 B	SIO	PI00	PI01		USB VBUS EN
18	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PI00	PI01		USB OVCUR DET
19	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PI00	PI01		USB VBUS DET
20	SPI0 RX	UART1 TX	I2C0 SDA	PWM2 A	SIO	PI00	PI01	CLOCK GPIN0	USB VBUS EN
21	SPI0 CSn	UART1 RX	I2C0 SCL	PWM2 B	SIO	PI00	PI01	CLOCK GPIN1	USB OVCUR DET
22	SPI0 SCK	UART1 CTS	I2C1 SDA	PWM3 A	SIO	PI00	PI01	CLOCK GPIN2	USB VBUS DET
23	SPI0 TX	UART1 RTS	I2C1 SCL	PWM3 B	SIO	PI00	PI01	CLOCK GPIN3	USB VBUS EN
24	SPI1 RX	UART1 TX	I2C0 SDA	PWM4 A	SIO	PI00	PI01	CLOCK GPIN4	USB OVCUR DET
25	SPI1 CSn	UART1 RX	I2C0 SCL	PWM4 B	SIO	PI00	PI01	CLOCK GPIN5	USB VBUS DET
26	SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PI00	PI01		USB VBUS EN
27	SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PI00	PI01		USB OVCUR DET
28	SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PI00	PI01		USB VBUS DET
29	SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PI00	PI01		USB VBUS EN



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