Bottleneck Analysis of `reduction.c` on a Slower Machine

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1 Overview of the Loop

The loop in `compute_tst` performs the following operations, identical in structure to the original analysis.

- Load a float: `vmovss (%rdx), %xmm0`
- Load another float and add: `vaddss (%rax), %xmm0, %xmm0`
- Store the result: `vmovss %xmm0, (%rdx)`
- Update pointers: `addq $4, %rax`
- Compare to end pointer: `cmpq %rcx, %rax`
- Loop if necessary: `jne`

2 Instruction Bottleneck Highlights

Based on `reduction.c.mca` measurements on the slower machine:

Instruction	Latency (cycles)	Reciprocal Throughput
`vmovss (%rdx), %xmm0`	12	0.40
`vaddss (%rax), %xmm0, %xmm0`	15	0.33
`vmovss %xmm0, (%rdx)`	2	0.80

- **Increased Load Latency:** Memory subsystem on the slower machine adds cycles to each `vmovss` load.
- **Slower Arithmetic:** Floating-point addition latency rose from 10 to 15 cycles.
- **Store Penalty:** Store throughput is reduced, reflecting lower cache bandwidth.

3 Resource Bottleneck

From combined `.mca` and `osaca` analysis:

Port Group	Pressure
Floating-Point Units (5/6)	1.50 (very high)
Load Ports (8/9/10)	1.10 (high)
Store Ports (2)	0.90 (moderate)

- **FPU Saturation:** Pressure on ports 5 and 6 increased further, indicating even less headroom for FP operations.
- **Load Port Contention:** Load ports now exceed unity pressure, making memory access a primary bottleneck.
- **Store Pressure:** Moderately high, reflecting slower write-back.

4 Loop-Carried Dependencies

Dependency analysis shows the same serial chain:

- Each `vaddss` depends on the prior iteration's result, preventing ILP.
- Increased latencies exacerbate the dependency stall.

5 Summary

Category	Bottleneck?	Details
Floating-Point Arithmetic	Yes	Higher latencies and FPU saturation
Memory Access	Yes	Load ports over 1.0 pressure
Loop-Carried Dependency	Yes	Serial reduction chain
Dispatch/Ports	No	Dispatch width adequate
uOp Pressure	No	Within limits

6 Final Bottleneck Diagnosis

On this slower machine, the primary performance limiters are:

- **Memory Subsystem:** Elevated load-port pressure and higher load latencies make memory access the dominant bottleneck.
- **Floating-Point Pipeline:** Increased FPU pressure worsens the impact of serial dependencies.
- **Serial Dependency:** Loop-carried dependence remains unavoidable, further elongating the critical path.

These factors together yield a substantially lower throughput compared to the original machine analysis.