ECE 385

Fall 2020

Experiment 1

Introductory experiment

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Introduction:

In this lab, we learnt that even though the minimal SOP or POS can help designing a circuit, some undesirable features would happen in real world known as static hazard. Static hazard happens when there exists a lag when switching the input although the expected result would be the same. To solve this problem, we may combine all the min-terms in the K-map so that all circles on the K-map are interweaved with each other.

Circuit Operation:

In this lab, we designed 2 circuits to implement the 2-to-1 MUX. With 3 inputs ABC and an output Z, where B is used as a switch to choose between AC.

For Prelab A, output Z = B'C + BA, but when B switch input from A to C, even though the output is the same, there would be a static hazard due to an extra not gate.

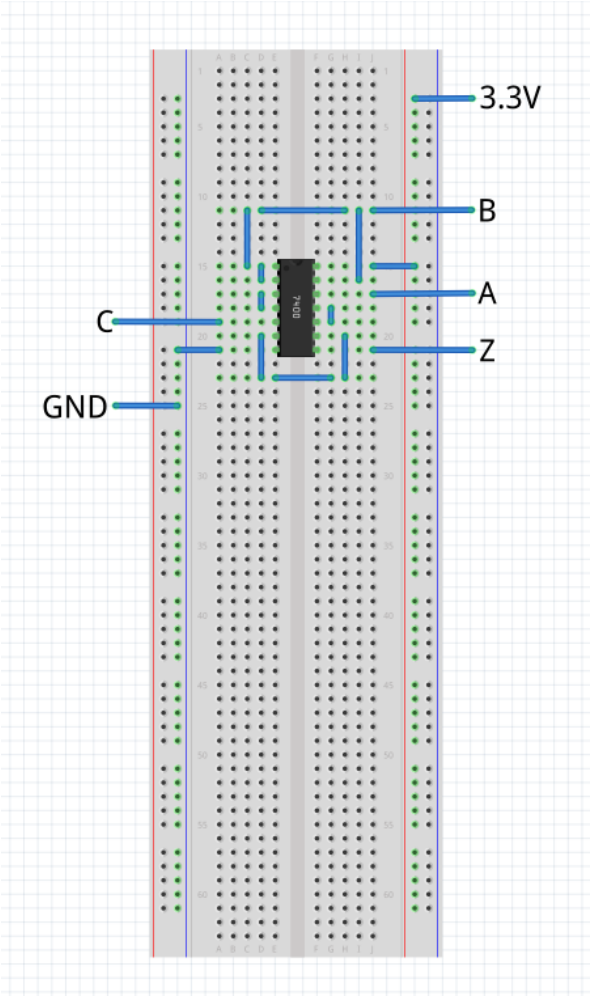
A\BC	00	01	11	10
0	0	1	0	0
1	0	1	1	1

For Prelab B, output Z = B'C + BA + AC, with this extra AC term, we are able to eliminate the static hazard, because the output from the extra term AC is always 0 which guarantees the output Z would not be changed.

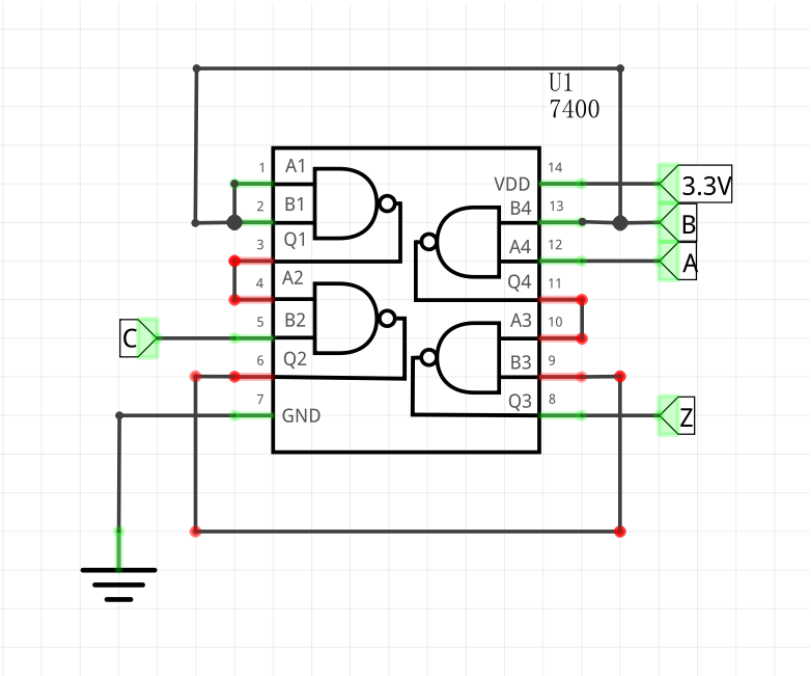
A\BC	00	01	11	10
0	0	1	0	0
1	0	1	1	1

Documentation:

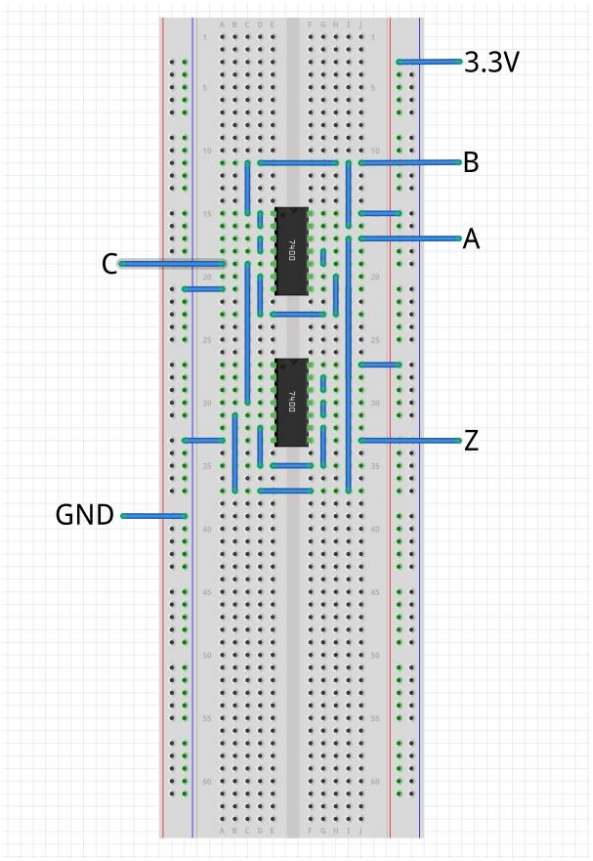
Prelab A Breadboard view:



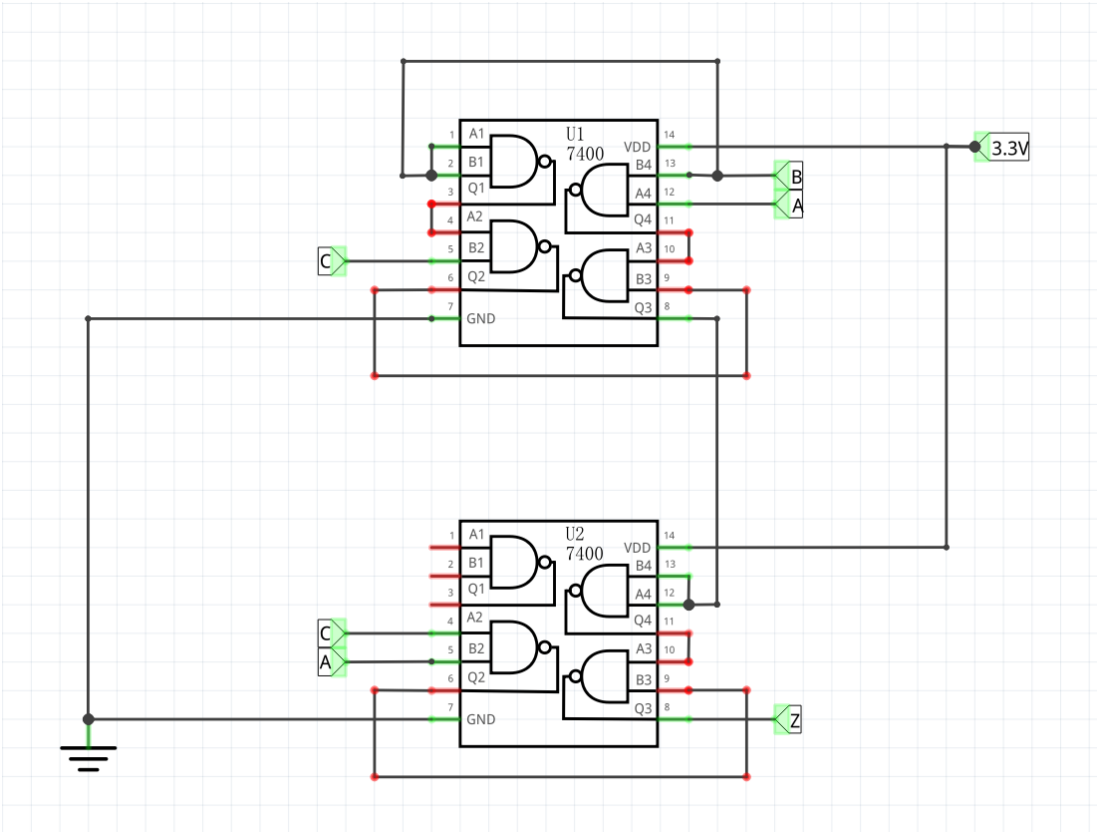
Prelab A Schematic View:



Prelab B Breadboard View:



Prelab B Schematic View:

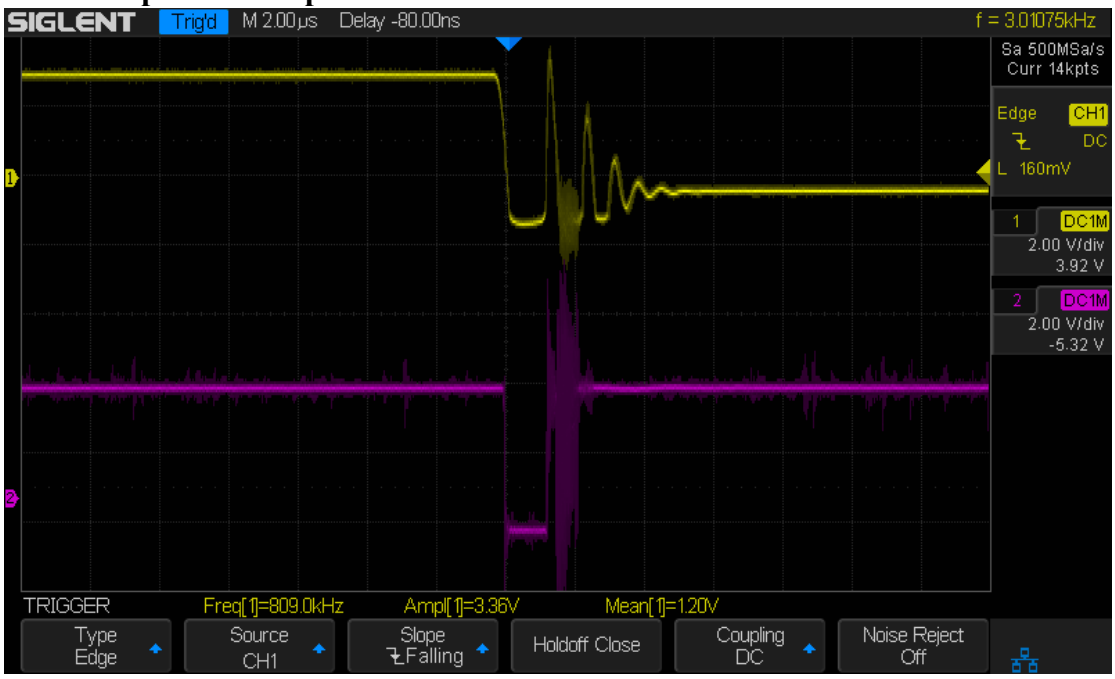


Truth Table for both Circuit A:

Z	A	B	C
0	0	0	0
1	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

If we set both inputs A and C to 1 and input B to be a 1 MHz and a 0 to 5-volt square wave, we will be able to observe the following outputs on the oscilloscope.The yellow line is the graph of input B. The purple line is the output Z.

Oscilloscope Printout part 2:



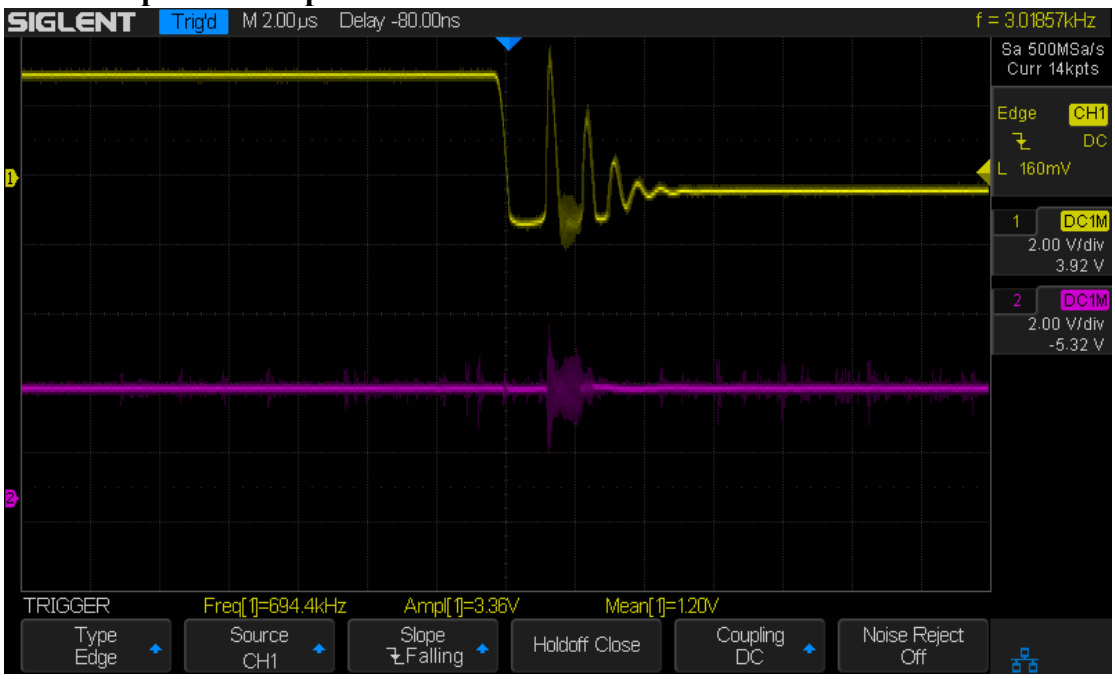
On the oscilloscope, we can see that there is a glitch on output Z when B is engaging with its falling edge. But it was too fast, therefore, a small capacitor can be added to make it salient.

Truth Table for both Circuit B:

Z	A	B	C
0	0	0	0
1	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

With a redundant term in the K-map was added, we can find that the glitch on output Z is diminished.

Oscilloscope Printout part 3:



Prelab Questions:

Not all groups may observe static hazards (why?)

Because the static hazard is so fast which is hard to be detected by LED.

If you do not observe a static hazard, chain an odd number of inverters together in place of the single inverter from Figure 16 or add a small capacitor to the output of the inverter until you observe a glitch. Why does the hazard appear when you do this?

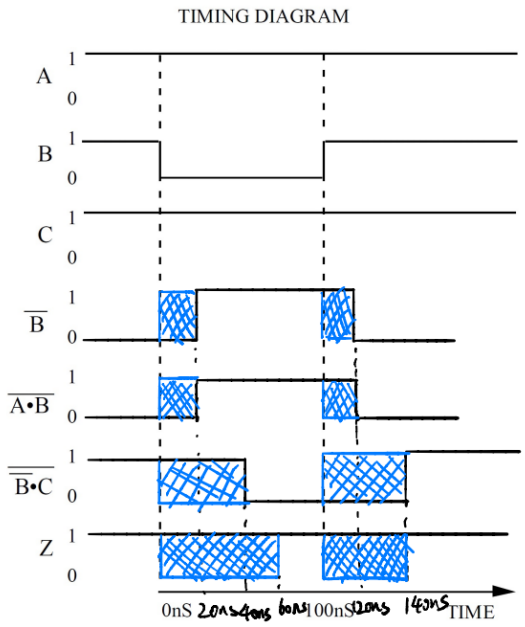
Because if the number of the inverters is odd, there must exist a path that has at least 1 more inverter than the other path which would make a lag between these two paths that is long enough for us to observe. Therefore, we are able to observe the glitch.

Lab Questions:

Does the output of part B of the pre-lab responds the same as part A? For the circuit of part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output, why?

Much of the output of Part B is the same as Part A except that it has no glitches since the logic is the same, only a redundant term is added.
We are more likely to observe a glitch at the falling edge of B since the output of (B'C)' gave the same result of the output from (AB)' due to the delay of the inverter so that the output Z would suddenly drop to 0 and back to 1.

Postlab Questions:



How long does it take the output Z to stabilize on the falling edge of B (in ns)? How long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.

It took 60ns for Z to stabilize on the falling edge and 40ns for Z to stabilize on the rising edge. The potential glitches will occur if the inputs are not determined due to the lag, so the Z may oscillate between 0 and 1. When B switches from A to C while AC are both 1, there is an extra 20ns delay on BC. During this delay (AB)' has changed into 1 while (B'C)' is still 1 due to the extra inverter, so Z turns out to be 0 for 20 ns even though the expected result is 1.

Explain how and why the debouncer circuit given in General Guide Figure 17 (GG.32) works. Specifically, what makes it behave like a switch and how the ill effect of mechanical contact bounces is eliminated?

C can choose between A and B to set different values on Q, which makes SPDT behave like a switch. An S-R latch is used to eliminate the contact bounce. When C is firstly connected A, D is sure to be 0 due to connection to the ground, Q would therefore be 1. Meanwhile, G is also 1 so QN is 0 which ensures that even if the switch bounces on A, Q will never change its value which is 1.

General Guide:

What is the advantage of a larger noise immunity? Why is the last inverter observed rather than simply the first? Given a graph of output voltage (VOUT) vs. input voltage (VIN) for an inverter, how would you calculate the noise immunity for the inverter?

A larger noise immunity can be used to sift noise so that we are able to get a much cleaner output. Noise can be accumulated so that more noise is persisted in the last inverter than the first inverter. To calculate the noise immunity, we steadily increase the input voltage to find a threshold which can be used to make the output change from low to high.

If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors?

When multiple LEDs are used, they are actually parallel connected to the resistor, making the resistance smaller and smaller. When much current goes through the resistor, the resistor cannot protect the circuit anymore.

Conclusion:

In this lab, we mainly focuses on the problem of static hazard which was caused by the delay of extra inverter. To solve this, we simply add a redundant term in the K-map. Then, we explored about contact bounce and noise immunity questions. No troubles were found during the lab since Professor Cheng did it instead of us.