ECE385
DIGITAL SYSTEMS LABORATORY
Instantiation Megafunctions (IP modules)

Megafunctions are what Intel calls their reconfigurable Intellectual Property (IP) modules. These modules are pre-designed FPGA components (such as interfaces, memory controllers, computation accelerators, etc.) which can be licensed from Intel or third parties and instantiated into an FPGA design. Typically, these can be configured graphically through a GUI, or through code via SystemVerilog parameters. For Experiment 6, you will configure an on-chip memory Megafunction for use as your main memory.

To start, open your existing Experiment 6 project that you've created. You can then expand the IP Catalog panel (by default located on the right side). Select RAM: 1-PORT and name your "IP Variant" as ***ram***.

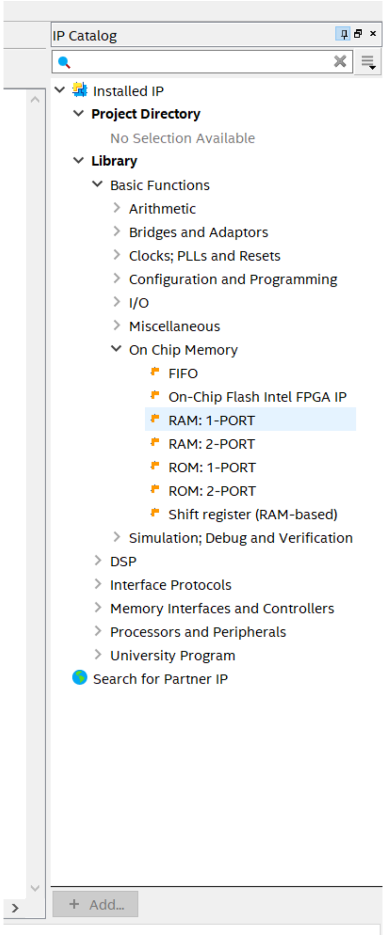
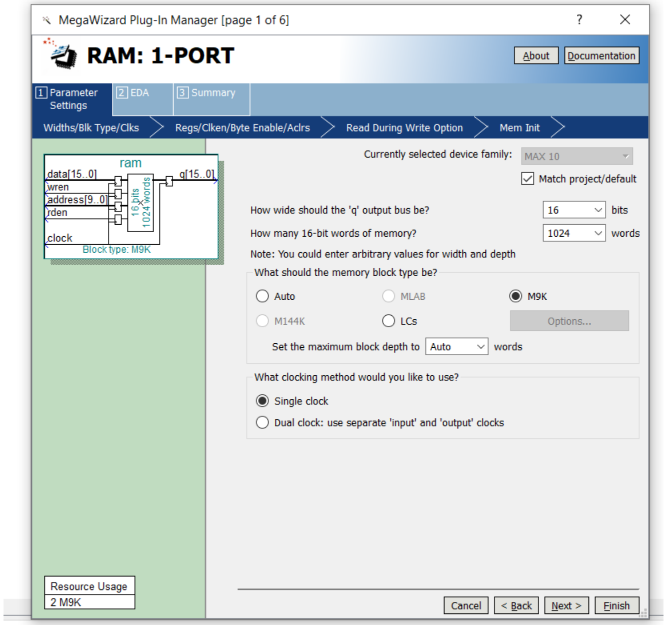


Figure 1 IP Catalog

IQT.2

You will then be presented with the following GUI tool. Populate the following according to the screenshots, and click Finish.



Currently selected device family: MAX 10

☑ Match project/default

How wide should the 'q' output bus be? 16 bits

How many 16-bit words of memory? 1024 words

Note: You could enter arbitrary values for width and depth

What should the memory block type be?

○ Auto ○ MLAB ● M9K

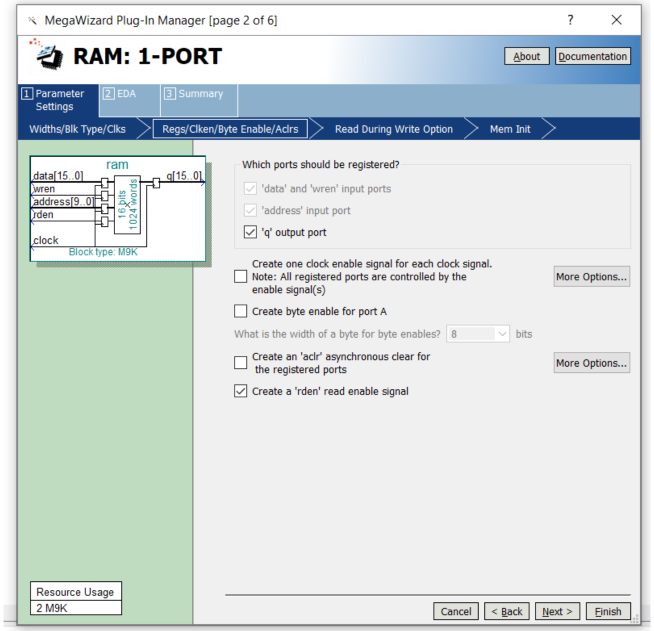
○ M144K ○ LCs Options...

Set the maximum block depth to Auto words

What clocking method would you like to use?

● Single clock

○ Dual clock: use separate 'input' and 'output' clocks



Which ports should be registered?

☑ 'data' and 'wren' input ports

☑ 'address' input port

☑ 'q' output port

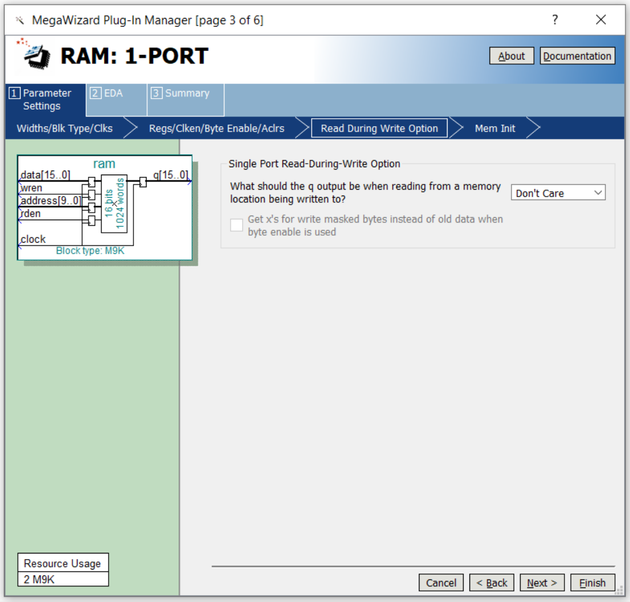
□ Create one clock enable signal for each clock signal. Note: All registered ports are controlled by the enable signal(s)

□ Create byte enable for port A

What is the width of a byte for byte enables? 8 bits

□ Create an 'aclr' asynchronous clear for the registered ports

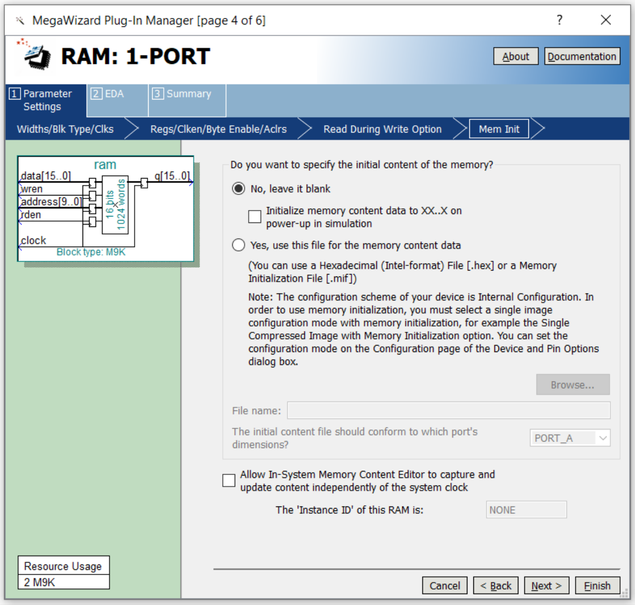
☑ Create a 'rden' read enable signal



Single Port Read-During-Write Option

What should the q output be when reading from a memory location being written to? Don't Care

□ Get x's for write masked bytes instead of old data when byte enable is used



Do you want to specify the initial content of the memory?

● No, leave it blank

□ Initialize memory content data to XX..X on power-up in simulation

○ Yes, use this file for the memory content data

(You can use a Hexadecimal (Intel-format) File [.hex] or a Memory Initialization File [.mif])

Note: The configuration scheme of your device is Internal Configuration. In order to use memory initialization, you must select a single image configuration mode with memory initialization, for example the Single Compressed Image with Memory Initialization option. You can set the configuration mode on the Configuration page of the Device and Pin Options dialog box.

File name:

The initial content file should conform to which port's dimensions? PORT_A

□ Allow In-System Memory Content Editor to capture and update content independently of the system clock

The 'Instance ID' of this RAM is: NONE

Although it is possible to populate the memory contents from the Megafunction GUI, we provide a module called instantiateram.sv which initializes the on-chip memory from the FPGA logic on reset. This is so the memory contents can be restored during a reset, rather than requiring a full FPGA reprogramming to restore.