ECE 385 Digital Systems Laboratory

Syllabus

The goal of ECE 385 course is to teach students design, build, and test/debug a digital system, which can be a 16-bit microprocessor, a dedicated logic core, or a system-on-a-chip (SoC) platform. Students will learn about the modular design approach, which is the underlining principle of IP-based SoC design methodology. Students will start with TTL logic in the first three weeks to strengthen their skills of using physical logic elements to build relatively complex circuits such as a 4-bit serial processor. Then, the course will make a transition to SystemVerilog and RTL design methodology. The concept of modular design is carried over to SystemVerilog so students would have a concrete understanding of the connection between wired circuits on the proto-board and mapped circuits on the FPGA board, and the RTL design abstraction can be better captured through this process. Students will then start to gradually learn how to design and realize digital circuits using SystemVerilog and the FPGA board. These labs would include 8-bit serial processor, arithmetic units, 16-bit SLC-3 processor, USB input and VGA display, and a simple SoC that connects a NIOS II embedded processor with a dedicated data-decryption hardware. Finally, students will have four weeks at the end of the semester to work on an open project of their own choice based on FPGA design with SystemVerilog. This open final project will be graded by creativity, complexity, and functionality of the design. At the conceptual level, students will learn combinational and sequential logic, storage elements, I/O and display, timing analysis, design tradeoffs, synchronous and asynchronous design methods, data-path and controller, microprocessor design, software/hardware co-design, and embedded systems.

Prerequisites: ECE 120, ECE 220 (or CS 225)

Credits: 3

Lecture meeting times and location: M/W 4:00-4:50pm; 1002 ECEB

Lab location: 4072 ECEB

Instructors: Prof. Zuofu Cheng

Office Hours: (posted on website)

Course website: http://courses.engr.illinois.edu/ece385

Grading policy:

- **9 Labs (195 points)**
- **Final Project (60 points)**
- **Two Midterm Exams – in-class multiple choice (30 points each – 60 points total)**
- **Peer Evaluation (5 points)**
- **Total – 320 Points**
- **Small section dependent curve (typically < 5 points)**
- **Standard grading scale (90 for A-, 80 for B-, etc) – may change in some semesters**

Course Materials:

- Lab manual (ECE 385 Lab Manual 18.1 – "Green Cover")
- Online materials on TTL and FPGA.
- On-line tutorial books on SystemVerilog.
- Reference books (ECE 120 textbook, others on reserve at Grainger)

Course Schedule:

Week	Lab to Demo	Notes
1	None – Lab session starts Tuesday. form groups in lab	No demo for lab 1, individual lab report, work on lab 2 demo **outside of class**
2	2 (TTL storage)	Groups must be formed to demo lab 2, work on lab 3
3	3 (Bit-serial processor)	Install Quartus and do Quartus and SystemVerilog Tutorial, work on lab 4
4	4 (Intro-SV - adders)	Demo on FPGA board, work on lab 5
5	5 (SV multiplier)	Work on lab 6 week 1
6	6 (Week 1 SLC-3 CPU)	Demo lab 6 week 1, **no extensions, lab 6.1 demo must be completed this week for credit, w**ork on lab 6 week 2
7	6 (Week 2 SLC-3 CPU)	Demo lab 6 week 2, **no demos for previous week's points**, first midterm in class, work on lab 7
8	7 (SoC with NIOS II)	Work on lab 8
9	8 (Drivers on NIOS II for USB host and VGA)	Work on lab 9 week 1
10	No lab	Spring Break
11	9 (Week 1 AES software encryption)	Demo lab 9 week 1, **no extensions, lab 9.1 demo must be completed this week for credit.** Work on lab 9 week 2 and final proposal
12	9 (Week 2 AES hardware decryption)	Demo lab 9 week 2, **no demos for previous week's points**, final project starts (final proposal due)
13	Optional checkpoint	Second midterm in class, work on final project
14	Required checkpoint	Work on final project
15	Optional checkpoint	Work on final project
16	Final project demos	Return kits after demo, turn in final report within 1 week