ARP Response Design

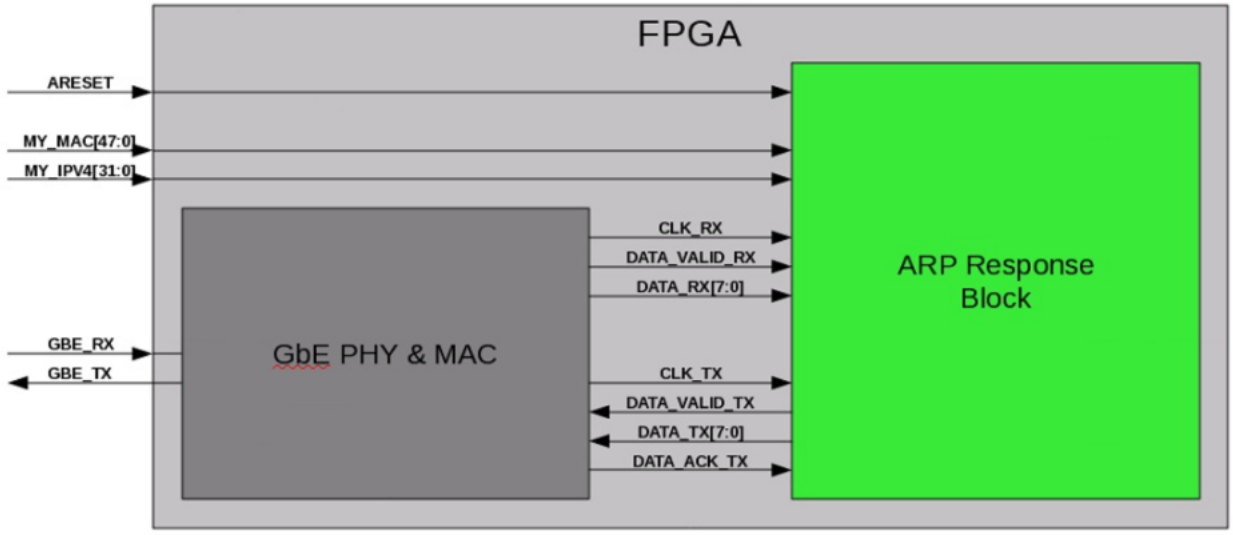
Overview

ARP (Address Resolution Protocol) is a mechanism that allows Layer 3 protocols (such as IPv4) to discover the Layer 2 address (such as Ethernet) of a device. For example:

> Computer A and B both have Ethernet connections and reside on the same LAN. They communicate to each other using IPv4. The IP address of computer A is 192.168.1.1 and the IP address of computer B is 192.168.1.2. If computer A has data for computer B, it needs to know computer B's Ethernet MAC to properly address the packet. Computer A will send out an ARP Request for 192.168.1.2. Computer B will respond with an ARP Response that contains Computer B's Ethernet MAC address.

Project

Design the ARP Response Block in either VHDL or Verilog. When an ARP Request matching the block's IPv4 address is received, an ARP Response should be generated.



Port Definitions

Port	Direction	Description
ARESET	Input	Active high, asynchronous reset signal.
MY_MAC[47:0]	Input	MAC Address for this Ethernet port. Signal value is static and does not change.
MY_IPV4[31:0]	Input	IPv4 Address for this Ethernet port. Signal value is static and does not change.
CLK_RX	Input	Used to clock DATA_VALID_RX and DATA_RX. This clock is a divided down version of the clock recovered from GBE_RX Frequency: 125MHz +/-300ppm
DATA_VALID_RX	Input	Valid Ethernet Frame data. This signal goes high when a valid Ethernet Frame has been received. It remains high for the entire length of the received Ethernet Frame (excluding the Preamble, Start of Frame, and FCS bytes).

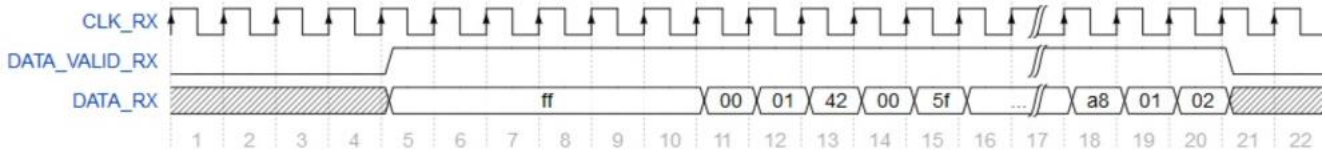
DATA_RX[7:0]	Input	Received Ethernet Frame data (excluding the Preamble, Start of Frame, and FCS bytes). Only valid when DATA_VALID_RX is high.
CLK_TX	Input	Used to clock DATA_VALID_TX, DATA_TX, and DATA_ACK_TX. This clock is derived from an on-board oscillator. Frequency: 125MHz +/-100ppm
DATA_VALID_TX	Output	Valid Ethernet Frame data. This signal goes high with the first byte of the Ethernet Frame to transmit. The MAC will respond with DATA_ACK_TX when it is ready for the remaining bytes.
DATA_TX[7:0]	Output	Transmit Ethernet Frame data. The data must be valid when DATA_VALID_TX is high.
DATA_ACK_TX	Input	Acknowledgement from the Ethernet MAC that it is ready to receive the rest of the Ethernet Frame. This signal only goes active for one clock cycle.

Timing Diagrams

Below is the timing diagram for receiving an ARP Request.

ARP Request

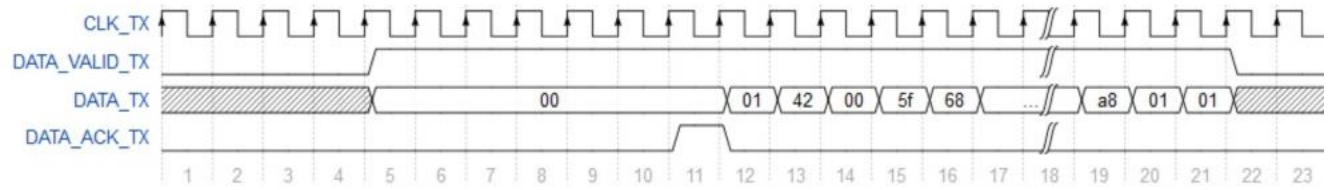
0x00:	ff	ff	ff	ff	ff	ff	00	01	42	00	5f	68	08	06	00	01
0x10:	08	00	06	04	00	01	00	01	42	00	5f	68	c0	a8	01	01
0x20:	00	00	00	00	00	00	c0	a8	01	02						



Below is the timing diagram for transmitting an ARP Response. Notice that DATA_TX is equal to the first byte of the Ethernet Frame until DATA_ACK_TX goes high.

ARP Response

0x00:	00	01	42	00	5f	68	00	02	23	01	02	03	08	06	00	01
0x10:	08	00	06	04	00	02	00	02	23	01	02	03	c0	a8	01	02
0x20:	00	01	42	00	5f	68	c0	a8	01	01						



For additional information about the MAC interface, see Xilinx User Guide 368. The MAC interface described in the Xilinx User Guide is very similar to the MAC interface in this project.

Tools

Free editions of Xilinx ISE and Altera Quartus II are readily available online for both Windows and Linux. Altera also offers a free edition of ModelSim for both Windows and Linux.

If you are using an Apple Mac and do not have access to a Windows or Linux machine, you can download VirtualBox and install Ubuntu 10.4.