Richard Dennis

Hardware Engineer

Boise, ID - Email me on Indeed: indeed.com/r/Richard-Dennis/1d20ade7d97eb567

Development of innovative technologies in a team-oriented environment with an emphasis on hardware design.

WORK EXPERIENCE

Hardware Engineer

Hewlett-Packard - Boise, ID - January 2007 to Present

Work closely with system architects in definition and design phase. Apply knowledge of PCB layout using high speed digital design rules as it pertains to such protocols as USB, PCIe, and LVDS. Duties include schematic design and capture, guiding electromagnetic compatibility debugging, functional verification, signal characterization, and environmental stress testing.

Teaching Assistant

University of Virginia - Integrated Circuit Fabrication Laboratory - Charlottesville, VA - January 2005 to May 2005

Developed weekly design problems for students to train them in the usage of the fabrication process simulator, ATHENA. Design problems were assigned to strengthen students' understanding of IC fabrication being conducted in UVA's on-site clean room.

Research Assistant

MIT Media Lab - Interactive Cinema Group - Cambridge, MA - June 2004 to August 2004

Worked on TViews project, which uses acoustic and infrared sensors to identify and locate multiple objects on a dynamic, 2-D human interface. Co-designed circuitry used to triangulate position of aforementioned objects. Manufactured objects using programmable machines such as a waterjet and lasercutter.

HTML Instructor

NASA RISE - Cambridge, MA - June 2003 to August 2003

Developed course content and instructed undergraduate students in design of web pages utilizing HTML code as well as novel web design programs and techniques.

Intern

Ford Motor Company - Dearborn, MI - June 2001 to August 2001

Participated in product development of an electrical actuation system for relays to control the flow of oil in an engine controlled environment for a confidential Ford Motor Company research project.

EDUCATION

Master of Science in Electrical Engineering

University of Virginia - Charlottesville, VA
August 2006

Bachelor of Science in Electrical Engineering and Computer Science

Massachusetts Institute of Technology - Cambridge, MA
June 2004

SKILLS

* Software: Cadence Design System, LabView, Mathcad, MatLab, Mentor Graphics, Microsoft Excel, Microsoft Word, Pspice, UNIX * Personal: Public speaking, formal technical writing, extensive analog and mixed-signal circuit design experience, machine shop experience

ADDITIONAL INFORMATION

Relevant Courses:

* Advanced VLSI Design, Nanoelectronic Devices, VLSI Design, Solid State Devices, Integrated Circuit Fabrication Laboratory, Statistics for Engineers and Scientists, Physics of Semiconductors, Microelectronic Integrated Circuit Fabrication
* Solid-State Circuits, Computer Systems Engineering, Bioelectronics Laboratory, Microelectronic Circuits and Devices, Analog Electronics Laboratory, Artificial Intelligence, Electromagnetics and Applications, Computation Structures, Signals and Systems, Circuits and Electronics, Probabilistic Systems Analysis, Structure and Interpretation of Computer Programs, Introduction to Computers and Engineering Problem Solving, Electricity and Magnetism, Differential Equations, Multi-variable Calculus, Managerial Psychology

Thesis:

* Utilization of CMOS Process Variations in the 0.25µm TSMC Process for Unique RFID Bit Encoding

Proposal:

* A method that uses the inherent variations between transistors combined with auxiliary digital signal processing circuitry to create unique, yet random, identifying strings that are to be incorporated into current Radio Frequency Identification (RFID) technology. The system generates a string of bits that is representative of the direction of mismatch between two control transistors. The mismatch between the transistors is modeled using the Monte Carlo tool within the Cadence Design Systems* package that randomly changes the threshold voltage parameter for each transistor for each iteration. The digital signal processing circuitry is responsible for testing each bit for its robustness in the presence of a controlled imbalance.