AKHIL MULPURI

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Academics

Master of Science in **Electrical and Computer Engineering** **August 2015 - Present**
University of Illinois at Chicago GPA - 3.38/4.0
Expected Graduation - **May 2017**

Bachelor of Technology in **Electrical and Electronics Engineering** **June 2011 – June 2015**
Gandhi Institute of Technology & Management University, Hyderabad, India GPA - 3.7/4.0

Relevant course work

Introduction to VLSI Design, Advanced Computer Architecture, Advanced VLSI Design, Advanced Microprocessor Architecture and Design, Computer Systems Design, Advanced Computer Communication Networks.

Technical Proficiency

Hardware Description and Programming Languages: **C, C++, Python, Verilog.**
EDA Simulation Tools: **Cadence virtuoso, Xilinx ISE.**
Misc. software's: **MS-Office, PSIM, AutoCAD.**
Operating Systems: **Windows, UNIX, MAC OS.**

Academic Projects

Design and layout for a 4 bit synchronous ALU (Arithmetic Logic Unit) using 250nm SOI technology
Validated the design with LVS and physical DRC verification. Performed power, delay calculations, static timing analysis. Good knowledge on EDA flow and RTL. **Tool: Cadence**

Design and layout for a negative edge-triggered register in master slave D flip-flop configuration in the standard 0.25 micron CMOS technology.
Designed and used static CMOS type inverters, latches of dynamic type, NMOS-only pass transistors are used as switches**.** Performed LVS, DRC verification, power, delay calculations, and static timing analysis. Simulated the circuit with parasitics and without parasitics. **Tool: Cadence**

Analyze the performance impact of varying architectural parameters using the architectural simulator SimpleScalar.
Ran a SPEC2000 benchmark program, equake, in sim-outorder and inorder execution modes and the performance related statistics such as CPI, IPC, elapsed time and miss rates were obtained. Varied the sizes of L1 instruction cache, data cache and observed the changes on cache miss rates and performance. Used these performance statistics and found out the optimal configuration. **Tools: VMware, SimpleScalar**

Implementation of a 16x16 bit serial multiplier.
Designed D Flip flops and used them to construct a serial multiplier. Designed in Xilinx ISE using Verilog, performed functional simulation and timing analysis. **Tools: Xilinx ISE, Verilog**