SX-Key Manual v1.1 Addendum Rev 3:

Description

The following is an addendum to the SX-Key/Blitz Development System Manual version 1.1. All page numbers refer to the SX-Key/Blitz Development System Manual version 1.1. **The items included in this addendum concern the use of the sxkey.exe software version 1.30.**

Explanation of Contents

This addendum is broken into the following sections:

1. General Information. **(should be read by everybody, regardless of which SX chip you are using)**
2. For those familiar with the SX18/28. **(should be read by those using 18 and 28-pin chips)**
3. For those familiar with the SX48/52. **(should be read by those using 48 and 52-pin chips)**

General Information (for users of any SX chip):

Software

The SX-Key Editor software version 1.30 is the first version to have integrated support for the SX18/28/48 and 52 chips. Previously, a different editor version was available for the 18/28 and 48/52 parts. This software supports the production versions of the SX18/28 and SX48/52 chips. Production versions of the SX18/28 chips have a date code that starts with the letter "A". Production versions of SX48 and SX52 chips have a date code of AA0004AA or greater. Previous date codes of the SX chips will not be supported by future software or documentation. It is recommended that Engineering Samples of SX chips be discarded.

The software is available for free download from the "Downloads" section of the Parallax, Inc. web site: http://www.parallaxinc.com (if it wasn't included on the Parallax CD you received).

The last paragraph on page 17 should read:

1. Run the SX-Key Editor software from the directory it was installed into in the procedure above. The software is called sxkey.exe.

The software supports a new command-line option for selecting the default com port to use. For example, using the following line in the Target: field of a shortcut to your SX-Key software:

```
C:\SXKey\SXKey.exe  /2
```

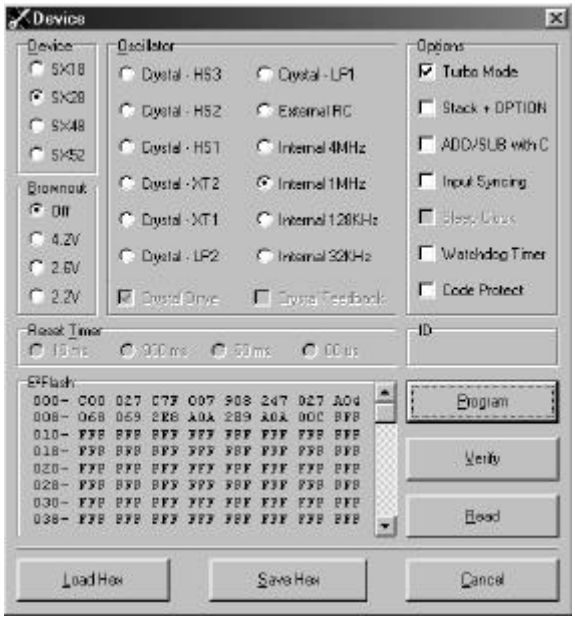
Would start the editor (assuming it is stored in the C:\SXKey directory) and tell it to use COM 2 for communicating with the SX-Key. Only com ports 1, 2, 3 and 4 are supported.

Development Board For SX48 and SX52

Unlike the SX18 and SX28, the SX48 and SX52 chips are only available in TQFP and PQFP package styles. Due to the nature of the package styles and the price of sockets to handle them, a development board with a socket for the SX48/52 chips is impractical. To make development easier, Parallax, Inc. has chosen to make a small module with the SX52 soldered to it. This board, called the 52con Carne, is designed to fit nicely into a standard breadboard and has connections for the SX-Key/Blitz, resonators, crystals, etc. Please refer to the 52con Carne Manual for complete information.

Device Window and Device Settings

The Device Windows shown on page 33 and 34 (Figures 5.5 and 5.6) has been modified and is shown below.



Disregard mention of the SXKey28L.exe and SXKey52.exe in the last paragraph on page 33.

The first paragraph on page 34 should read:

The Oscillator, Options and Brownout sections specify the configuration of the SX fuses for options like turbo mode, code protect, oscillator type and brown-out reset detection. Oscillator options "Crystal – HS3" through "Crystal – RC" specify external clock sources and "Internal 4MHz" through "Internal 32KHz" specifies the internal clock source. The "Crystal Drive" and "Crystal Feedback" options are available when using external clock sources only. SX18/28 only supports the Crystal Feedback setting. Crystal Drive enables or disables the OSC2 drive output. Crystal Feedback enables or disables the internal feedback resister between OSC1 and OSC2 pins. When using a clock-oscillator pack (connected only to OSC1) the Drive and Feedback may be disabled to conserve energy. All options are described in the table below.

The Oscillator items specify oscillator drive (gain) settings for external oscillators or for the internal oscillator. The table below indicates the setting to use on the DEVICE line in source code to select the appropriate Oscillator item. This table replaces Tables 5.4 and 5.5 on page 35.

Oscillator Item	DEVICE-Line Setting	When To Use
Crystal – HS3 Crystal – HS2 Crystal – HS1 Crystal – XT2 Crystal – XT1 Crystal – LP2 Crystal – LP1	OSCHS3 OSCHS2 OSCHS1 OSCXT2 OSCXT1 OSCLP2 OSCLP1	Specifies oscillator drive capacity. Crystal-HS3 (OSCHS3) drives the crystal/resonator very hard; used for high frequencies. Crystal-LP1 (OSCLP1) drives the crystal/resonator very lightly; used for low frequencies.
Crystal – Drive Crystal – Feedback	DRIVEOFF FEEDBACKOFF	These items are normally on. Disable them with the device setting to save power when using a clock/oscillator pack connected only to OSC1. Crystal-Drive specifies OSC2 drive and Crystal-Feedback specifies oscillator feedback resister. Use these in addition to "gain" settings, above.
External RC	OSCRC	Specifies special drive for resister-capacitor clock circuits.
Internal 4 MHz	OSC4MHZ	For internal 4 MHz oscillator.
Internal 1 MHz	OSC1MHZ	For internal 1 MHz oscillator.
Internal 128 KHz	OSC128KHZ	For internal 128 KHz oscillator.
Internal 32 KHz	OSC32KHZ	For internal 32 KHz oscillator.

The Brownout section of the Device window specifies the approximate voltage level at which the SX will enter a brownout condition. This setting is normally off. Use one of the settings below to enable it.

Brownout Item	DEVICE-Line Setting	When To Use
4.2V	BOR42	Use this when a brownout at approximately 4.2 volts is desired.
2.6V	BOR26	Use this when a brownout at approximately 2.6 volts is desired.
2.2V	BOR22	Use this when a brownout at approximately 2.2 volts is desired.

The following table replaces the Device Directive Settings, Table 6.2, on page 43.

Setting	Description	Default
SX18 SX28 SX48 SX52	Specifies the device type, 18, 28, 48 or 52-pin	SX18
OSCHS3 OSCHS2 OSCHS1 OSCXT2 OSCXT1 OSCLP2 OSCLP1 OSCRC OSC4MHZ OSC1MHZ OSC128KHZ OSC32KHZ	External crystal/resonator – drive level 7 (for 20 to 50+ MHz) External crystal/resonator – drive level 6 (for 16 to 50+ MHz) External crystal/resonator – drive level 5 (for 8 to 50 MHz) External crystal/resonator – drive level 4 (for 1 to 24 MHz) External crystal/resonator – drive level 3 (for 32 KHz to 10 MHz) External crystal/resonator – drive level 2 (for 32 KHz to 1 MHz) External crystal/resonator – drive level 1 (for 32 KHz) External RC circuit Internal oscillator set to 4 MHz Internal oscillator set to 1 MHz Internal oscillator set to 128 KHz Internal oscillator set to 32 KHz	OSCHS3
DRIVEOFF FEEDBACKOFF	Used in combination with OSCLP1 – OSCHS3 and clock/oscillator packs to disable OSC2 drive and feedback resisters, respectively.	Drive and Feedback are on
DRT18MS DRT960MS DRT60MS DRT60US	Device reset timer waits 18 ms after MCLR rises (SX48/52 only) Device reset timer waits 960 ms after MCLR rises (SX48/52 only) Device reset timer waits 60 ms after MCLR rises (SX48/52 only) Device reset timer waits 60 us after MCLR rises (SX48/52 only)	DRT18MS
BOR42 BOR26 BOR22	Brownout to trigger at < 4.2 volts Brownout to trigger at < 2.6 volts Brownout to trigger at < 2.2 volts	no brownout
TURBO	Specifies turbo mode (1:1 execution) (SX18/28 only; 48/52 are always in turbo mode).	compatible mode (1:4 execution)
STACKX_OPTIONX	Stack is extended to 8 levels and Option register is extended to 8 bits. (SX18/28 only; 48/52 always have this set).	2 levels/6 bits
CARRYX	ADD and SUB instructions use Carry flag as input*	Carry flag ignored
SYNC	Input Syncing enabled	Input Syncing disabled
WATCHDOG	Watchdog Timer enabled	Watchdog disabled
PROTECT	Code Protect enabled	Code Protect disabled
SLEEPCLOCK	Clock is enabled during sleep, to allow faster recovery (SX48/52 only)	No clock during sleep

* Many instructions are adversely affected by the carry flag when CARRYX is specified. See Appendix B for more information.

For Those Familiar with the SX18 and SX28 (and the old v1.09 software):

Please use the v1.30 software and review the changes mentioned in the "General Information" section above.

Tips for using old source code in the v1.30 SX-Key Editor software:

1. When using a clock/oscillator pack (or similar device connected only to the OSC1 pin), the oscillator gain still must be set for the appropriate frequency, but the Feedback resister is not needed. For example, if using a clock/oscillator pack of 10 MHz, the DEVICE line below may be most appropriate:

   DEVICE SX28, OSCHS1, FEEDBACKOFF

This would set the SX28 chip's oscillator gain (OSCHS1) for a range of approximately 8 to 50 MHz and disable the internal feedback resister between OSC1 and OSC2 (FEEDBACKOFF).

The SX-Key Editor software version 1.30 now supports the additional pre-defined equates, shown below (for the SX18 and SX28):

```
CMP   -or- COMPARATOR       =   $08     ;Comparator register
WKPEN -or- WAKE_PENDING     =   $09     ;Wake-up Pending register
WKED  -or- WAKE_EDGE        =   $0A     ;Wake-up Edge register
WKEN  -or- WAKE_ENABLE      =   $0B     ;Wake-up Enable register
ST    -or- SCHMITT          =   $0C     ;Schmitt-Trigger register
LVL   -or- LEVEL            =   $0D     ;Logic Level register
PLP   -or- PULL_UP          =   $0E     ;Pull-up resister register
TRIS  -or- DIRECTION        =   $0F     ;Tristate (direction) register
```

See the sxkey.txt file for a list of all equates, directives, device settings and commands.

For Those Familiar with the SX48 and SX52 (and the old v1.20 software):

Please use the v1.30 software and review the changes mentioned in the "General Information" section above. The software and production-level SX48/52 chips now support nearly the same device settings (oscillator, brownout, etc) as for the SX18/28.

1. Oscillator settings are identical to the SX18/28: (OSCLP1 – OSCHS3).
2. New Crystal-Drive and Crystal-Feedback control allows better low-power settings when using external clock/oscillator packs (connected only to OSC1).
3. Brownout now has identical settings as with the SX18/28: (BOR22 – BOR42).
4. New "device name" settings (SX48 and SX52) are required for source code. Ie: DEVICE SX48, OSCHS2

Tips for using old source code in the v1.30 SX-Key Editor software:

1. Device name must now be specified in the DEVICE line. For example, if your DEVICE line looks like:

   DEVICE OSC4MHz, PROTECT

   It must now be changed to (assuming you're using an SX52):

   DEVICE SX52, OSC4MHz, PROTECT

2. When using a clock/oscillator pack (or similar device connected only to the OSC1 pin), the oscillator gain still must be set for the appropriate frequency, but the OSC2 Drive output and Feedback resister are not necessarily needed. Disabling the Drive and Feedback will help ensure better low-power consumption. For example, if using a clock/oscillator pack of 10 MHz, the DEVICE line below may be most appropriate:

   DEVICE SX52, OSCHS1, DRIVEOFF, FEEDBACKOFF

This would set the SX52 chip's oscillator gain (OSCHS1) for a range of approximately 8 to 50 MHz and turn off the drive on OSC2 (DRIVEOFF) and disable the internal feedback resister between OSC1 and OSC2 (FEEDBACKOFF).

The Reset section of the Device window (shown in the "General Information" section, above, specifies the approximate time the SX48/52 chip should wait from deassertion of the MCLR pin to start running again.

Reset Item	DEVICE-Line Setting	When To Use
18ms	DRT18MS	A reset delay of 18 ms is desired.
960ms	DRT960MS	A reset delay of 960 ms is desired.
60ms	DRT60MS	A reset delay of 60 ms is desired.
60us	DRT60US	A reset delay of 60 us is desired.

Figure 5.8 on page 36 should be removed; the Configure window for the SX48/52 is now exactly the same as for the SX18/28. In addition, ignore the three paragraphs on page 36 and 37 that discuss the Device Erasure, Code/Fuse Program and Adaptive sections.

The SX-Key Editor software version 1.30 now supports the additional pre-defined equates, shown below (for the SX48 and SX52):

```
TIMER_CAPTURE_LOW       =   $00     ;Low Timer Capture register
TIMER_CAPTURE_HIGH      =   $01     ;High Timer Capture register
TIMER_COMPARE2_LOW      =   $02     ;Low Timer Compare register 2
TIMER_COMPARE2_HIGH     =   $03     ;High Timer Compare register 2
TIMER_COMPARE1_LOW      =   $04     ;Low Timer Compare register 1
TIMER_COMPARE1_HIGH     =   $05     ;High Timer Compare register 1
TIMER_CONTROL_B         =   $06     ;Timer Control register B
TIMER_CONTROL_A         =   $07     ;Timer Control register A
CMP   -or- COMPARATOR   =   $08     ;Comparator register
WKPEN -or- WAKE_PENDING =   $09     ;Wake-up Pending register
WKED  -or- WAKE_EDGE    =   $0A     ;Wake-up Edge register
WKEN  -or- WAKE_ENABLE  =   $0B     ;Wake-up Enable register
ST    -or- SCHMITT      =   $0C     ;Schmitt-Trigger register
LVL   -or- LEVEL        =   $0D     ;Logic Level register
PLP   -or- PULL_UP      =   $0E     ;Pull-up resister register
TRIS  -or- DIRECTION    =   $0F     ;Tristate (direction) register

RD                      =   $08     ;RD i/o register
RE                      =   $09     ;RE i/o register
```

See the sxkey.txt file for a list of all equates, directives, device settings and commands.

Architecture Considerations

The Banking structure on the SX48/52 chips is different than it was in the engineering sample units. The BANK instruction on the Engineering Samples would change between either the odd banks or the even banks, depending on the current bank. The BANK instruction on the Production units effectively changes banks within 0 though 7 or 8 though 15, depending on which block of banks the SX is currently in. Only 3 of the 4 bits governing the currently selected bank are actually affected by the BANK instruction on the SX48/52. For example, if the current bank is 0, the BANK 7 instruction will switch to bank 7. Additionally, a BANK 15 instruction will also switch to bank 7. If, however, the current bank is 8, the BANK 7 instruction will switch to bank 15. Additionally, a BANK 15 instruction will also switch to bank 15.

To switch to a different block of banks, you will need to set or clear bit 7 of the FSR register. For example, the following code will switch to bank 7 within the upper block of banks (effectively bank 15).

```
Setb FSR.7
Bank 7

-- or --

Setb FSR.7
Bank 15
```

The Mode register is 5 bits wide on the SX48/52 (as opposed to 4 bits on the SX18/28). The MODE instruction, however, can only affect the lower 4 bits of the mode register. It is suggested that two instructions be used to properly set all bits of the mode register. For example, the following code will set the mode register to $1F:

```
Mov     W,#$1F
Mov     M,W
```

NOTE: Depending on the rise-time of the MCLR pin in relation to the rise-time of the Vdd pin upon a power-up condition, the Mode register may become corrupt during debug operations. It is always recommended that the above two lines of code be executed (to set Mode to the default, or desired, state) before using ANY instructions that rely on the state of Mode.

There may be many modifications/enhancements to the SX architecture of the 48/52 that you are not aware of, especially if you normally use the 18/28-pin chips. It is recommended that you download the latest datasheet for the 48/52-pin SX chips from the Ubicom website (http://www.ubicom.com/) and review it carefully to avoid problems associated with architectural differences.