

# SN74F161A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS056B – MARCH 1987 – REVISED AUGUST 2001

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for N-Bit Cascading
- Fully Synchronous Operation for Counting

## description

This synchronous, presettable, 4-bit binary counter has internal carry look-ahead circuitry for use in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. However, counting spikes can occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of CLK.

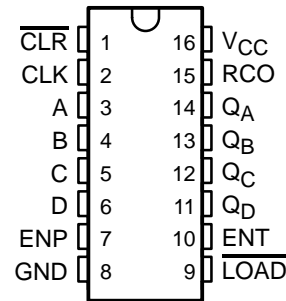
This counter is fully programmable. That is, it can be preset to any number between 0 and 15. Because presetting is synchronous, a low logic level at the load ( $\overline{LOAD}$ ) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of ENP and ENT.

The clear function is asynchronous, and a low logic level at the clear ( $\overline{CLR}$ ) input sets all four of the flip-flop outputs to low, regardless of the levels of CLK,  $\overline{LOAD}$ , ENP, and ENT.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications, without additional gating. This function is implemented by the ENP and ENT inputs and an RCO output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-logic-level pulse while the count is 15 (HHHH). The high-logic-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The SN74F161A features a fully independent clock circuit. Changes at ENP, ENT, or  $\overline{LOAD}$  that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.

D, DB, OR N PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F161AN	SN74F161AN
	SOIC – D	Tube	SN74F161AD	F161A
		Tape and reel	SN74F161ADR	
	SSOP – DB	Tape and reel	SN74F161ADB	F161A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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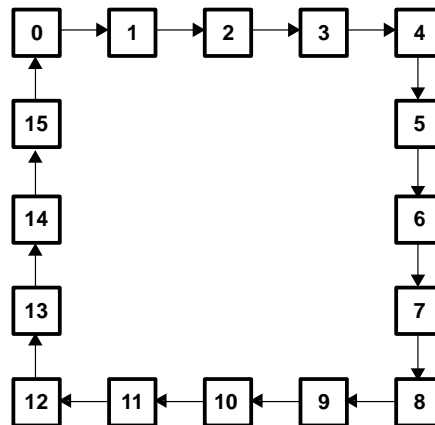
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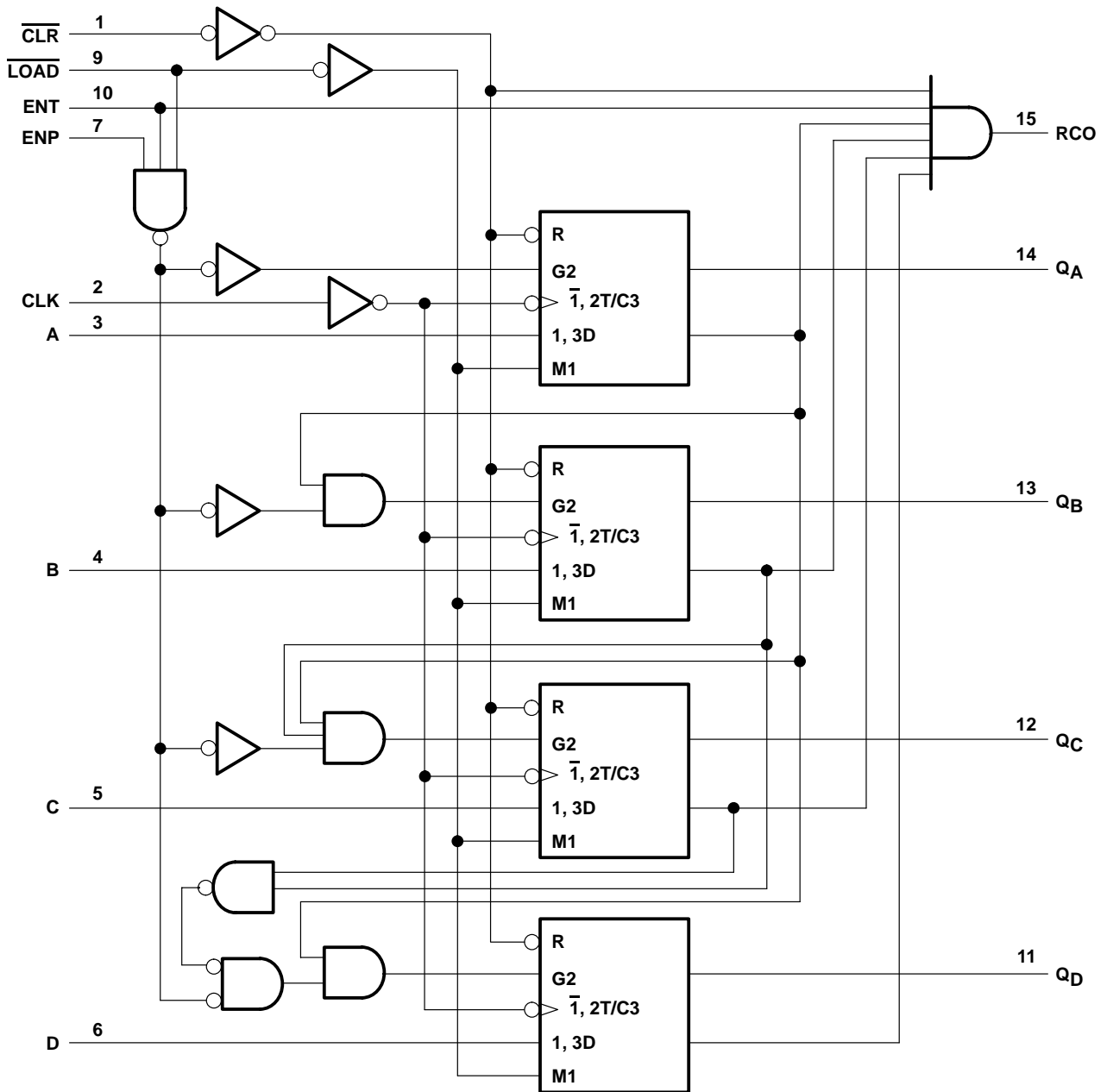
### state diagram



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## logic diagram (positive logic)

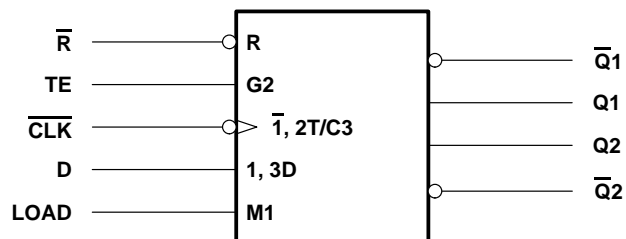


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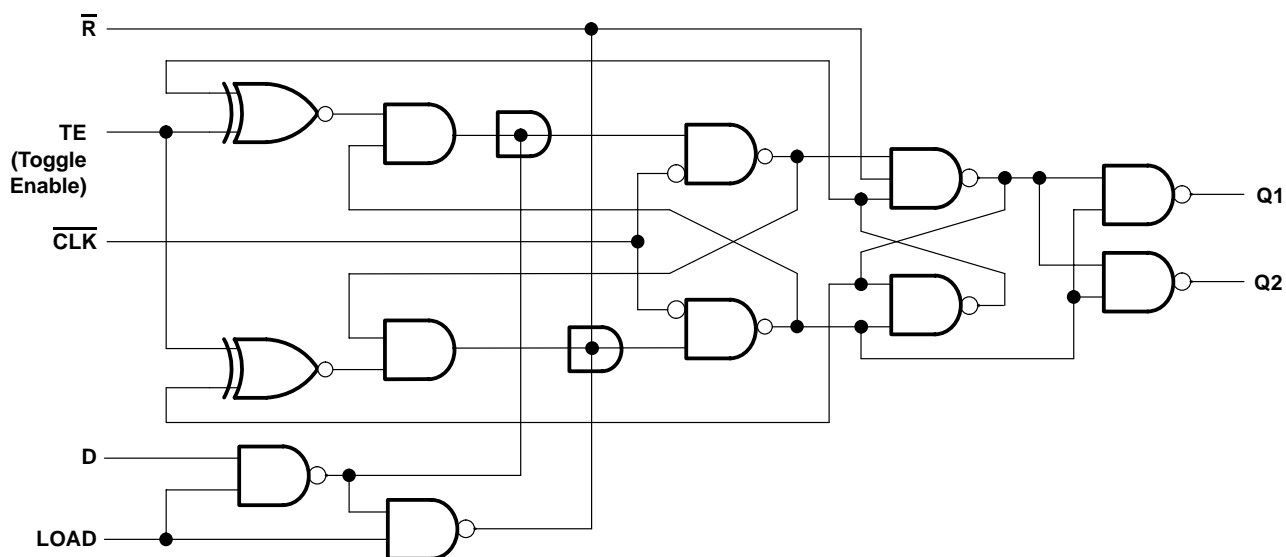
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### logic symbol, each flip-flop



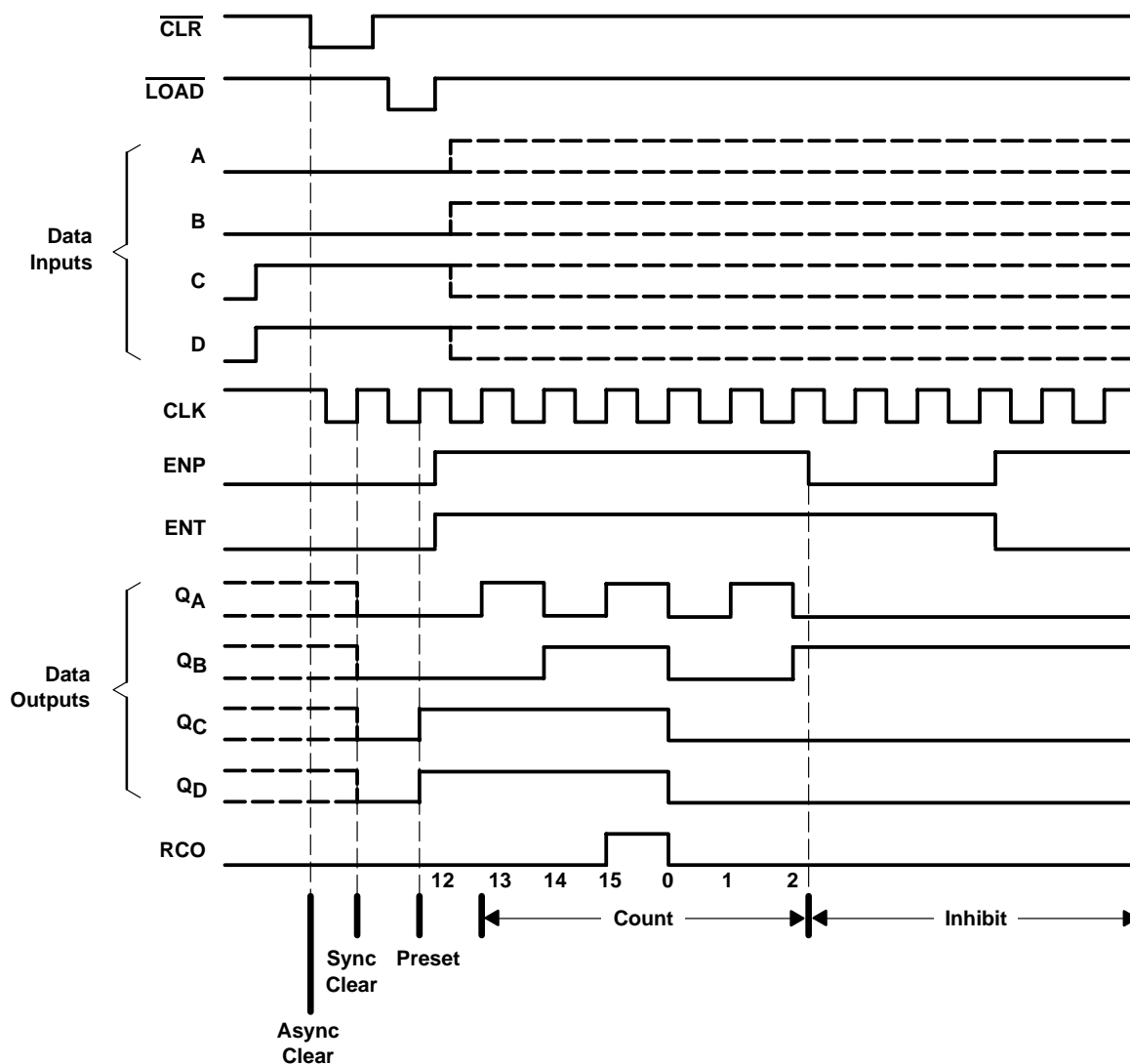
### logic diagram, each flip-flop (positive logic)



### typical clear, preset, count, and inhibit sequences

The following timing sequence is illustrated below:

1. Clear outputs to zero
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to $V_{CC}$
Current into any output in the low state	40 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
DB package	82°C/W
N package	67°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{IK}$ Input clamp current			–18	mA
$I_{OH}$ High-level output current			–1	mA
$I_{OL}$ Low-level output current			20	mA
$T_A$ Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.5	3.4		V
	$V_{CC} = 4.75$ V, $I_{OH} = -1$ mA	2.7			
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA		0.3	0.5	V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
$I_{IL}$	ENP, CLK, A, B, C, D			–0.6	mA
	ENT, LOAD			–1.2	
	CLR			–0.6	
$I_{OS}^{\S}$	$V_{CC} = 5.5$ V, $V_O = 0$	–60		–150	mA
$I_{CC}$	$V_{CC} = 5.5$ V		37	55	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>\S</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

				$V_{CC} = 5\text{ V}$ , $T_A = 25^{\circ}\text{C}$		MIN	MAX	UNIT
				MIN	MAX			
f <sub>clock</sub>	Clock frequency			0	100	0	90	MHz
t <sub>w</sub>	Pulse duration	CLK high or low (loading)		5		5		ns
		CLK (counting)	High	4		4		
			Low	6		7		
		CLR low		5		5		
t <sub>su</sub>	Setup time	Data before CLK↑	High or low	5		5		ns
		LOAD before CLK↑	High	11		11.5		
			Low	8.5		9.5		
		ENP and ENT before CLK↑	High	11		11.5		
			Low	5		5		
t <sub>h</sub>	Hold time	Data after CLK↑	High or low	2		2		ns
		LOAD after CLK↑	High	2		2		
			Low	0		0		
		ENP and ENT after CLK↑		High or low	0		0	
t <sub>su</sub>	Inactive-state setup time, CLR high before CLK↑†			6		6		ns

<sup>†</sup> Inactive-state setup time also is referred to as recovery time.

### switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $C_L = 50\text{ PF}$ , $R_L = 500\ \Omega$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V TO } 5.5\text{ V}$ , $C_L = 50\text{ PF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN TO MAX}^\ddagger$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$f_{\text{max}}$			100	120		90		MHz
$t_{\text{PLH}}$	CLK ( $\overline{\text{LOAD}}$ high)	Any Q	2.7	5.1	7.5	2.7	8.5	ns
$t_{\text{PHL}}$			2.7	7.1	10	2.7	11	
$t_{\text{PLH}}$	CLK ( $\overline{\text{LOAD}}$ low)	Any Q	3.2	5.6	8.5	3.2	9.5	ns
$t_{\text{PHL}}$			3.2	5.6	8.5	3.2	9.5	
$t_{\text{PLH}}$	CLK	RCO	4.2	9.6	14	4.2	15	ns
$t_{\text{PHL}}$			4.2	9.6	14	4.2	15	
$t_{\text{PLH}}$	ENT	RCO	1.7	4.1	7.5	1.7	8.5	ns
$t_{\text{PHL}}$			1.7	4.1	7.5	1.7	8.5	
$t_{\text{PHL}}$	CLR	Any Q	4.7	8.6	12	4.7	13	ns
		RCO	3.7	7.6	10.5	3.7	11.5	

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 4: Load circuits and waveforms are shown in Figure 1.

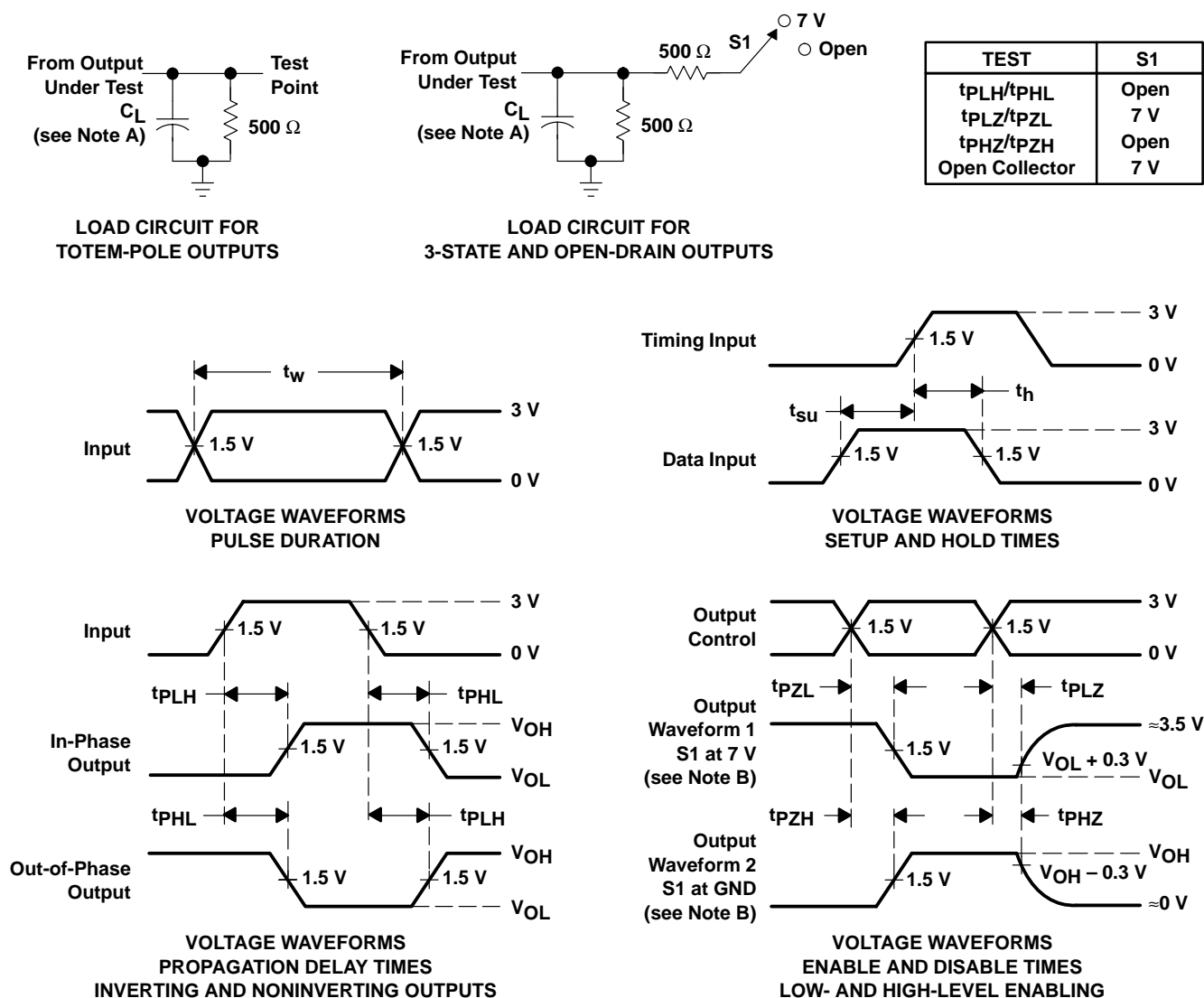


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### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ , duty cycle = 50%.
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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