DSbD Cohort 2 Results

Pytilia

24/02/2023

This document shows the results obtained from the packet processing application created by Pytilia as part of the DSbD Cohort 2 TAP. The packet processing application has 3 different modes of operation. The first involves a consumer in the same address space/process receiving the packets via CHERI capabilities. The second involves a consumer in a separate listener application receiving packets via traditional IPC methodology, using UDP sockets for communication. The third mode of operation involves the packets being read into a buffer and freed after no processing occurs, allowing the noise in the results to be removed.

1 Packet Processing Latency against Packet Count

In this section, packet count was varied between 20,000 and 200,000 in increments of 20,000. The packet size remained constant at 512B.

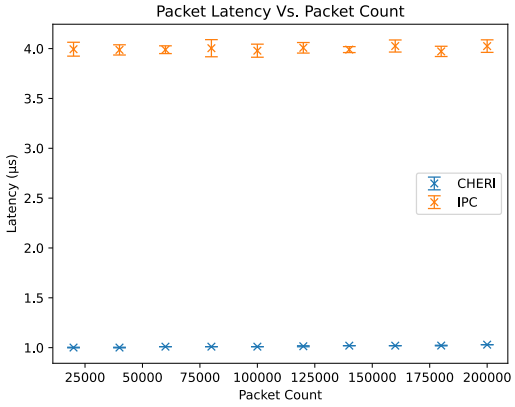

Figure 1: Packet processing latency against packet count.

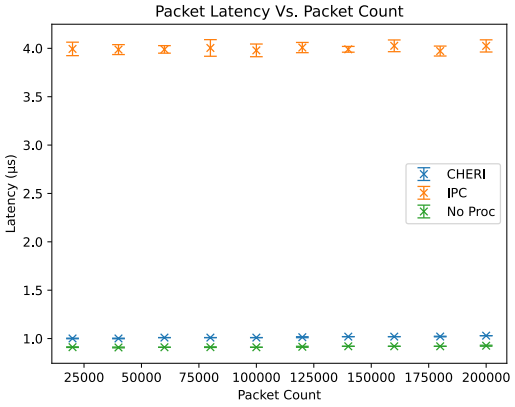

Figure 2: Packet processing latency against packet count for all 3 modes of operation.

Figure 1 shows that the CHERI-enabled plugin had a lower packet processing latency than the IPC mode of communication. The packet count did not appear to affect the average packet processing latency in any significant way. Figure 2 shows that the noise in the packet processing latency is significant in relation to the CHERI-based mode of operation.

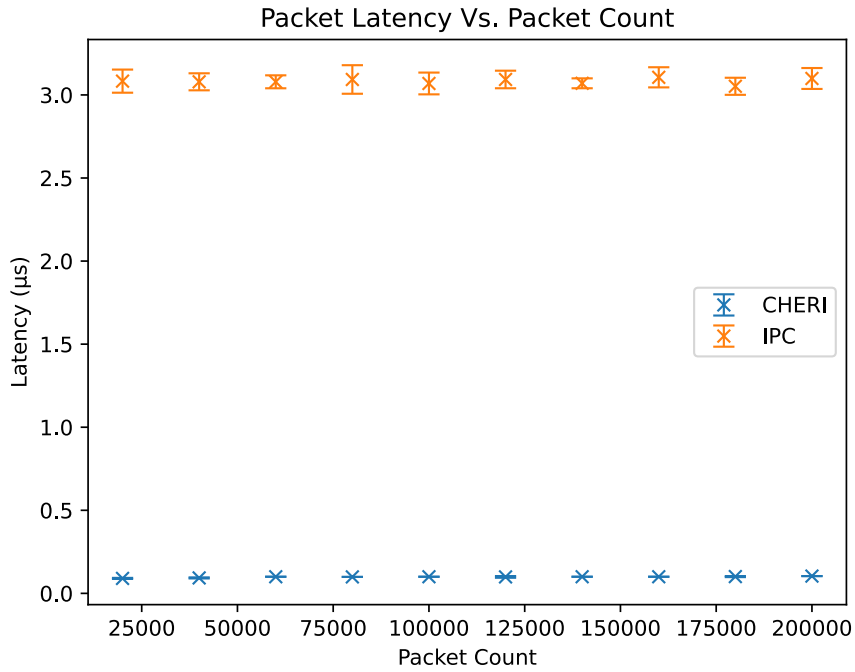

Figure 3: Adjusted packet processing latency against packet count.

Figure 3 was generated by subtracting the calculated average packet processing latency when no processing occurs from the results obtained from the 2 main modes of operation.

Tables 1 and 2 below show the average adjusted packet processing latencies for the two processing modes of operation for varying packet counts.

Packet Count	20,000	40,000	60,000	80,000	100,000
(CHERI) Latency/μs	0.09	0.09	0.10	0.10	0.10
(IPC) Latency/μs	3.08	3.08	3.08	3.09	3.07

Table 1: Adjusted packet processing latencies for different packet counts.

Packet Count	120,000	140,000	160,000	180,000	200,000
Latency/μs (CHERI)	0.10	0.10	0.10	0.10	0.10
Latency/μs (IPC)	3.09	3.07	3.11	3.05	3.10

Table 2: Adjusted packet processing latencies for different packet counts.

2 Packet Processing Latency against Packet Size

In this section, packet size was varied between 512B and 8KiB in ascending powers of 2. The packet count remained constant at 100,000.

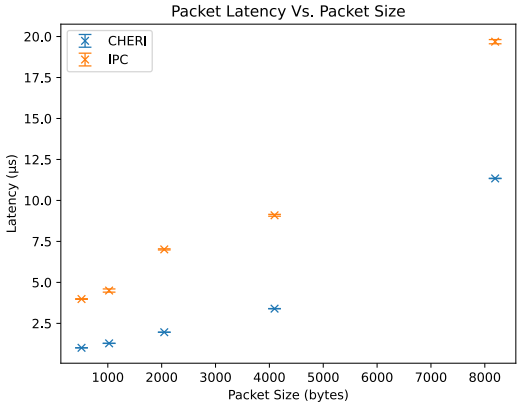

Figure 4: Packet processing latency against packet size.

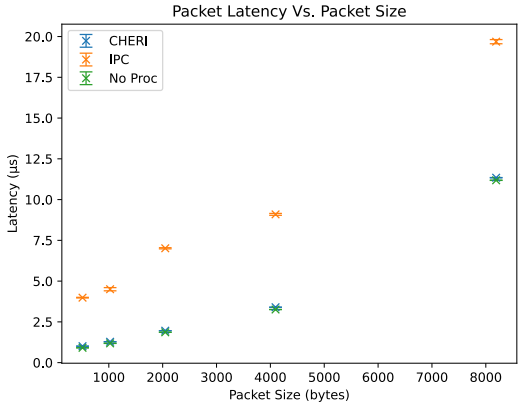

Figure 5: Packet processing latency against packet size for all 3 modes of operation.

Figure 4 shows that the CHERI-enabled plugin had a lower packet processing latency than the IPC mode of communication. This figure appears to show that packet size increases the latency for both modes of operation. Figure 5, however, shows that the noise in the packet processing latency at approximately the same rate as the CHERI-based mode of operation.

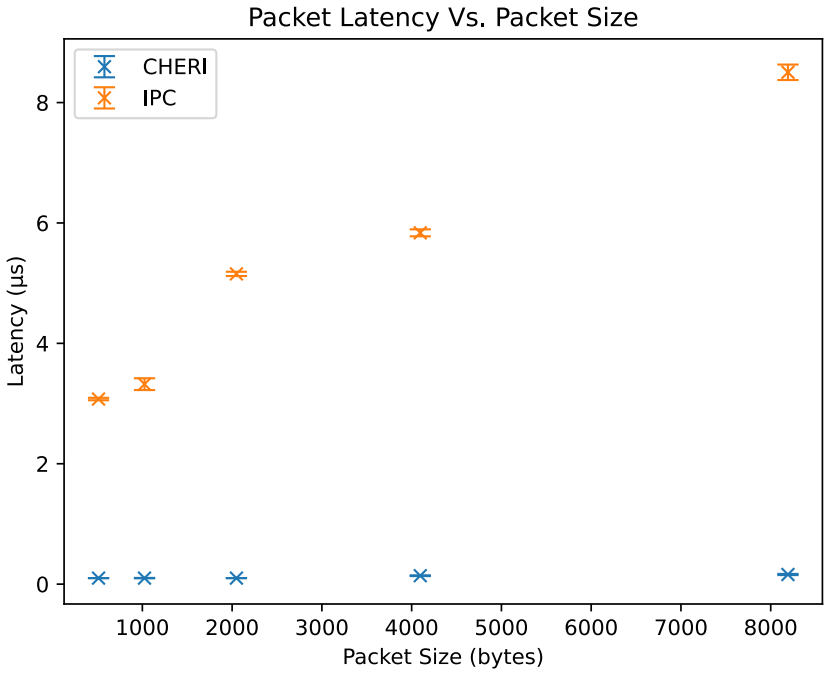

Figure 6: Adjusted packet processing latency against packet size.

Figure 6 was generated by subtracting the calculated average packet processing latency when no processing occurs from the results obtained from the 2 main modes of operation. This shows

that as packet size increases, the latency in the IPC mode of operation increases, whereas the CHERI-based mode of operation remains about constant.

Table 3 below shows the average adjusted packet processing latencies for the two processing modes of operation, for varying packet sizes.

Packet Size/B	512	1,024	2,048	4,096	8,192
(CHERI) Latency/μs	0.10	0.10	0.10	0.14	0.16
(IPC) Latency/μs	3.08	3.32	5.15	5.84	8.50

Table 3: Adjusted packet processing latencies for different packet sizes.

3 CPU Utilisation against Packet Count

In this section, packet count was varied between 20,000 and 200,000 in increments of 20,000. The packet size remained constant at 512B.

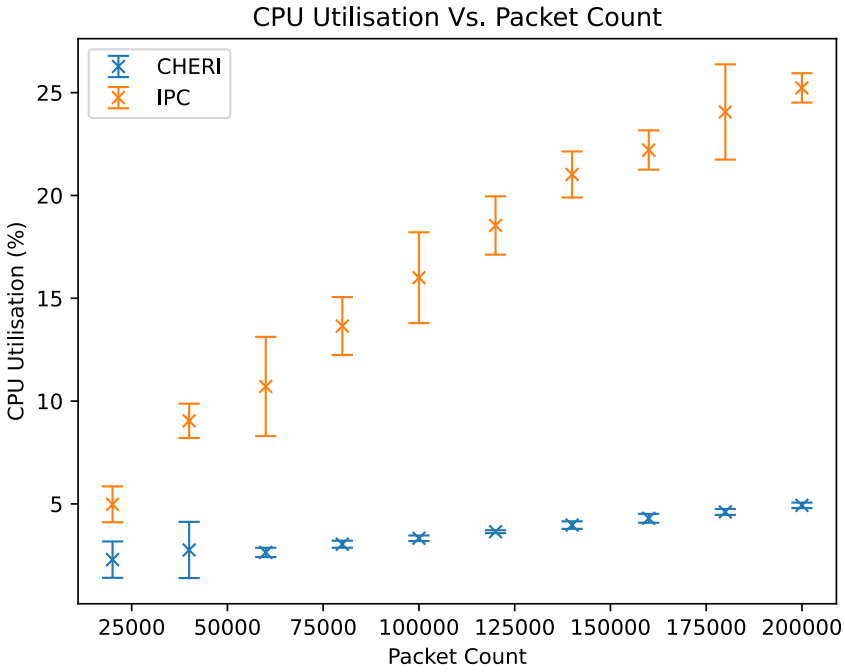

Figure 7: CPU Utilisation against packet count.

Figure 7 shows that as packet count increases, the CPU utilisation increases for both main modes of operation. The increase is significantly higher, however, for the IPC mode of operation. This indicates that as packet count increases, the benefit of using CHERI capabilities also increases.

4 CPU Utilisation against Packet Size

In this section, packet size was varied between 512B and 8KiB in ascending powers of 2. The packet count remained constant at 100,000.

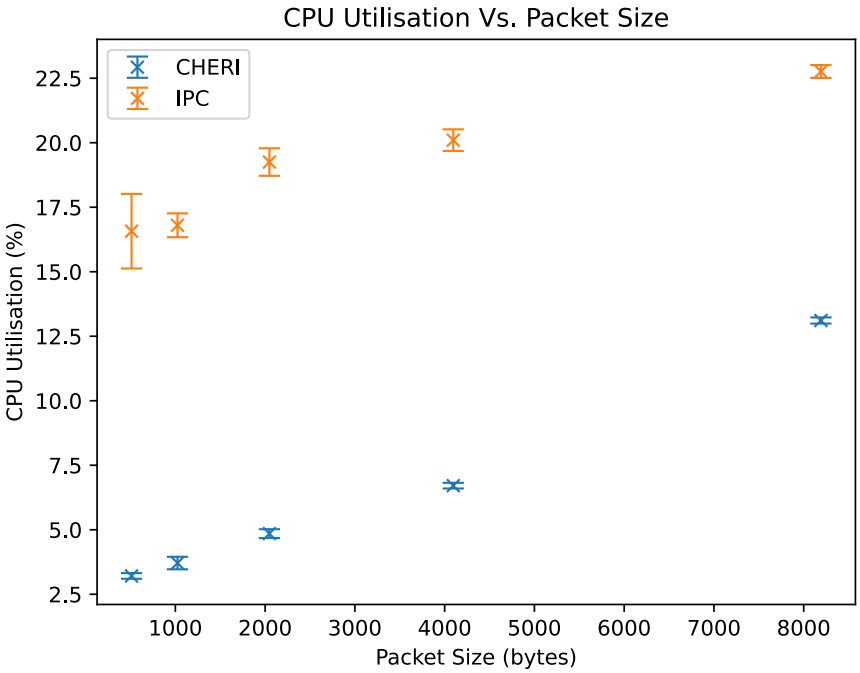

Figure 8: CPU Utilisation against packet size.

Figure 8 shows that as packet count increases, the CPU utilisation increases for both main modes of operation.