

Ben-Gurion University of the Negev

Faculty of Engineering Science

School of Electrical and Computer Engineering

Dept. of Electrical and Computer Engineering

Fourth Year Engineering Project

PDR

P4 based Caching-based Acceleration Mechanisms in Datacenter Networks

|  |  |  |  |
| --- | --- | --- | --- |
|  | **p-2022-035** | | **Project number:** |
| **Nisani Amit**  **205664345** | | **Kedik Michael**  **316645415** | **Students**  **(name & ID):** |
|  | **Prof. Avin Chen, Dr. Scalosub Gabriel** | | **Supervisors:** |
|  | **29/10/22** | | **Submitting date:** |

# **Abstract**

**P4 based Caching-based Acceleration Mechanisms in Datacenter Networks**

Students Names: Kedik Michael, Nisani Amit

kedikm@post.bgu.ac.il

Advisers’ Names: Prof. Avin Chen, Dr. Scalosub Gabriel

## English abstract

Switches in data center networks are required to store an enormous amount of traffic rules. Usually, those rules are stored in an external device, called a controller, to which the access slows the network’s performance.

The purpose of the project is to find a solution that decreases multiple access to this external device by using Caching-based Acceleration Mechanisms to speed up the routing process.

Our objective is to minimize the number of accesses to the controller, by using caching technologies and re-placing forwarding rules in distinct switches, which will speed up the overall throughput in the network.

The innovation is using the Cache Mechanisms and the connectivity between switches from different layers in the topology to get the necessary forwarding rule.

The proposed method is to create a basic network, based on a data center topology, with several switches that have cache storage for the most used forwarding rules. In case of missing information, a switch sends the request to a higher-ranked switch. The highest-rank switch is the controller, which holds the entire forwarding policy.

We expect to get a significant speed-up of our overall throughput in the network.

**Keywords:** Switch, Cache, Routing, Controller, Mininet, P4, Data center, Software-Defined Networking.

**מנגנוני האצה מבוססי מטמון ברשתות מרכזי נתונים מבוססי P4**

שמות הסטודנטים: קדיק מיכאל, ניסני עמית

כתובת מייל: kedikm@post.bgu.ac.il

שם המנחה: פרופ' אבין חן, דר' גבריאל סקלוסוב

## תקציר

מתגים ברשתות מרכזי נתונים נדרשים לאחסן כמות גדולה של חוקי תעבורה. בדרך כלל, חוקים אלה מאוחסנים במכשיר חיצוני, הנקרא בקר, שהגישה אליו מאטה את ביצועי הרשת.

מטרת הפרויקט היא למצוא פתרון שיגרום להפחתת כמות הגישות למכשיר החיצוני, על ידי שימוש במנגנוני האצה מבוססי מטמון כדי לייעל את תהליך הניתוב.

המטרה שלנו היא למזער את מספר הגישות לבקר, על ידי שימוש בטכנולוגיות מבוססות זכרון מטמון ועדכון של חוקי תעבורה במתגים, ובכך לשפר את התפוקה הכוללת ברשת.

החדשנות היא שימוש במנגנוני המטמון ובקישוריות בין מתגים משכבות שונות בטופולוגיה, כדי להפחית את התעבורה העודפת ברשת.

השיטה המוצעת היא יצירת רשת בסיסית, המבוססת על טופולוגיה של מרכז נתונים, עם מספר מתגים בעלי זכרון מטמון עבור חוקי התעבורה הרלוונטיים. במקרה שלמתג אין את חוק התעבורה הרלוונטי כאשר מגיעה אליו חבילת מידע, הוא שולח בקשת ניתוב למתג בעל דירוג גבוה יותר. המתג בעל הדרגה הגבוהה ביותר הוא הבקר, המחזיק בכל מדיניות ההעברה.

אנו מצפים לקבל שיפור משמעותי של התפוקה הכוללת ברשת.

# **Research Proposal**

**Project’s name:** P4 based Caching-based Acceleration Mechanisms in Datacenter Networks.

**Project application:** increasing the throughput of a data center will reduce unnecessary traffic in the network. It will allow services that are more efficient by using the same resources.

**Technology:**

* **Mininet** – Mininet is a network emulator, which creates a network of virtual hosts, switches, controllers, and links. Its support flexible custom routing and Software-Defined Networking.[1]
* **P4 -** Programming Protocol-independent Packet Processors (P4) is a domain-specific language for network devices, specifying how data plane devices (switches, NICs, routers, filters, etc.) process packets.[2]
* **P4runtime -** The P4Runtime API is a control plane specification for controlling the data plane elements of a device defined or described by a P4 program.[3]
* **SDN -** Software Defined Networking (SDN) advocates separation of control and data plane. This paradigm shift in networking architecture.[4]
* **SDN Controller -** An SDN controller has complete view of the network. The controller also has the ability to change the network structure and services at run time.[4]

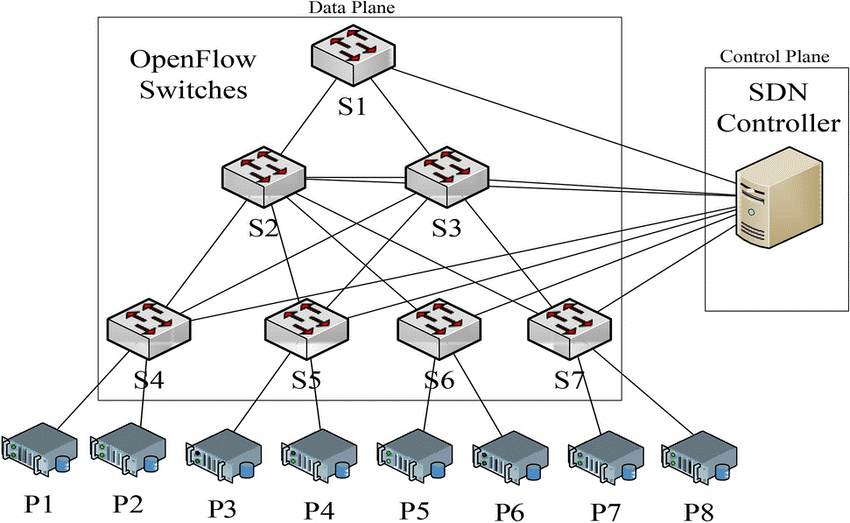


Figure 1: block diagram of SDN network using SDN controller

We will adjust routing table and allocate shared-cache of the switches through the SDN controller, to decrease the number of forwarding requests arriving to the SDN controller.

By using Mininet's emulator we can mimic the behavior and connectivity of a DC network and thus to get more realistic results, as seen in figure 1.

# **Proposed method**

In modern IP routers, Internet Protocol (IP) lookup forms a bottleneck in packet forwarding because the lookup speed cannot catch up with the increase in link bandwidth.[5] Therefore, there are two main approaches to that issue –

* Ternary content-addressable memories (TCAMs) have emerged as viable devices for designing high-throughput forwarding engines on routers. TCAMs search the data (IP address) in a single clock cycle. Because of this property, TCAMs are particularly attractive for packet forwarding and classifications. Despite these advantages, large TCAM arrays have high power consumption and lack scalable design schemes, which limit their use.[5]
* The use of caching base mechanism - to serve the applications running on a computer in distributed systems, not only the local memory but also the memory on remote servers must be effectively managed to minimize operations. The critical challenges in an effective memory cache management include: Insightfully understanding and quantifying the locality inherent in the memory access requests and Intelligently placing and replacing data in the multi-level caches of a distributed system.[6]

# **Proposed solution**

In this project, we will create a Data-Center network layout consisting of several layers so that each layer’s purpose is different from the one below or under it. We will do so by using Mininet, which is a network emulator that is used to emulate virtual hosts, routers, network controllers, and switches as mentioned above.

We will implement a cache mechanism on every switch in the network that will contain

forwarding rules needed by the switch. If the switch knows where to forward a certain packet, it will be considered a cache hit; otherwise, it will be considered a cache miss.

The goal of this proposed solution is that the cache will hold the rules needed to handle as many packets as possible, in order to maximize the cache-hit rate and reduce the number of hops to the higher layers in the network, thus reducing the overall unnecessary traffic in the network.

When a cache miss happens, the unknown destination packet will be sent to a higher-layer switch, hopefully, that this switch will contain the destination in its cache table. This action will continue until a cache hit will occur or the packet will reach the final layer, the controller that holds the information about all the destinations in our network.

The controller will manage our distributed algorithm, inserting rules to caches in switches belonging to different layers in the topology.

# References

[1] “**Mininet Overview**” mininet.org. <http://mininet.org/overview> (accessed: Oct. 26, 2022).

[2] **"P4 Open Source"** P4.org. <https://p4.org/> (accessed: Oct. 26, 2022).

[3] **"P4Runtime Specification"** P4.org. <https://p4.org/p4-spec/p4runtime/main/P4Runtime-Spec.html#tab-p4-type-usage> (accessed: Oct. 26, 2022).

[4] Zuhran Khan Khattak, Muhammad Awais and Adnan Iqbal, **"Performance Evaluation of OpenDaylight SDN Controller"**, [IEEE International Conference on Parallel and Distributed Systems (ICPADS)](https://ieeexplore.ieee.org/xpl/conhome/7092978/proceeding), 2014.

[5] V. Ravikumar and R. Mahapatra, "**TCAM architecture for IP lookup using prefix properties**", IEEE Micro, vol. 24, no. 2, pp. 60-69, March-April 2004.

[6] S. Jiang, "**Efficient Caching Algorithms for Memory Management in Computer Systems**", College of William & Mary - Arts & Sciences, 2004.

**הערכה לשיחת סקר תכנון ראשוני (PDR)**

אם יש צורך, לכל סטודנט/ית בנפרד

מספר הפרויקט: \_\_\_\_\_-\_\_\_\_20-P

שם הפרויקט:

שם המנחה החיצוני:

שם המנחה מהמחלקה:

שם הסטודנט/ית: ת.ז.:

|  |  |  |  |
| --- | --- | --- | --- |
| % | מהות | ציון | הערות |
| 100 | שיחה + דו"ח - הבנת הנושא ומהות העשייה, הבנת הצורך, סביבת היישום, הגדרת מדדים, מקורות ועבודות דומות.  הצגת התקצירים, מפרט טכני/הצעת מחקר והצעת תכנון מפורטים. |  |  |
|  |  |  |  |
|  |  |  |  |
|  | ציון סופי |  |  |

הערות: