CSE 291 Securing Processor Architectures - Lab 1

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1 Discussion Question 1

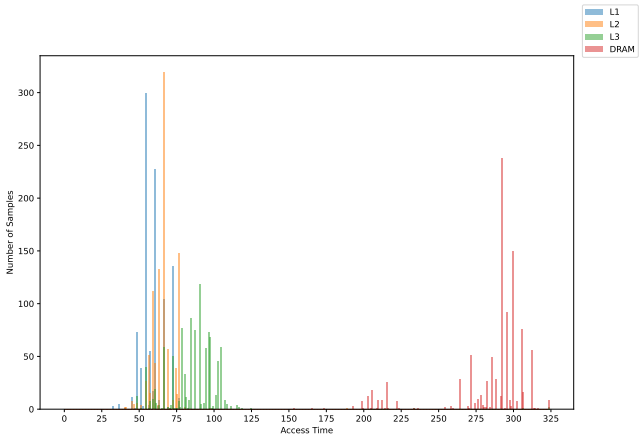
	Cache Line Size	Total	Ways	Sets	Raw Latency
L1	64 bytes	32 KiB	8	64	4
L2	64 bytes	256 KiB	8	512	12
L3	64 bytes	8 MiB	16	8192	26-31

2 Discussion Question 2

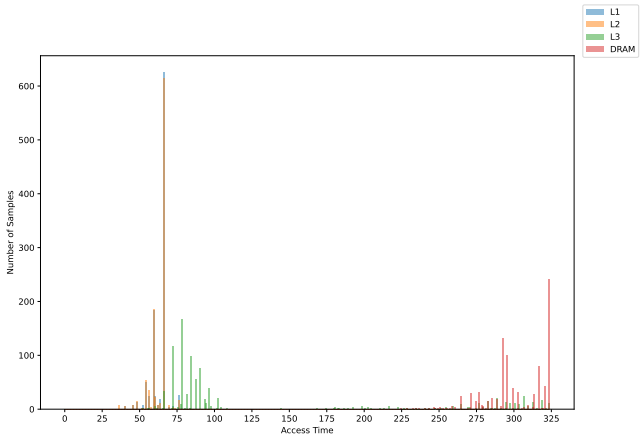
L2_LINES: 32768 bytes / 64 bytes = 512
L3_LINES: 262144 bytes / 64 bytes = 4096

3 Graphs

3.1 When CPU is not warmed up



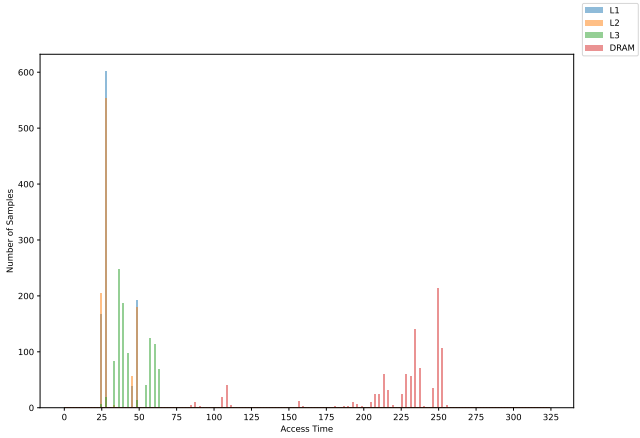
(a) My first attempt



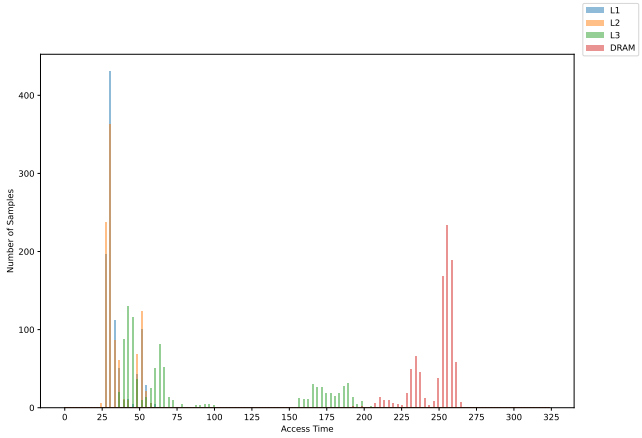
(b) Reference

In my first attempt I did not realize the CPU had to be warmed up, Anything past 78 and before 150 is L3, after 150 is DRAM. The reference is shown on the right

3.2 When CPU is warmed up



(a) My second attempt



(b) Reference when CPU is warmed up

I then changed my code to try to warm up the CPU when run. This moved the cutoff from from L2 to L3 to about 50. DRAM is anything over 80. If there where not some L1 and L2 times near 50, the threshold for L3 could be moved to around 27. However this is similar to the Reference, so I think this good enough.

4 Discussion Question 3

L2_L3_THRESHOLD: 50
L3_DRAM_THRESHOLD: 80

5 Question 6

To indicate that a message is being sent, the sender will cause contention in an agreed upon set in the L2 cache by accessing multiple different tags at the same time for that index. When this happens, the receiver knows a message is being sent.

To send data, 8 cache sets are used. To indicate a 1, a set is made contentious in the L2 by the sender. To send a 0 nothing is done in that set. Since there could be interference, this is done across 3 groups of 8 sets, and a vote is done to decided if that bit was a 1 or 0.

That means 24 cache sets are used to send bits, and 1 cache set is used to indicate if the sender is sending or not.

Huge pages are used so that the index bits of L2 are effectively virtually addressed, allowing them to be picked by the program