SOLUTION: Homework 4 – Timers/Counters

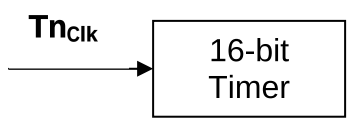
Assigned Date: Friday, October 19, 2012

Due Date: Friday, October 26, 2012

Weight: 60 pts

Problem 1 (10 points total)

Let's say that we take our peripheral clock (40 MHz) and divide it by 64. We call the divided frequency clock Tn_{Clk}, and use this clock to control the incrementing of our 16-bit timer/counter. Let's further add that we toggle the signal produced by our timer/counter every time the 16-bit timer matches our period register value of 0x07FF. What is the resulting frequency of our signal obtained (show the result to the hundredths place)? Show all calculations!



Tn_{Clk} = 40 MHz / 64 = 625 kHz

1 cc of Tn_{Clk} = Timer++ (incrementation of Timer) ➔ 0x07FF PR + 1 reset = 1/2 period = 1 toggle

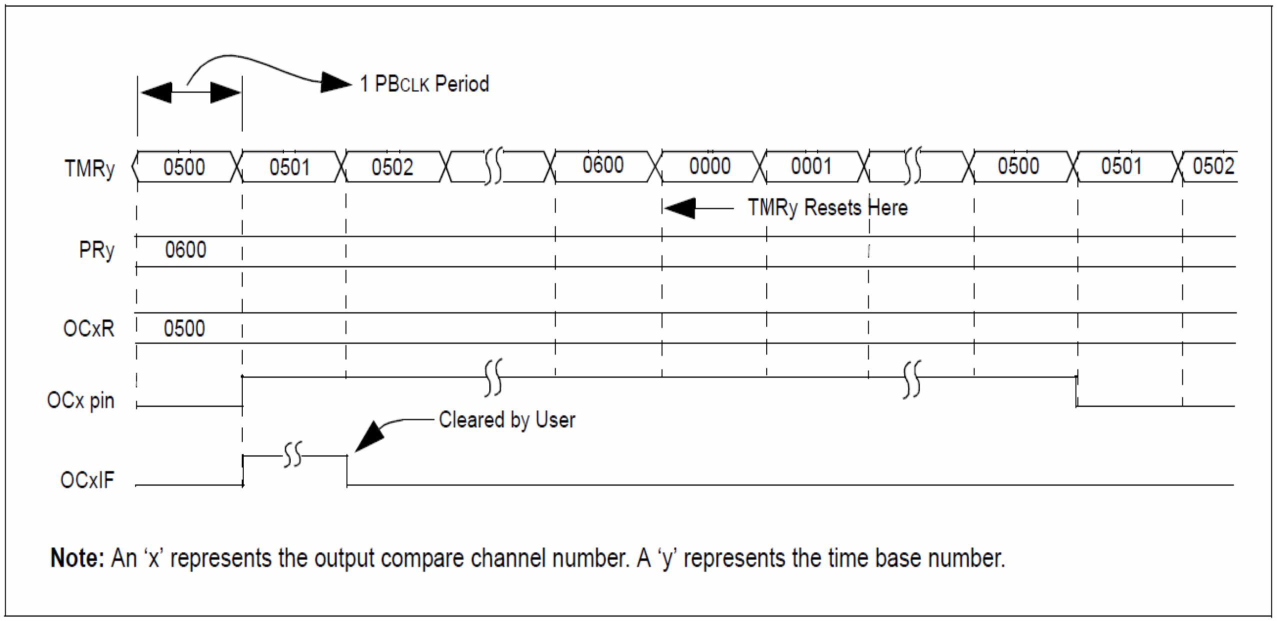
1 T of resultant signal = 2 toggles → (0x07FF PR + 1 reset) * 2 = (2047_{10} PR + 1 reset) * 2

Let's call our resultant signal S, T_S = [(1 / Tn_{Clk}) * 2048_{10} cc] * 2 toggles = 6.55 ms

Thus, f_S = (1 / T_S) = 152.59 Hz

Problem 2 (10 points total)

Provided the following diagram and the fact PR_y and OCxR remain constant, what is the resulting frequency of the OCx signal (show the result to the hundredths place)? What is the duty cycle of OCx (show the result to the hundredths place)? NOTE: assume TMR_y is incrementing every 1 microsecond.



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We know the following:

- PRy = 0x0600
- OCxR = 0x0500
- T_{Ty} = 1 us; f_{Ty} = 1 / 1 us = 1 MHz
- OCx toggles on a compare match

What is the resulting frequency of OCx?

Note: OCx does not start a repeatable cycle until after the first 501 cycles (TMR_y = 0 → TMR_y = 500) of f_{Ty}. Our calculation must compute the frequency of OCx after this point.

Let's first compute the period of OCx. We'll call this period T_{OCx}.

T_{OCx} = [(OCxR + 1 reset) + (PRy – OcxR – 1 reset)] * 1 us * 2

= [(0x0500 + 1) + (0x0600 – 0x0500 – 1)] * 1 us * 2

= [(1280_{10} + 1) + (1536_{10} – 1280_{10} – 1)] * 1 us * 2, hence

*= PRy * 1 us * 2 =* 1536_{10} ** 1 us * 2 = 3.072 ms*

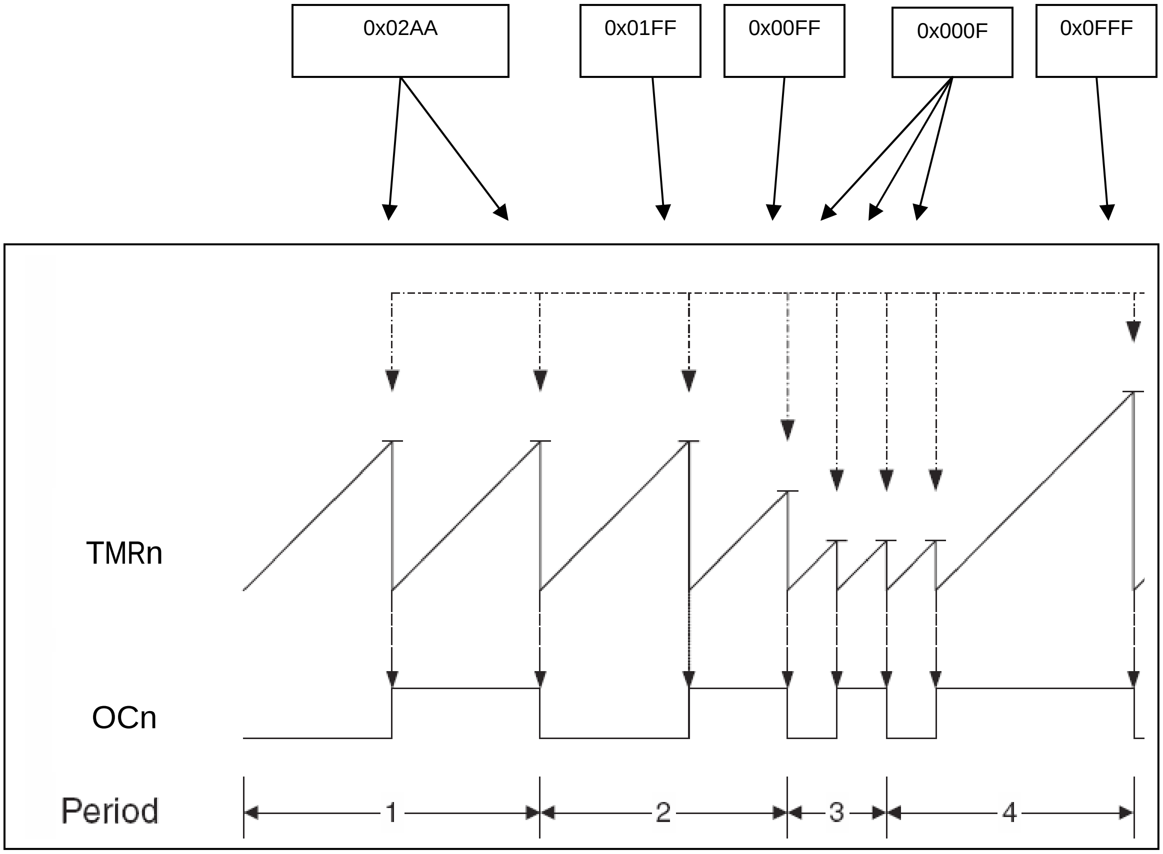
f_{OCx} = 1 / T_{OCx} = 325.52 Hz

What is the resulting duty cycle of OCx?

Duty cycle = (0x0600) / (0x0600 * 2) = 50.00 %

Problem 3 (30 points total)

For each of the four periods shown below for the OCn signal, (a) calculate the period in seconds, (b) calculate the corresponding frequency, and (c) calculate the duty cycle as a percentage. Assume that TMRn is incremented at a frequency of clk_{Tn} = 80 MHz/8.



Note: Computations list numbers in decimal

Period	Calculated Period	Frequency	Duty Cycle
1	(682 cc * 2) * 0.1 us = **136.40 us**	(1 / 136.40 us) = **7,331.38 Hz**	(682 cc / 1364 cc) = **50.00%**
2	(511 cc + 255 cc) * 0.1 us = **76.60 us**	(1 / 76.60 us) = **13,054.83 Hz**	(255 cc / 766 cc) = **33.29%**
3	(15 cc * 2) * 0.1 us = **3.00 us**	(1 / 3.00 us) = **333,333.33 Hz**	(15 cc / 30 cc) **= 50.00%**
4	(15 cc + 4095 cc) * 0.1 us = **411.00 us**	(1 / 411.00 us) = **2,433.09 Hz**	(4095 cc / 4110 cc) = **99.64%**

Problem 4 (10 points total)

List and describe 5 real-world applications in which 16-bit and/or 32-bit timers may be used.

- Robotics, car control systems, etc……..