Zhanghao Wu

Undergraduate in computer science

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Education

Shanghai Jiao Tong University(SJTU) *Shanghai, China*

B.S. in Computer Science *Sep. 2016 - Jun. 2020 (expected)*

- Member of ACM Class, an elite CS program for top 5% talented students.
- GPA: 92.07 / 100, Rank:2 / 38.
- Research interests: Computer Architecture and Deep Learning.

Research Experience

SpeechLab *Shanghai Jiao Tong University*

Undergraduate Researcher, advised by Prof. Kai Yu *Jul. 2018 - PRESENT*

- Focusing on Rich Audio Analysis (RAA), analysis and classification of non-text information within human speech.
- Designed a Variational Auto-encoder (VAE) data augmentation model to improve the training process of speaker verification. (A submitted paper)
- Implemented a Deep Canonical Correlation Analysis (DCCA) to combine i-vector and x-vector, which are two kinds of highly complementary embedding of speaker.

Teaching Experience

C++ Programming(CS152) *Shanghai Jiao Tong University*

Teaching Assistant *Spring 2018*

- Gave lectures on how to begin programming and what dynamic programming is.
- Designed part of the homework and exam problems, to help students practice C++ programming.

Honors & Awards

2017 **Outstanding Winner**, Mathematical Contest in Modeling (Top 0.5%, international) *COMAP*

2018 **National Scholarship** *Ministry of Education of P.R. China*

2017 **Fan Hsu-Chi Chancellor's Scholarship**, (Top 0.1%) *Shanghai Jiao Tong University*

2017 **Merit Student** *Shanghai Jiao Tong University*

2016 - 2018 **Zhiyuan Honorary Scholarship** *Shanghai Jiao Tong University*

Selected Projects

MW Compiler *Jun. 2018*

Michaelvll/MWCompiler

- Designed a compiler implemented in Java from scratch, translating Mx*, a Java-and-C-like language, program into x64-nasm code.
- Implemented optimizations for the compiler, faster than gcc O1 on test set, **98/100**.

RISCV CPU *Jan. 2018*

Michaelvll/RISCV_CPU

- Designed and implemented a FPGA-supported RISC-V CPU with 5-stage pipeline implemented in Verilog HDL. And becomes the only two implementation that support FPGA in class, **100/100**.

Train Ticket *Jun. 2017*

TimerChen/TrainTickets

- Implemented the frontend UI for the Train Ticket project, a group project for Data Structure 2017 (CS147), SJTU.

Chinese Land Battle Chess AI *Nov. 2016*

Michaelvll/Chinese-Land-Battle-Chess-AI

- Designed and Implemented a rule-based AI for Chinese Land Battle Chess, a course project for C++ Programming 2016(CS152), SJTU.