Zhanghao Wu

Undergraduate in computer science

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Research Interests

Deep learning, especially Natural Language Processing, Speech and Efficient Machine Learning.

Education

Shanghai Jiao Tong University (SJTU) *Shanghai, China*

Bachelor of Engineering in Computer Science at ACM Honors Class, Zhiyuan College *Sep. 2016 - Jun. 2020*

- **ACM Honors Class** is an elite CS program for top 5% talented students in Computer Science Department.
- GPA: Overall: **92.13/100** (3.99/4.3) | Ranking: **2nd/37** (in ACM Hornors Class).
- Advisors: Prof. Kai Yu, Prof. Yanmin Qian and Prof. Yong Yu.

Massachusetts Institute of Technology (MIT) *Cambridge, USA*

Research Assistant at HanLab, Microsystems Technology Laboratories *Jul. 2019 - Jan. 2020*

- Advisor: Prof. Song Han.

Publications

Efficient Transformer for Mobile Application

Zhanghao Wu, Zhijian Liu, Ji Lin, Yujun Lin and Song Han ICLR 2020 (submitted)

Data Augmentation using Variational Autoencoder for Embedding based Speaker Verification

Zhanghao Wu, Shuai Wang, Yanmin Qian and Kai Yu Interspeech 2019 **(oral)**

Real-Time Image Classification with Proxyless Neural Architecture Search And Quantization-Aware Finetuning

Han Cai, Tianzhe Wang, **Zhanghao Wu**, Kuan Wang, Ji Lin and Song Han ICCV 2019 workshop

Research Experience

HanLab *Massachusetts Institute of Technology, USA*

Research Assistant, supervised by Prof. Song Han *Jul. 2019 - Jan. 2020 (expected)*

- Focusing on privacy preserving and efficient machine learning.
- Working on efficient natural language processing, especially for machine translation. Proposed a novel primitive with higher capacity than the original transformer under mobile settings and submitted to ICLR 2020.
- Designed an efficient privacy-preserving cloud-edge inference method utilizing the linearity of neural networks.
- Won first place in the CVPR'19 Visual Wake Words challenge and third place (first place of all academic groups) in CVPR'19 Low Power Image Recognition Competition.

SpeechLab *Shanghai Jiao Tong University, China*

Undergraduate Researcher, advised by Prof. Yanmin Qian and Prof. Kai Yu *Jul. 2018 - PRESENT*

- Focused on Rich Audio Analysis (RAA), analysis and classification of non-text information within human speech.
- Implemented Deep Canonical Correlation Analysis (DCCA) in pytorch and released the code on GitHub.
- Participated in the translation of the book: *Reinforcement Learning: An Introduction by Sutton, R.S., Barto, A.G.*
- Established a VAE based data augmentation to improve the robustness of speaker verification systems by modelling the patterns of noise and reverberation in the speaker embeddings. It was accepted by Interspeech 2019 **(oral)**.

Honors & Awards

Competitions

- **First place**, Visual Wakeup Words (VWW) Challenge CVPR'19, *2019*
- **Third place**, Low Power Image Recognition Competition ICCV'19, *2019*
- **Outstanding Winner**, Mathematical Contest in Modeling (Top 0.5%) COMAP, *2017*

Scholarships

- **National Scholarship**, (Top 1%) Ministry of Education of P.R. China, *2018 & 2019*
- **Fan Hsu-Chi Chancellor's Scholarship**, (Top 0.1%) Shanghai Jiao Tong University, *2017*
- **Merit Student** Shanghai Jiao Tong University, *2017*
- **Zhiyuan Honorary Scholarship** Shanghai Jiao Tong University, *2016 - 2018*

Teaching Experience

Compiler (MS208), Teaching Assistant Shanghai Jiao Tong University, *Spring 2019*

C++ Programming (CS152), Teaching Assistant Shanghai Jiao Tong University, *Spring 2018*

Selected Projects

VWW mit-han-lab/VWW *May. 2019*

- Won first place in the CVPR'19 Visual Wake Words challenge. The task is human detection on IoT device that has a tight computation budget: <250KB model size, <250KB peak memory usage, <60M Mult-Adds.

DeepCCA Michaelvll/DeepCCA *Dec. 2018*

- An implementation of Deep Canonical Correlation Analysis in pytorch with 40 stars.

MW Compiler Michaelvll/MWCompiler *Jun. 2018*

- Designed a compiler implemented in Java from scratch, translating Mx*, a Java-and-C-like language, program into x64-nasm code.
- Implemented optimizations for the compiler, faster than gcc O1 on test set, **98/100**.

RISCV CPU Michaelvll/RISCV_CPU *Jan. 2018*

- An FPGA-supported RISC-V CPU with 5-stage pipeline in Verilog HDL. It was the only two implementations that could actually be executed on the FPGA in class, **100/100**.