CRICOS PROVIDER 00123M

School of Computer Science

COMP SCI 2000 Computer Systems
Lecture 5

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seekLIGHT

Review – Sequential logic

- This operates on data and a clock signal;
  as such, can be made to be *state*-aware and provide storage and synchronization services.
- Sequential devices are sometimes called “clocked devices”.
- All sequential chips can be based on one low-level sequential gate, called “data flip flop”, or DFF.
- We looked at the 1 and multiple bit register.

What we're doing now

- This lecture we're going to talk about:
  - Hardware clocks
  - Memory chip hierarchy
    - Flip-flop gates
    - Binary cells
    - Registers
    - Random Access Memory
  - Counters
  - Putting it all together

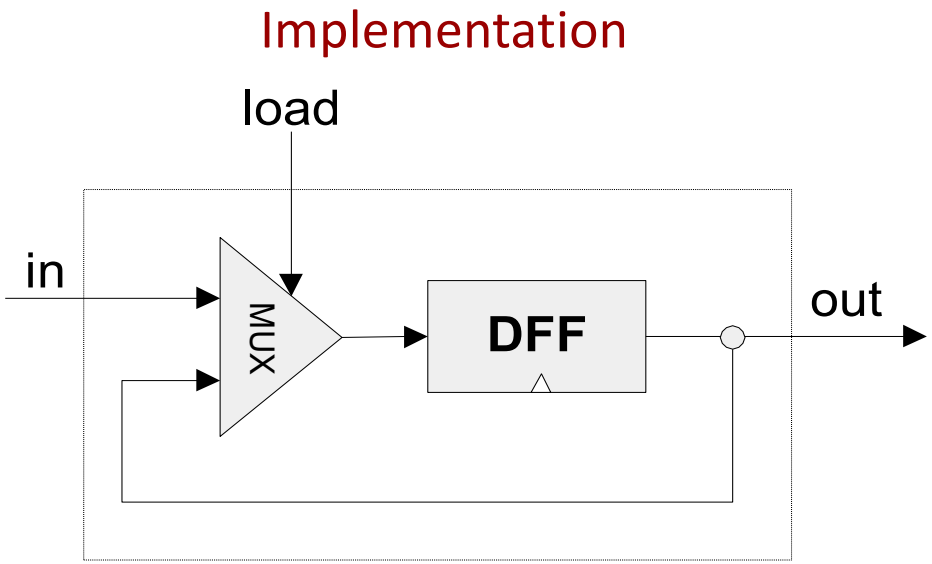
Random Access Memory

- We've seen what a multi-bit register looks like.
- But first…
- Terminology check! What are the following:
  - Bit
  - Byte
  - Word
- What do each of these look like in terms of abstract diagrams?

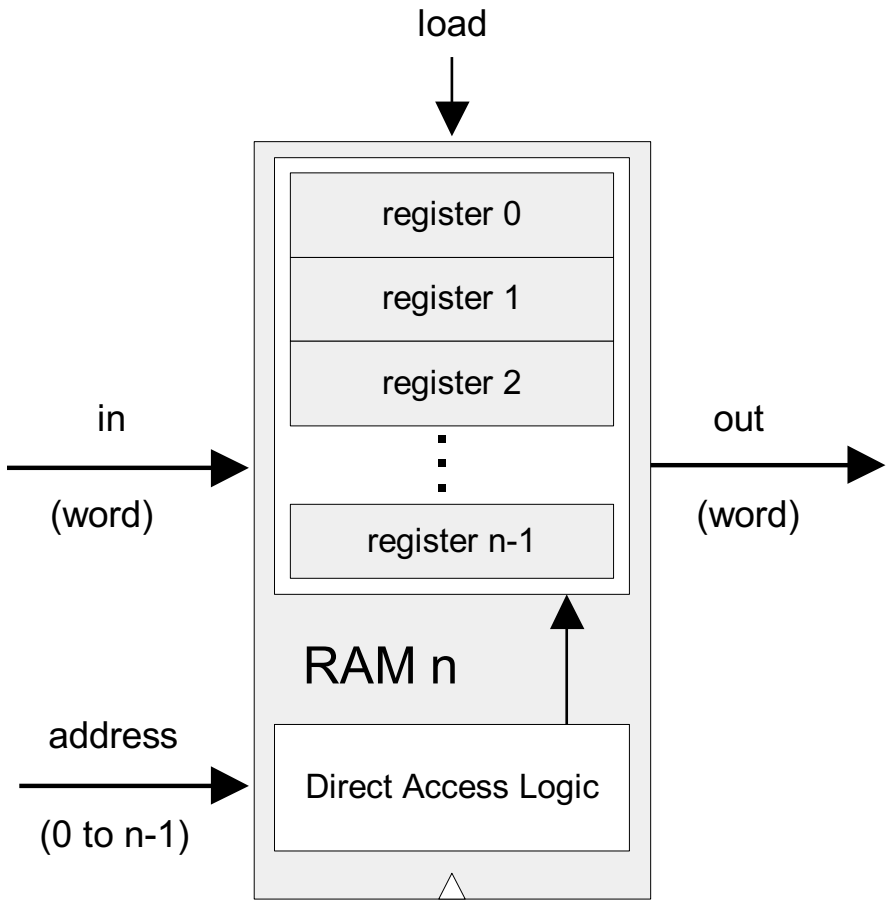
Lecture 5
Worksheet
Question 1

Abstract Memory Design

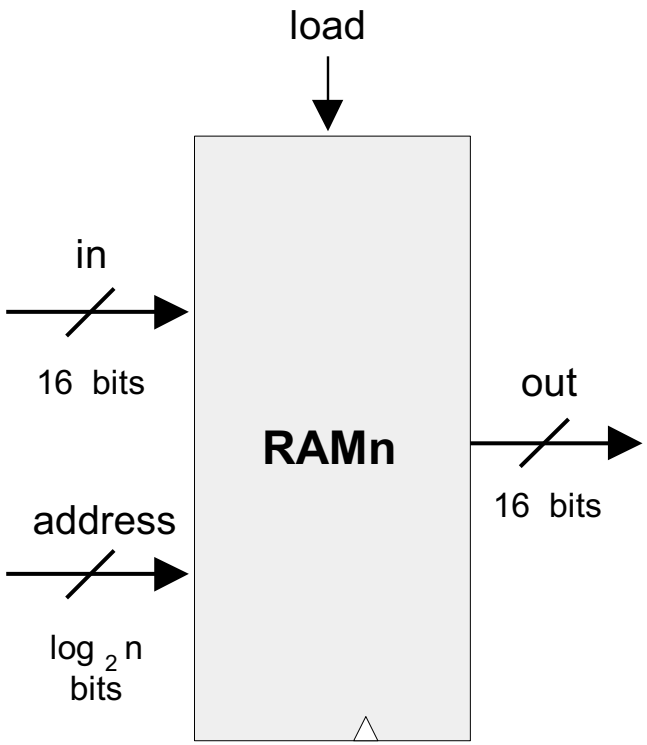
- What do you think RAM looks like as an abstract design?
- Remember the one bit register?
- (consider second part of question 1 on worksheet 1)



RAM


load
register 0
register 1
register 2
register n-1
in
(word)
out
(word)
RAM n
address
(0 to n-1)
Direct Access Logic

RAM interface

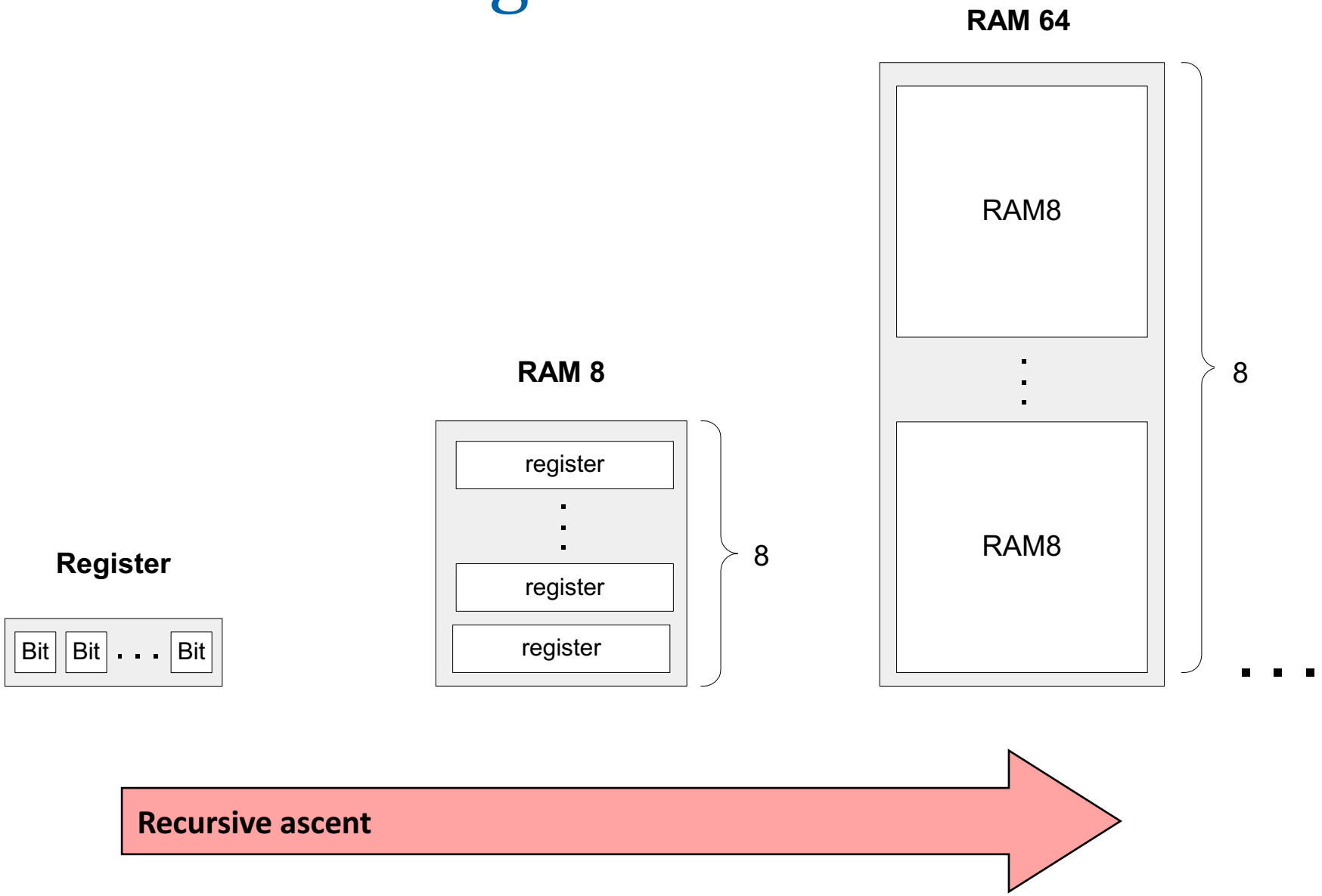



```
Chip name:   RAMn  // n and k are listed below
Inputs:      in[16], address[k], load
Outputs:     out[16]
Function:    out(t)=RAM[address(t)](t)
             If load(t-1) then
                RAM[address(t-1)](t)=in(t-1)
Comment:     "=" is a 16-bit operation.
```

The specific RAM chips needed for the Hack platform are:

Chip name	n	K
RAM8	8	3
RAM64	64	6
RAM512	512	9
RAM4K	4096	12
RAM16K	16384	14

From little things…



What else do we need?

- We can use the clock signal and our bit implementation to store things.
- Is this enough to run a program?
  - What's probably the most important thing to know when running a program?
  - (Is this the most important thing? Discuss!)

Lecture 5
worksheet
question 2

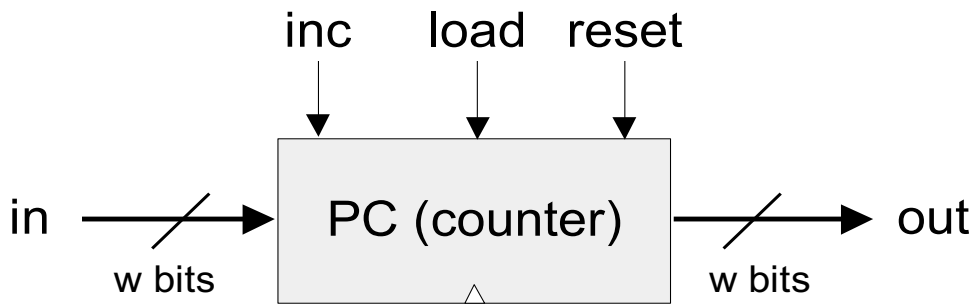
Program Counter

- We need to develop the logic for a counter as the simplest program is run from contiguous places in memory, one after the another.
- What do we need for a counter?

Program Counter

- We need to develop the logic for a counter as the simplest program is run from contiguous places in memory, one after the another.
- What do we need for a counter?
  - Set state to some base value
  - Increment state in every clock cycle
  - Stop incrementing over clock cycles
  - Reset state

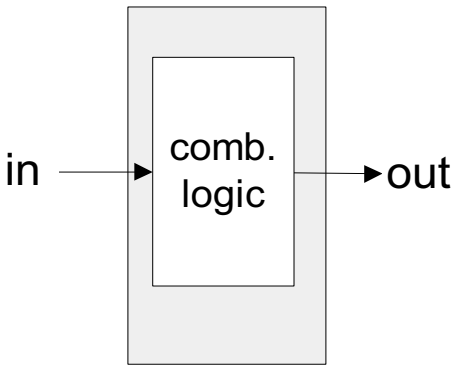
Program Counter - Diagram




```
If reset(t-1) then out(t)=0
   else if load(t-1) then out(t)=in(t-1)
        else if inc(t-1) then out(t)=out(t-1)+1
             else out(t)=out(t-1)
```

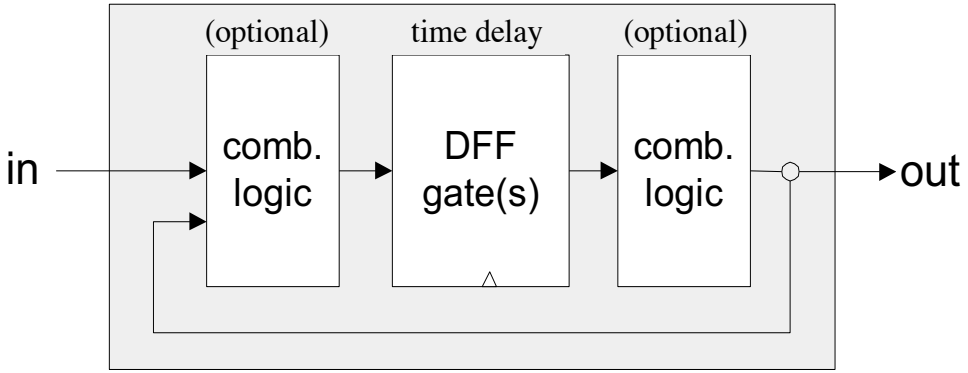
Sequential vs Combinational

Combinational chip

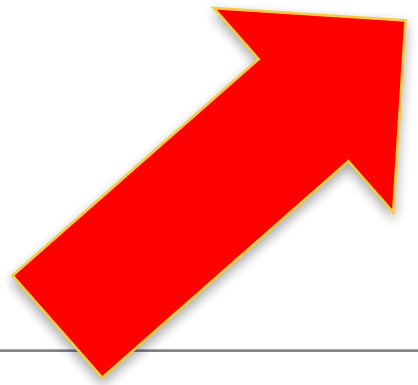


out = *some function of* (in)

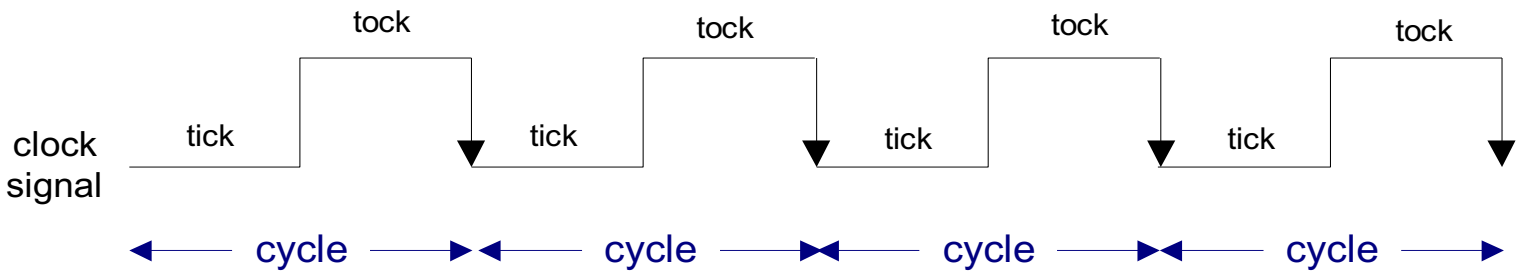
Sequential chip



out(t) = *some function of* (in(t-1), out(t-1))



Making clocks work



- During a tick-tock cycle, the internal states of all the clocked chips are allowed to change, but their outputs are "latched"
- At the beginning of the next cycle, the outputs of all the clocked chips in the architecture commit to the new values.
- What are the implications of this?

RAM Terminology

- What are:
  - SRAM?
  - DRAM?
  - Flash RAM?
- Do you know what caches are?

Lecture 5 worksheet question 3.

Hierarchy

- SRAM tends to be found in the cache, expensive but fast.
- DRAM often used for main memory, cheaper but slower.
- Longer term storage from this point on, cheapest of all but greatest access times.
- Caching and paging are still important areas of research!

Next lecture

- You should read “Chapter 4” of the textbook.
- Assignment 1 is due this week.
- Any questions? Ask on the forum or right now!