THE UNIVERSITY OF ADELAIDE
AUSTRALIA

COMPUTER NETWORKS AND APPLICATIONS

COMP SCI 3001

Faculty of Engineering, Computer and Mathematical Sciences

Data Link Layer

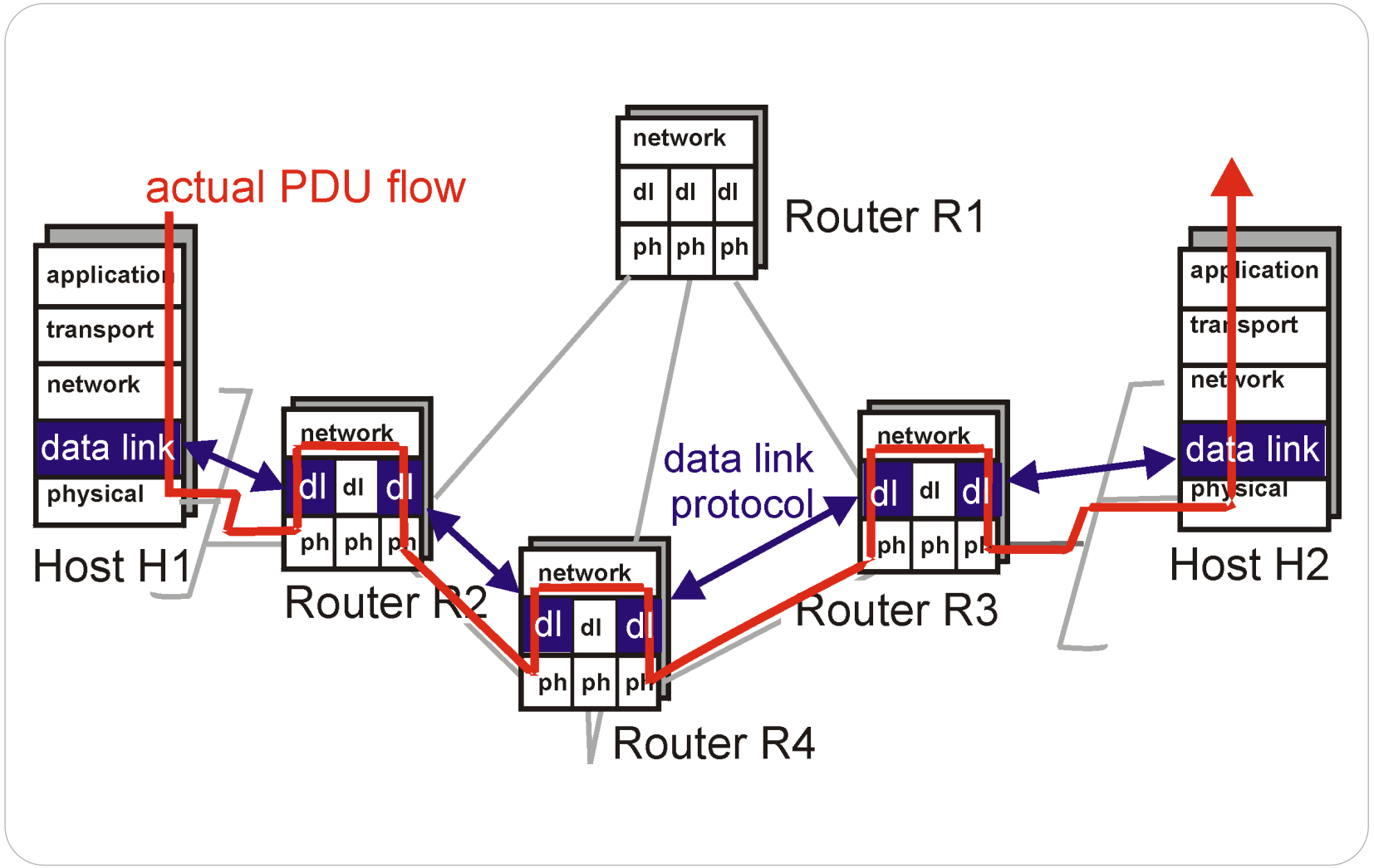
Data Link Layer introduction

Our goals

- Understand the principles behind Data Link Layer services
  - error detection, correction
  - sharing a broadcast channel: multiple access
  - link layer addressing
  - reliable data transfer, flow control: **done!**
- Instantiation and implementation of various link layer technologies

Data Link Layer introduction

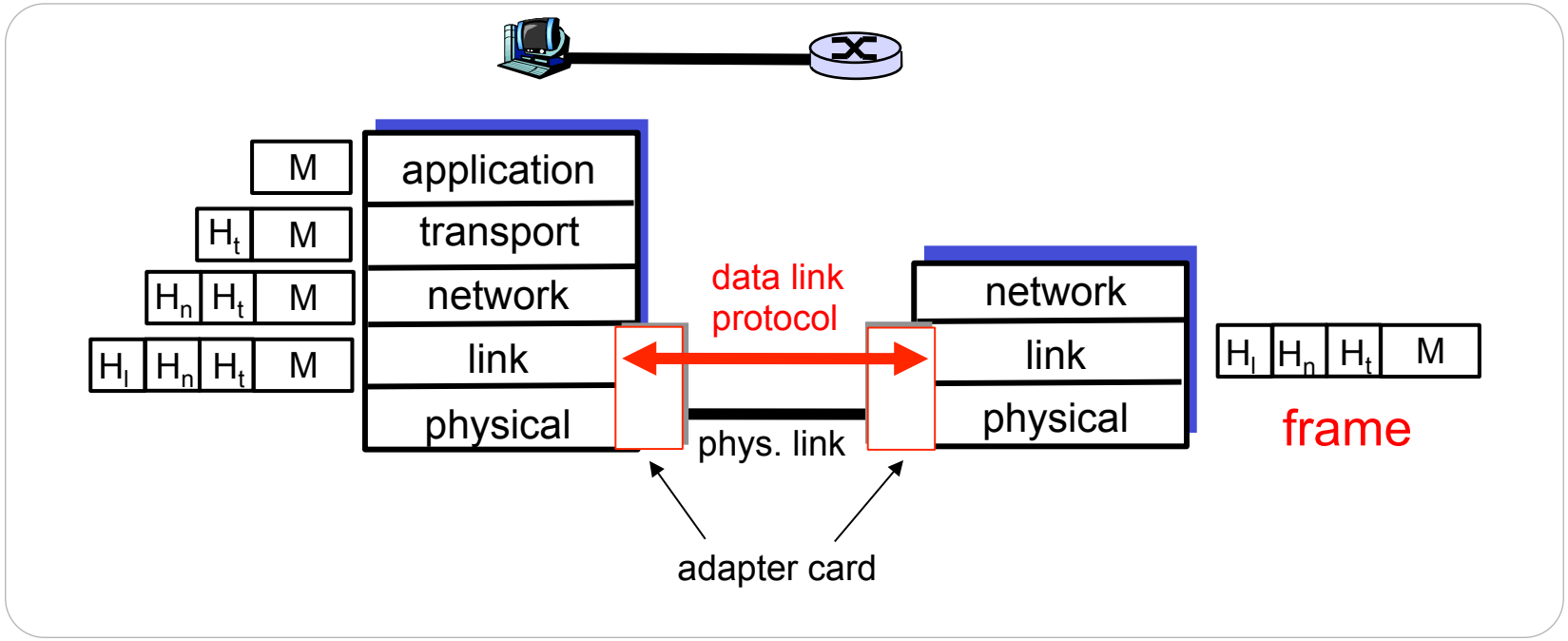
Context



Data Link Layer introduction

One link

- Two **physically connected** devices
  - host-router, router-router, host-host
- Unit of data: **frame**
- Implemented in ‘adapter’, eg PCMCIA card, Ethernet card
  - typically includes RAM, DSP chips, host bus interface and link interface



Link layer services

Framing, link access

- Encapsulate datagram into **frame**, adding header, trailer
- Implement channel access if shared medium
- 'Physical addresses' used in frame headers to identify source and destination
  - different from IP address!

Reliable delivery between two physically connected devices

- We learned how to do this already (remember TCP?)
- Seldom used on **low bit error** link (fiber, some twisted pair)
- Wireless links: high error rates
  - Q: why both link-level and end-end reliability?

Link layer services (cont.)

Flow control

- Pacing between sender and receiver(s)

Error detection

- Errors caused by signal attenuation and noise
  - every link **will** have errors
- Receiver detects presence of errors
  - signals sender for retransmission or drops frame

Error correction

- Receiver identifies **and corrects** bit error(s) without resorting to re-transmission
- Also called **Forward Error Control**

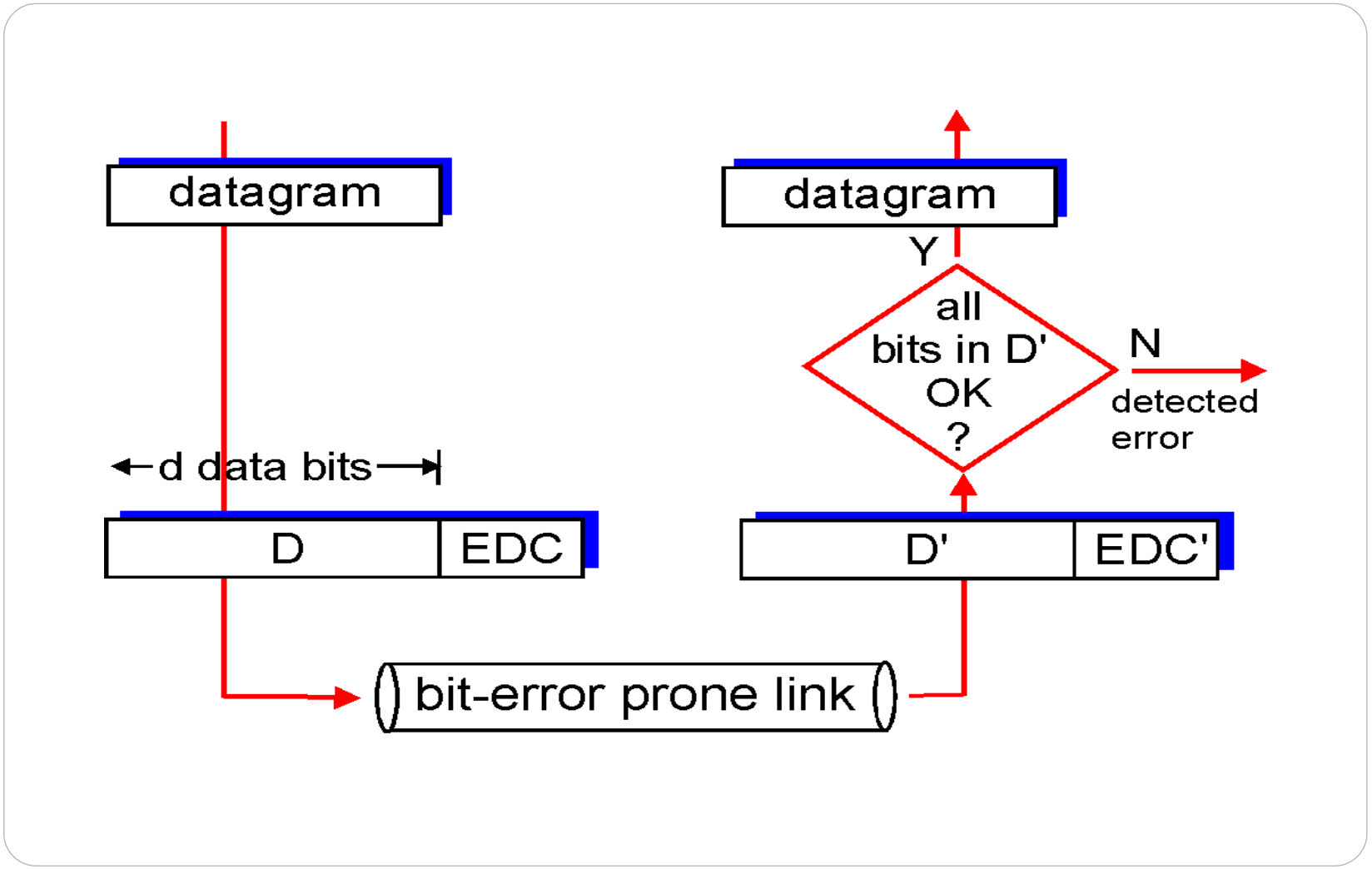
Error detection

EDC = Error Detection and Correction bits (redundancy)

D = Data protected by error checking, **may** include header fields

- Error detection not 100% reliable!
- **Protocol may miss some errors, but rarely**
- **Larger EDC field yields better detection and correction**

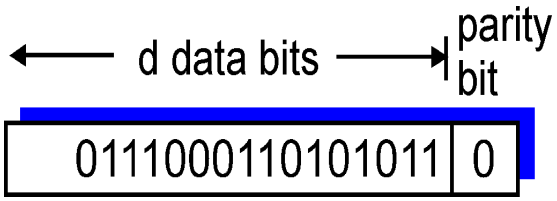
Error detection



Parity

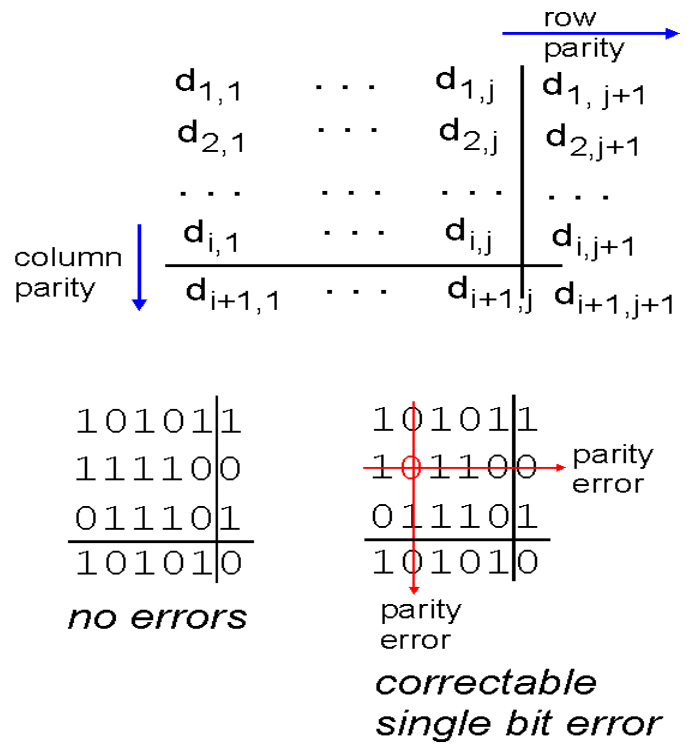
Single bit parity

Detect single bit errors



Two dimensional bit parity

Detect **and correct** single bit errors



Checksums

- Errors do **not usually occur as a one-off single bit error**
  - we normally have an error burst
  - burst length = k implies bit 0 and k are in error, but some of the others **might** be OK
- Checksums deal with multiple bit errors
  - already seen checksums (remember TCP?)
- Internet checksum is 1's complement sum of the segment contents (viewed as 16 bit numbers)
- General principle of checksums
  - sender computes checksum and sends it
  - receiver computes and compares

Checksums - CRCs

- Cyclic Redundancy Check polynomials
- View data bits, **D** as a binary number
- Choose r+1 bit pattern (generator), **G**
- **Goal:** choose r CRC bits, **R** such that
  - <D,R> exactly divisible by G (modulo 2)
  - receiver knows G and divides <D,R> by G
  - if non-zero remainder: error detected!
  - **can detect all burst errors less than r+1 bits**
- Widely used in practice (ATM, HDLC)