Michal Palič

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Education

Imperial College London — London, United Kingdom
MEng Electronics and Information Engineering — *October 2020 - June 2024 (Ongoing)*
Y1 average: 78.6%, Y2 average: 80.6%
Selected courses: *Discrete Mathematics (87%), Instruction architectures and Compilers (87%), Networks & Databases (83%), Programming for engineers (85%), Machine Learning (Pending), Advanced Computer Architecture(Pending)*

Gymnázium Jura Hronca — *Bratislava, Slovakia*
International Baccalaureate Diploma; Points: 41 — *September 2018 - May 2020*
Selected subjects(Grade): *Computer Science HL(7), Physics HL(7), Mathematics HL(6), Extended Essay (A)*

Relevant Experience

Undergraduate Research Opportunity, Imperial College

EEE Intelligent Digital Systems Lab

FpgaConvNet is a software suite written in **Python 3**, developed by the Intelligent Digital Systems Lab for the mapping of convolutional neural networks to FPGAs.

FpgaConvNet Demonstrator Development — *August 2022 - October 2022*

Contributed to the development of this tool-chain by addressing encountered bugs, improving stability and contributing extensive documentation. Collaborated with University of Strathclyde doctoral students to identify and demonstrate promising applications for the suite.

- **Mnist classifier development**: Specified and trained MNIST style classifier in **Keras**. Developed, benchmarked and evaluated a ZYNQ 7 SoC based demonstrator using the **Xilinx Vivado HLS** and **Xilinx Vivado** suites.
- **Modulation classifier development**: Identified promising application in RF modulation classification under multi-path fading. Reported or resolved encountered usability issues not previously considered by the core development team.

FpgaConvNet Optimiser Development — *July 2021 - October 2021*

- **Automated Design Space Exploration**: Analysed optimiser performance and addressed the identified deficiencies by researching and implementing new simulated annealing techniques such as periodic restarting and automated annealer parameter estimation. This resulted in an a 10x optimizer performance improvement for some workloads.

Imperial Formula Racing

Head of Electronics — *September 2021 - Present*

Is currently leading a critical 10 member section of a 100+ member inter-departmental project with the aim to deliver an Electric Vehicle to compete at Silverstone in the Formula Student UK 2023 competition.

- **Digital logic design**: Supervising, guiding and reviewing the the implementation of discrete digital logic and programmable safety systems in **C++** and **Arduino Due** hardware. Designs conform to detailed competition specification with a focus on fault tolerance.
- **PCB Design**: Collaborating with academic advisors to develop safe high and low voltage PCB designs in **Eagle**.

BratMUN 2019

Deputy Head — *November 2018 - November 2019*

- **Event Summary**: Organized Slovakia's forefront international Model United Nations conference consisting of over 150 students from 6 countries.
  - **Event Management**: Successfully organized, opened and moderated the opening ceremony hosted at a formal venue.
  - **Official communication**: Successfully invited foreign dignitaries as speakers.
  - **Event website development**: Led an IT team of 4 students to expand existing web infrastructure to handle the registration for the event.

Projects and Awards

Autonomous Mars Rover (Winner: Top Second Year Group Project) *June 2022*
Led development of a rover capable of autonomous navigation and mapping of simulated alien surface in a group of 7. Managed the project timeline through daily stand-up meetings, set targets and fostered compromises on module development time and direction between team members. Was responsible for the prototype of the video processing pipeline in **Python OpenCV** and its implementation in **SystemVerilog**. My key technical contributions included: A fast pipelined fixed point RGB to HSV converter, filtering/feature extraction using 2D convolution hardware and run-time pipeline reconfiguration using a NIOS II softcore CPU. meetings(GitHub)

MIPS C Compiler (Top 5 in cohort) *March 2022*
Developed a near fully featured ANSI **C** to MIPS compiler written in **C++** in a group of two. Supported features included integer, floating point , pointer, array, scope, function and type operations. Part of the Instruction Architectures and Compilers coursework. (GitHub)

Medusa IO *March 2022*
Developed an online multiplayer Snake inspired game with server, client, cloud database and FPGA elements in a group of 6. Was responsible for FPGA based accelerometer input and visual output processing in **SystemVerilog** using **Intel Quartus** and a **NIOS II** soft-core processor. My contributions included: The design and implementation of a FIR filtering accelerator and the corresponding filter. (GitHub)

MIPS I CPU (87%) *December 2021*
Led the development of a fully featured integer MIPS I CPU in groups of 6 using **SystemVerilog**. Was also responsible for correctness, functional block integration, Avalon-MM memory interfacing and Caching. Part of the Instruction Architectures and Compilers coursework. (GitHub)

NASA Space Apps Challenge (Top 2 in London, advanced to global judging) *October 2021*
Developed a JavaScript and Web GL based web app for the visualization of asteroid light curves though ray-tracing and rasterization. Created as part of a 48 hour hackathon in team of 4. (lumiro.cc)

Ray traced renderer *October 2021*
A self-driven project in **Python** with the aim of developing an understanding of physically accurate rendering techniques in preparation for the 2021 NASA Space Apps Challenge. (GitHub)

Design of ARM inspired CPU/FPU (Winner: Top First Year Group Project) *June 2021*
Developed and implemented a custom RISC CPU architecture in groups of 3. My contributions included: Integer and Floating point arithmetic hardware timing optimization, pipeline balancing, UART and interrupt hardware development. (GitHub)

Austrian Young Physicists' Tournament (1st place) *April 2019*
Represented Slovakia's National team. Developed a piece of original physical research, communicated and defended the results in front of jury and peers in the form of a 10 minute presentation and debate.

Skills Summary

Programming Languages: System Verilog, Python, C++, Bash

Tools: GIT, GitHub, Intel Quartus Prime, Xilinx Vivado, Keras, Autodesk Eagle

Platforms: Ubuntu, Windows, Arduino

Languages: Slovak (Native Proficiency), English (Bilingual proficiency), German (Limited Working Proficiency)

Academic Honors

- 2022 Dean's list (95th percentile) for academic performance in school year
- 2022 Head of Department's Prize for the top Second Year Group Project - Autonomous Mars Rover
- 2021 Dean's list (90th percentile) for academic performance in school year
- 2021 Head of Department's Prize for the top First Year Group Project - Design of ARM inspired CPU and FPU