SmartSCM™ Modem

V.90/K56flex™/V.34/V.32bis CX88168 Single Chip Modem with CX20463 SmartDAA™ and Optional CX20437 Voice Codec for Embedded Applications

Data Sheet

Conexant Proprietary Information

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Revision Record

Revision	Date	Comments
C	6/16/2000	Revision B release. Supersedes 100490B.
B	6/2/2000	Revision B release. Supersedes 100490A and 100491A.
A	1/26/2000	Initial release.

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1 INTRODUCTION

1.1 Overview

The Conexant™ SmartSCM™ V.90/K56flex Modem Device Set with SmartDAA technology supports analog data up to 56 kbps, analog fax to 14.4 kbps, telephone answering machine (TAM)/telephony extensions, voice/speakerphone (optional), GSM, analog cellular (optional), and parallel/serial host interface operation depending on model. Table 1-1 lists the available models.

The modem operates with PSTN telephone lines worldwide and supports optional direct connect to an AMPS analog cellular phone. The parallel host interface model also supports direct connect to a GSM phone.

Conexant's SmartDAA technology (patent pending) eliminates the need for a costly analog transformer, relays, and opto-isolators typically used in discrete DAA (Data Access Arrangement) implementations The SmartDAA architecture also simplifies product implementation by eliminating the need for country-specific board configurations enabling worldwide homologation of a single modem board design and a single bill of materials (BOM).

The SmartDAA system-powered DAA operates reliably without drawing power from the line, unlike line-powered DAAs which operate poorly when line current is insufficient due to long lines or poor line conditions. Enhanced features, such as monitoring of local extension status without going off-hook, are also supported.

Incorporating Conexant's proprietary Digital Isolation Barrier (DIB) design (patent pending) and other innovative DAA features, the SmartDAA architecture simplifies application design, minimizes layout area, and reduces component cost.

The SmartSCM device set, consisting of a CX88168 Single Chip Modem (SCM) in a 128-pin TQFP and a CX20463 SmartDAA™ Line Side Device (LSD) in a 32-pin TQFP, supports data/fax/TAM operation with hardware-based modem controller, digital signal processing, and DAA/telephone line interface functions (Figure 1-1 and Figure 1-2).

The SCM device integrates modem controller (MCU), modem data pump (MDP), 256k bytes ROM, 32k bytes RAM, and SmartDAA system side device (SSD) functions onto a single die.

Modem functions for both parallel and serial interface configurations operate using only internal memory with the exception of GSM which requires external memory. The external memory interface can also be used for customized modem code and added/modified country profiles.

Low profile, small TQFP packages and low voltage operation with low power consumption make this device set ideal for embedded and palmtop applications using parallel host or serial DTE interface.

The modem operates by executing firmware from internal ROM and RAM. Customized modem firmware can be executed from optional external memory, either from ROM/flash ROM or from serial EEPROM and RAM. GSM operation requires an external 1 Mbit (128k x 8) ROM/flash ROM.

In V.90/K56flex data mode (/56 models), the modem can receive data at line speeds up to 56 kbps from a digitally connected V.90 or K56flex-compatible central site modem. In this mode, the modem can transmit data at line speeds up to V.34 rates.

In V.34 data mode (/56 and /33 models), the modem operates at line speeds up to 33.6 kbps. When applicable, error correction (V.42/MNP 2-4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost average data throughput. Non-error-correcting mode is also supported.

In V.32 bis data mode, the modem operates at lines speeds up to 14.4 kbps.

In V.22 bis fast connect mode, the modem can connect at 2400 bps with a very short training time, which is very efficient for small data transfers.

Fax Group 3 send and receive rates are supported up to 14.4 kbps with T.30 protocol.

V.80 synchronous access mode supports host-controlled communication protocols, e. g., H.324 video conferencing.

In TAM mode, enhanced 2-bit or 4-bit per sample coding schemes at 8 kHz sample rate provide flexible format compatibility and allows efficient digital storage of voice/audio. Also supported are 8-bit linear and IMA 4-bit ADPCM coding. This mode supports applications such as digital telephone answering machine (TAM), voice annotation, and recording from and playback to the telephone line.

S models, using the optional CX20437 Voice Codec (VC) in a 32-pin TQFP, support position independent, full-duplex speakerphone (FDSP) operation using microphone and speaker, as well as other voice/TAM applications using handset or headset. S models can also support analog cellular operation with direct connection to an analog cellular phone (in lieu of a telephone handset/headset connection).

GSM operation supports data services offered by the Global System for Mobile Communications network: data transmissions to PSTN, ISDN or GSM users. GSM data operation allows data and fax transfer, and connection to videotex.

Analog cellular and GSM direct connect operation is supported by licensed firmware for specific phone types.

This data sheet describes the modem capabilities. Commands and parameters are defined in the Commands Reference Manual (Doc. No. 100722).

Table 1-1. SmartSCM Modem Models and Functions

Model/Order/Part Numbers					Supported Functions			
Marketing Name	**Device Set Order No.**	**Single Chip Modem (SCM) [128-Pin TQFP] Part No.**	**Line Side Device (LSD) [32-Pin TQFP] Part No.**	**Voice Codec (VC) [32-Pin TQFP] Part No.**	**V.90 and K56flex Data**	**V.34 Data**	**V.32 bis Data, V.17 Fax, TAM, Worldwide**	**Voice/FDSP, Analog Cellular**
EMBEDDED APPLICATIONS								
SmartSCM/56	DS56-L145-061	CX88168-11	20463-11	—	Y	Y	Y	—
SmartSCM/56S	DS56-L145-071	CX88168-11	20463-11	20437-11	Y	Y	Y	Y
SmartSCM/33	DS28-L189-061	CX88168-12	20463-11	—	—	Y	Y	—
SmartSCM/33S	DS28-L189-071	CX88168-12	20463-11	20437-11	—	Y	Y	Y
SmartSCM/14	DS96-L853-041	CX88168-13	20463-11	—	—	—	Y	—
SmartSCM/14S	DS96-L853-051	CX88168-13	20463-11	20437-11	—	—	Y	Y
AFTERMARKET APPLICATIONS								
SmartSCM/56	DS56-L144-121	CX88168-11	20463-11	—	Y	Y	Y	—
SmartSCM/56S	DS56-L144-131	CX88168-11	20463-11	20437-11	Y	Y	Y	Y

Notes:

1. Model options:
   - S — Voice/full-duplex speakerphone (FDSP) and analog cellular
   - 56 — 56 kbps max. rate per V.90
   - 33 — 33.6 kbps max. rate per V.34
   - 14 — 14.4 kbps max. rate per V.32 bis.
2. Supported functions (Y = Supported; – = Not supported).
   - TAM — Telephone answering machine (Voice playback and record through telephone line)
   - FDSP — Full-duplex speakerphone and voice playback and record through telephone line, handset, and mic/speaker
3. For ordering purposes, the CX prefix may not be included in the part number for some devices. Also, the CX prefix may not appear in the part number as branded on some devices.

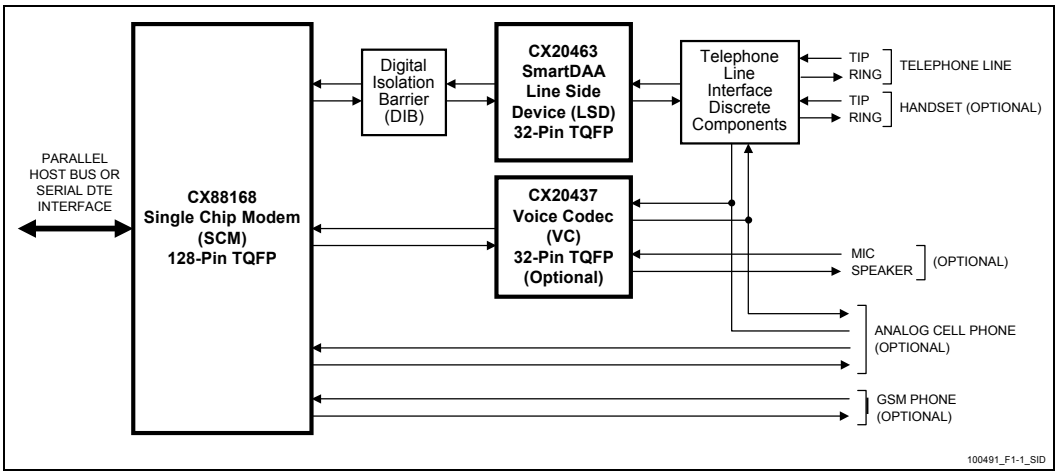

Figure 1-1. SmartSCM Modem Simplified Interface Diagram

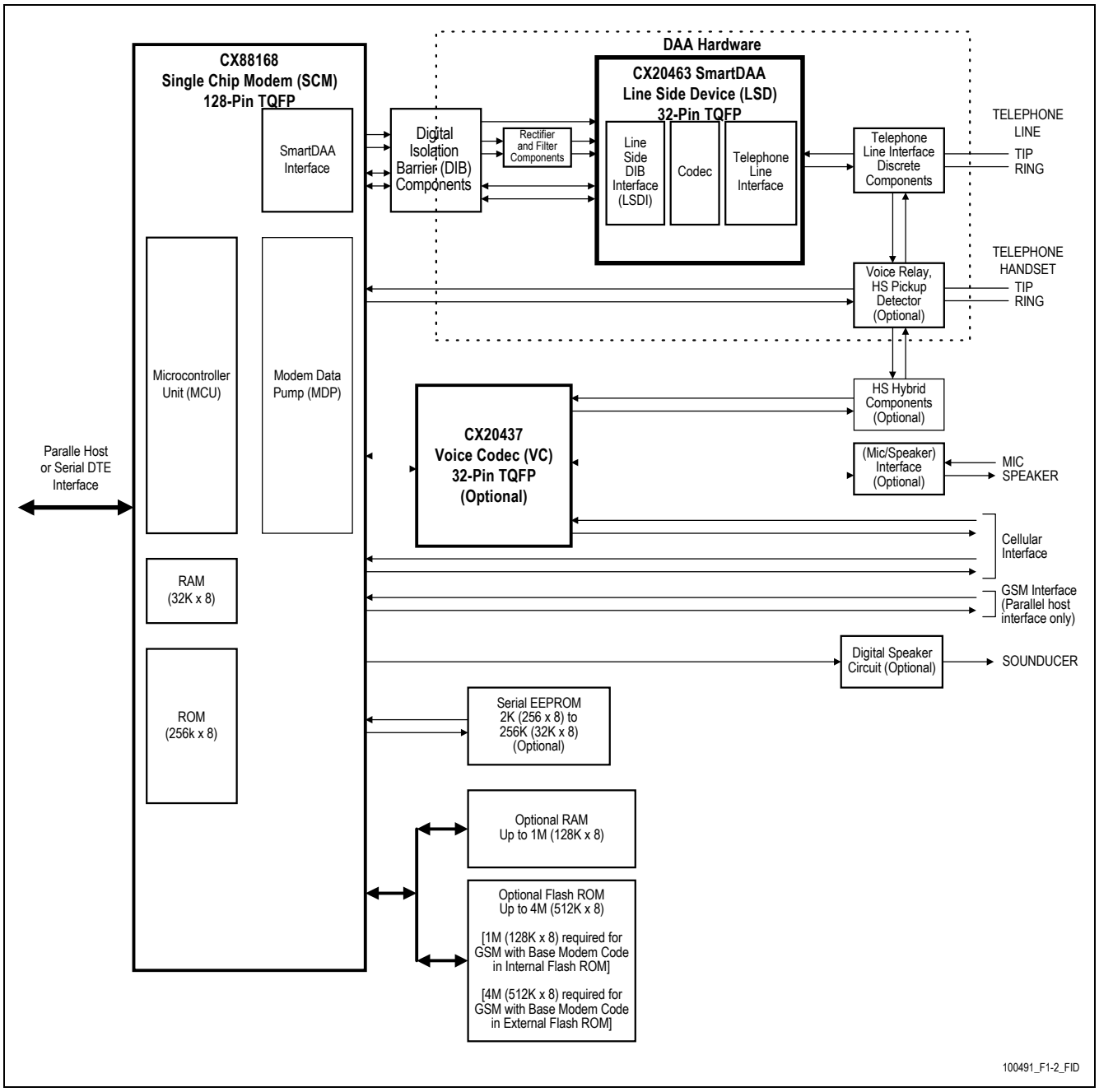

Figure 1-2. SmartSCM Modem Major Interfaces

1.2 Features

1.2.1 General Modem Features

- Data modem
  - ITU-T V.90/K56flex (/56 models)/V.34 (/56 and /33 models), V.32bis, V.32, V.22 bis, V.22, V.23, and V.21; Bell 212A and Bell 103
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - MNP 10EC™ enhanced cellular performance
  - V.250 and V.251 commands
- V.22 bis fast connect
- Analog cellular direct connect using optional CX20437 Voice Codec (S models)
- GSM cellular direct connect (parallel interface only)
- Fax modem send and receive rates up to 14.4 kbps
  - V.17, V.29, V.27 ter, and V.21 channel 2
  - EIA/TIA 578 Class 1 and T.31 Class 1.0, and EIA/TIA 578 Class 2 commands
- V.80 synchronous access mode supports host-controlled communication protocols with H.324 interface support
- Interfaces to optional external ROM/flash ROM and/or to optional external serial EEPROM and RAM for customized modem firmware
- Downloadable Architecture
  - Downloadable MCU firmware from the host/DTE to optional external flash ROM
  - Downloadable MDP code modules from the MCU transparent to the host
- Data/Fax/Voice call discrimination
- Hardware-based modem controller
- Hardware-based digital signal processor (DSP)
- Worldwide operation
  - Complies to TBR21 and other country requirements
  - Caller ID detection
  - Call progress, blacklisting
  - Internal ROM includes default values for 29 countries
- Caller ID and distinctive ring detect
- Telephony/TAM
  - V.253 commands
  - 2-bit and 4-bit Conexant ADPCM, 8-bit linear PCM, and 4-bit IMA coding
  - 8 kHz sample rate
  - Concurrent DTMF, ring, and Caller ID detection
- Full-duplex speakerphone (FDSP) mode using optional CX20437 Voice Codec (S models)
  - Microphone and speaker interface
  - Telephone handset or headset interface
  - Acoustic and line echo cancellation
  - Microphone gain and muting
  - Speaker volume control and muting
- Built-in host/DTE interface with speeds up to 230.4 kbps
  - Parallel 16550A UART-compatible interface
  - Serial ITU-T V.24 (EIA/TIA-232-E) logical interface
- Direct mode (serial DTE interface)
- Flow control and speed buffering
- Automatic format/speed sensing
- Serial async data; parallel async data
- Thin packages support low profile designs (1.6 mm max. height)
  - CX88168 SCM: 128-pin TQFP
  - CX20463 LSD: 32-pin TQFP
  - CX20437 VC: 32-pin TQFP
- +3.3V operation with +5V tolerant digital inputs
- Typical power use
  SCM and LSD: 470 mW (Normal Mode); 140 mW (Sleep Mode)
  VC: 5 mW (Normal Mode)

1.2.2 SmartDAA Features

- System side powered DAA operates under poor line current supply conditions
- Wake-on-ring
- Ring detection
- Line polarity reversal detection
- Line current loss detection
- Pulse dialing
- Line-in-use detection – detects even while on-hook
- Remote hang-up detect – for efficient call termination
- Extension pickup detect
- Call waiting detection
- Digital PBX line protection
- Meets worldwide DC VI Masks requirements

1.2.3 Applications

- Handheld computers
- Gaming devices
- Point of sales terminals
- Remote monitoring and data collection systems

1.3 Technical Overview

1.3.1 General Description

Modem operation, including dialing, call progress, telephone line interface, telephone handset interface, optional voice/speakerphone interface, optional analog cellular phone interface, GSM interface, and host interface functions are supported and controlled through the V.250, V.251, and V.253-compatible command set.

The modem hardware connects to the host via a parallel or serial interface as selected by the PARIF input. The OEM adds a crystal circuit, DIB components, telephone line interface, telephone handset/telephony extension interface, voice/speakerphone interface, cellular interface, GSM interface, optional external serial EEPROM, optional external ROM/flash ROM, optional external RAM, and other supporting discrete components as supported by the modem model (Table 1-1) and required by the application to complete the system.

Customized modem firmware can be supported by the use of external memory in various combinations, e.g., either external ROM/flash ROM (up to 256k bytes), or external serial EEPROM (256 to 32k bytes) and external RAM (up to 128k bytes). To support country profile addition or modification, external serial EEPROM (256 to 32k bytes) can be installed. Customized code can include OEM-defined commands, i.e., identification codes (I3), identifier string (I4), manufacturer identification (+GMI), model identification (+GMM), and revision identification (+GMR), as well as code modification.

Parallel interface operation is selected by PARIF input high. Telephone line, cellular (AMPS) phone, or GSM phone interface operation is selected by the LINE/CELL and LINE/GSM inputs. Installation of cellular phone driver is also required for cellular phone interface operation. Installation of GSM firmware is also required for GSM phone interface operation.

Serial interface operation is selected by PARIF input low. Telephone line or cellular (AMPS) phone interface operation is selected by the LINE/CELL input. Installation of cellular phone driver is also required for cellular phone interface operation.

1.3.2 MCU Firmware

MCU firmware performs processing of general modem control, command sets, data modem, error correction and data compression (ECC), fax class 1, fax class 1.0, fax class 2, voice/audio/TAM/speakerphone, worldwide, V.80, and serial DTE/parallel host interface functions according to modem models (Table 1-1).

MCU firmware can be customized to include OEM-defined commands, i.e., identification codes (I3), identifier string (I4), manufacturer identification (+GMI), model identification (+GMM), and revision identification (+GMR), as well as code modification.

1.3.3 Operating Modes

Data/Fax Modes

In V.90/K56flex data modem mode (/56 models), the modem can receive data from a digital source using a V.90- or K56flex-compatible central site modem at line speeds up to 56 kbps. Asymmetrical data transmission supports sending data at line speeds up to V.34 rates. This mode can fallback to full-duplex V.34 mode and to lower rates as dictated by line conditions.

In V.34 data modem mode (/56 and /33 models), the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33.6 kbps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps down to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standards are supported.

In V.32 bis data modem mode, the modem can operate at line speeds up to 14.4 kbps.

In V.22 bis fast connect data mode, the modem can connect at 2400 bps with a very short training time, which is very efficient for small data transfers.

In fax modem mode, the modem can operate in 2-wire, half-duplex, synchronous modes and can support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax data transmission and reception performed by the modem are controlled and monitored through the EIA/TIA-578 Fax Class 1, T.31 Fax Class 1.0, or Fax Class 2 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

Synchronous Access Mode (SAM) - Video Conferencing

V.80 Synchronous Access Mode between the modem and the host/DTE is provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

Worldwide Operation

The modem operates in TBR21-compliant and other countries. Country-dependent modem parameters for functions such as dialing, carrier transmit level, calling tone, call progress tone detection, answer tone detection, blacklisting, caller ID, and relay control are programmable (see Section 2.13).

SmartDAA technology allows a single PCB design and single BOM to be homologated worldwide. Advanced features such as extension pickup detection, remote hang-up detection, line-in-use detection, and digital PBX detection are supported.

Country code IDs are defined by ITU-T T.35.

Internal ROM includes default profiles for 29 countries including TBR21-compliant profiles. These profiles can be overridden by modified values stored in external serial EEPROM. If optional external ROM/flash ROM is used, a maximum of 31 country profiles can be stored in external ROM/flash ROM. Additional country profiles can also be stored in external serial EEPROM (request additional country profiles from a Conexant Sales Office). The default countries supported are:

Country	Country Code	Country	Country Code	Country	Country Code
Australia	09	India	53	Portugal	8B
Austria	0A	Ireland	57	Singapore	9C
Belgium	0F	Italy	59	South Africa	9F
Brazil	16	Japan	00	Spain	A0
China	26	Korea	61	Sweden	A5
Denmark	31	Malaysia	6C	Switzerland	A6
Finland	3C	Mexico	73	Taiwan	FE
France	3D	Netherlands	7B	United Kingdom	B4
Germany	42	Norway	82	United States	B5
Greece	46	Poland	8A		

TAM Mode

TAM Mode features include 8-bit linear coding at 8 kHz sample rate. Tone detection/generation, call discrimination, and concurrent DTMF detection are also supported. ADPCM (4-bit IMA) coding is also supported to meet Microsoft WHQL logo requirements.

TAM Mode is supported by three submodes:

1. Online Voice Command Mode supports connection to the telephone line or, for S models, a microphone/speaker/handset/headset.
2. Voice Receive Mode supports recording voice or audio data input from the telephone line or, for S models, a microphone/handset/headset.
3. Voice Transmit Mode supports playback of voice or audio data to the telephone line or, for S models, a speaker/handset/headset.

Voice/Speakerphone Mode (S Models)

S models include additional telephone handset, external microphone, and external speaker interfaces which support voice and full-duplex speakerphone (FDSP) operation.

Hands-free full-duplex telephone operation is supported in Speakerphone Mode under host control. Speakerphone Mode features an advanced proprietary speakerphone algorithm which supports full-duplex voice conversation with acoustic, line, and handset echo cancellation. Parameters are constantly adjusted to maintain stability with automatic fallback from full-duplex to pseudo-duplex operation. The speakerphone algorithm allows position independent placement of microphone and speaker. The host can separately control volume, muting, and AGC in microphone and speaker channels.

1.3.4 Reference Design

A data/fax/TAM/speakerphone reference design for an external modem (RD00-D970) is available to minimize application design time, reduce development cost, and accelerate market entry.

A design package is available in electronic form. This package includes schematics, bill of materials (BOM), vendor part list (VPL), board layout files in Gerber format, and complete documentation.

1.3.5 GSM (Parallel Host Interface)

Supported GSM features include:

- Data modem
  - V.21, V.23, V.22, V.22 bis, V.32
  - ISDN interoperability: 300 bps to 9600 bps
- Transparent asynchronous mode up to 9600 bps
- Non-transparent mode (RLP) up to 9600 bps
- Fax modem send and receive rate up to 9600 bps
- AT GSM commands (ETSI 07.07)
- GSM direct connect
- Firmware interface for OEM-provided phone driver
- Automatic GSM cable presence detection
- Built-in parallel host (16550A UART) interface

GSM operation requires an external 1 Mbit (128k x 8) ROM/flash ROM. If optional external ROM/flash ROM is used for the base modem code, GSM operation requires 1 Mbit of an the external 4 Mbits (512k x 8) ROM/flash ROM.

1.4 Hardware Description

SmartDAA™ technology (patent pending) eliminates the need for a costly analog transformer, relays, and opto-isolators that are typically used in discrete DAA implementations. The programmable SmartDAA architecture simplifies product implementation in worldwide markets by eliminating the need for country-specific components.

1.4.1 CX88168 Single Chip Modem

The CX88168 Single Chip Modem (SCM), packaged in a 128-pin TQFP, includes a Microcontroller (MCU), a Modem Data Pump (MDP), 256k bytes internal ROM, 32k bytes internal RAM, and SmartDAA interface functions.

The SCM connects to host via a parallel host (PARIF = high) or a logical V.24 (EIA/TIA-232-E) serial DTE interface (PARIF = low).

The SCM performs the command processing and host interface functions. The crystal frequency is 28.224 MHz.

The SCM optionally connects to external OEM-supplied ROM/flash ROM and RAM over a non-multiplexed 19-bit address bus and 8-bit data bus. GSM operation requires external 1M (128k x 8) ROM/flash ROM.

The SCM optionally connects to an external OEM-supplied serial EEPROM over a dedicated 2-line serial interface. The capacity of the EEPROM can be 256 bytes up to 32k bytes. The EEPROM can hold information such as firmware configuration customization, country code parameters, and cellular drivers.

The SCM performs telephone line signal modulation/demodulation in a hardware digital signal processor (DSP) which reduces computational load on the host processor.

The SmartDAA Interface communicates with, and supplies power and clock to, the LSD through the DIB.

1.4.2 Digital Isolation Barrier

The OEM-supplied Digital Isolation Barrier (DIB) electrically DC isolates the SCM from the LSD and telephone line. The SCM is connected to a fixed digital ground and operates with standard CMOS logic levels. The LSD is connected to a floating ground and can tolerate high voltage input (compatible with telephone line and typical surge requirements).

The DIB transformer couples power and clock from the SCM to the LSD.

The DIB data channel supports bidirectional half-duplex serial transfer of data, control, and status information between the SCM and the LSD over two lines.

1.4.3 CX20463 SmartDAA Line Side Device

The CX20463 SmartDAA Line Side Device (LSD) includes a Line Side DIB Interface (LSDI), a coder/decoder (codec), and a Telephone Line Interface (TLI).

The LSDI communicates with, and receives power and clock from, the SmartDAA interface in the SCM through the DIB.

LSD power is received from the MDP PWRCLKP and PWRCLKN pins via the DIB through a half-wave rectifying diode and capacitive power filter circuit connected to the DIB transformer secondary winding.

The CLK input is also accepted from the DIB transformer secondary winding through a capacitor and a resistor in series.

Information is transferred between the LSD and the SCM through the DIB_P and DIB_N pins. These pins connect to the SCM DIB_DATAP and DIB_DATAN pins, respectively, through the DIB.

The TLI integrates DAA and direct telephone line interface functions and connects directly to the line TIP and RING pins, as well as to external line protection components.

Direct LSD connection to TIP and RING allows real-time measurement of telephone line parameters, such as the telephone central office (CO) battery voltage, individual telephone line (copper wire) resistance, and allows dynamic regulation of the off-hook TIP and RING voltage and total current drawn from the central office (CO). This allows the modem to maintain compliance with U.S. and worldwide regulations and to actively control the DAA power dissipation.

1.4.4 CX20437 Voice Codec

The optional CX20437 Voice Codec (VC), packaged in a 32-pin TQFP, supports voice/full-duplex speakerphone (FDSP) operation with interfaces to a microphone and speaker and to a telephone handset/headset. The VC also supports and analog cellular operation with direct connect interface to a cellular phone (in lieu of telephone handset/headset connection).

1.5 Commands

The modem supports data modem, fax class 1 modem, fax class 1.0 modem, fax class 2 modem, voice/audio, full-duplex speakerphone (FDSP), MNP 10/MNP 10EC, and V.80 commands, and S Registers in accordance with modem model options. See Doc. No. 100722 for a description of the commands.

Data Modem Operation. Data modem functions operate in response to the AT commands when +FCLASS=0. Default parameters support U.S./Canada operation.

MNP 10 Operation. MNP 10 functions operate in response to MNP 10 commands.

MNP 10EC Operation. MNP 10EC is enabled by the -SEC=1 command.

Fax Modem Operation. Facsimile functions operate in response to fax class 1 commands when +FCLASS=1, fax class 1.0 commands when +FCLASS=1.0, or to fax class 2 commands when +FCLASS=2 is installed.

Voice/Audio Operation. Voice/audio mode functions operate in response to voice/audio commands when +FCLASS=8.

Speakerphone Operation. FDSP functions operate in response to speakerphone commands when +FCLASS=8 and +VSP=1 is selected.

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2 TECHNICAL SPECIFICATIONS

2.1 Serial DTE Interface Operation

2.1.1 Automatic Speed/Format Sensing

Command Mode and Data Modem Mode. The modem can automatically determine the speed and format of the data sent from the DTE. The modem can sense speeds of 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 16800, 19200, 21600, 24000, 26400, 28800, 38400, 57600, 115200, and 230400 bps and the following data formats:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	7	2	10
Odd	7	1	10
Even	7	1	10
None	8	1	10
Odd	8	1	11*
Even	8	1	11*
*11-bit characters are sensed, but the parity bits are stripped off during data transmission in Normal and Error Correction modes.			

The modem can speed sense data with mark or space parity and configures itself as follows:

DTE Configuration	Modem Configuration
7 mark	7 none
7 space	8 none
8 mark	8 none
8 space	8 even

Fax Modem Mode. In V.17 fax mode, the modem can sense speeds up to 230.4 kbps.

2.2 Parallel Host Bus Interface Operation

Command Mode and Data Modem Mode. The modem can operate at rates up to 230.4 kbps by programming the Divisor Latch in the parallel interface registers if supported by communications software and/or driver (a Windows 95/98 driver is available from Conexant).

Fax Modem Mode. In V.17 mode, the modem can operate at rates up to 230.4 kbps by programming the Divisor Latch in the parallel interface registers if supported by communications software and/or driver (a Windows 95/98 driver is available from Conexant).

2.3 Establishing Data Modem Connections

Telephone Number Directory

The modem supports four telephone number entries in a directory that can be saved in a serial NVRAM. Each telephone number can be up to 32 characters (including the command line terminating carriage return) in length. A telephone number can be saved using the &Zn=x command, and a saved telephone number can be dialed using the DS=n command.

Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with ITU-T Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

Call Progress Tone Detection

Ringback, equipment busy, congested tone, warble tone, and progress tones can be detected in accordance with the applicable standard.

Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in ITU-T modes and 2225 ± 40 Hz in Bell modes.

Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to allow transmission of the billing tone signal.

Connection Speeds

The modem functions as a data modem when the +FCLASS=0 command is active.

Line connection can be selected using the +MS command. The +MS command selects modulation, enables/disables automode, and selects minimum and maximum line speeds (Table 2-1).

Automode

Automode detection can be enabled by the +MS command to allow the modem to connect to a remote modem in accordance with draft PN-3320 for V.34 (Table 2-1).

Table 2-1. +MS Command Automode Connectivity

<mod>	Modulation	Possible Rates (bps) [1]	Notes
V21	V.21	300	
V22	V.22	1200	
V22B	V.22 bis	2400 or 1200	
V23	V.23	1200	See Note 2
V32	V.32	9600 or 4800	
V32B	V.32 bis	14400, 12000, 9600, 7200, or 4800	Default for /14 models
V34	V.34	33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, or 2400	Default for /33 models
V90	V.90	56000, 54667, 53333, 52000, 50667, 49333, 48000, 46667, 45333, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000	Default for /56 models
K56	K56flex	56000, 54000, 52000, 50000, 48000, 46000, 44000, 42000, 40000, 38000, 36000, 34000, 32000	
B103	Bell 103	300	
B212	Bell 212	1200	

Notes:

1. See optional <automode>, <min_rate>, and <max_rate> subparameters for the +MS command.
2. For V.23, originating modes transmit at 75 bps and receive at 1200 bps; answering modes transmit at 1200 bps and receive at 75 bps. The rate is always specified as 1200 bps. V.23 half duplex is not supported.
3. If the DTE speed is set to less than the maximum supported DCE speed in automode, the maximum connection speed is limited to the DTE speed.

2.4 Data Mode

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

Flow Control

DTE-to-Modem Flow Control. If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

Escape Sequence Detection

The +++ escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 Register value greater than 127.

BREAK Detection

The modem can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modem response to a received BREAK signal.

Telephone Line Monitoring

GSTN Cleardown (V.90, K56flex, V.34, V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Loss of Carrier (V.22 bis and Below). If carrier is lost for a time greater than specified by the S10 register, the modem disconnects (except MNP 10).

Receive Space Disconnect (V.22 bis and Below). If selected by the Y1 command in non-error-correction mode, the modem disconnects after receiving 1.6 ± 10% seconds of continuous SPACE.

Send SPACE on Disconnect (V.22 bis and Below)

If selected by the Y1 command in non-error-correction mode, the modem sends 4 ± 10% seconds of continuous SPACE when a locally commanded hang-up is issued by the &Dn or H command.

Fall Forward/Fallback (V.90/K56flex/V.34/V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.90/K56flex/V.34/V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the +MS or N1 command.

When connected in V.90/K56flex/V.34/V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the current modulation depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

Retrain

The modem may lose synchronization with the received line signal under poor or changing line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

Programmable Inactivity Timer

The modem disconnects from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 255 seconds by using register S30. A value of 0 disables the inactivity timer.

DTE Signal Monitoring (Serial DTE Interface Only)

DTR#. When DTR# is asserted, the modem responds in accordance with the &Dn and &Qn commands.

RTS#. RTS# is used for flow control if enabled by the &K command in normal or error-correction mode.

2.5 Error Correction and Data Compression

V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn command or S46 register, operates when a LAPM or MNP 10 connection is established.

The V.42 bis data compression employs a “string learning” algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2k-byte dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

2.6 MNP 10 Data Throughput Enhancement

MNP 10 protocol and MNP Extended Services enhance performance under adverse channel conditions such as those found in rural, long distance, or cellular environments. An MNP 10 connection is established when an MNP 2-4 connection is negotiated with a remote modem supporting MNP 10.

MNP Extended Services. The modem can quickly switch to MNP 10 operation when the remote modem supports MNP 10 and both modems are configured to operate in V.42.

V.42 bis/MNP 5 Support. V.42 bis/MNP 10 can operate with V.42 bis or MNP 5 data compression.

2.7 MNP 10EC™ Enhanced Cellular Connection

A traditional landline modem, when used for high-speed cellular data transmission, typically encounters frequent signal interference and degradation in the connection due to the characteristics of the analog cellular network. In this case, cellular-specific network impairments, such as non-linear distortion, fading, hand-offs, and high signal-to-noise ratio, contribute to an unreliable connection and lower data transfer performance. Implementations relying solely on protocol layer methods, such as MNP 10, generally cannot compensate for the landline modem's degraded cellular channel performance.

The modem achieves higher cellular performance by implementing enhanced cellular connection techniques at both the physical and protocol layers, depending on modem model. The modem enhances the physical layer within the modulation by optimizing its responses to sudden changes in the cellular connection. The MNP 10EC protocol layer implemented in the modem firmware improves data error identification/correction and maximizes data throughput by dynamically adjusting speed and packet size based on signal quality and data error performance.

2.8 Telephony Extensions

The following telephony extension features are supported and can be typically be implemented in designs for set-top box applications and TAM software applications to enhance end-user experience:

- Line In Use detection
- Extension Pickup detection
- Remote Hang-up detection

2.8.1 Line In Use Detection

The Line In Use Detection feature can stop the modem from disturbing the phone line when the line is already being used. When an automated system tries to dial using ATDT and the phone line is in use, the modem will not go off hook and will respond with the message “LINE IN USE”.

2.8.2 Extension Pickup Detection

The Extension Pickup Detection feature (also commonly referred as PPD or Parallel phone detection) allows the modem to detect when another telephony device (i.e., fax machine, phone, satellite/cable box) is attempting to use the phone line.

This feature can be used to quickly drop a modem connection in the event when a user picks up a extension phone line. For example, this feature allows set top boxes with an integrated SmartSCM modem to give normal voice users the highest priority over the telephone line.

This feature can also be used in Telephone Answering Machine applications (TAM). Its main use would be to stop the TAM operation when a phone is picked up.

2.8.3 Remote Hangup Detection

The Remote Hangup Detection feature will cause the modem go back onhook during a data connection when the remote modem is disconnected for abnormal termination reasons (remote phone line unplugged, remote server/modem shutdown. For Voice applications, this method can be used in addition to silence detection to determine when a remote caller has hung up to terminate a voice recording.

2.9 Fax Class 1, Fax Class 1.0, and Fax Class 2 Operation

Facsimile functions operate in response to fax class 1 commands when +FCLASS=1, fax class 1.0 commands when +FCLASS=1.0, or to fax class 2 commands when +FCLASS=2 is installed

In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Some AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

2.10 Voice/Audio Mode

Voice and audio functions are supported by the Voice Mode. Voice Mode includes three submodes: Online Voice Command Mode, Voice Receive Mode, and Voice Transmit Mode.

2.10.1 Online Voice Command Mode

This mode results from the connection to the telephone line or a voice/audio I/O device (e.g., microphone, speaker, or handset) through the use of the +FCLASS=8 and +VLS commands. After mode entry, AT commands can be entered without aborting the connection.

2.10.2 Voice Receive Mode

This mode is entered when the +VRX command is active in order to record voice or audio data input at the RIN pin, typically from a microphone/handset or the telephone line.

Received analog voice samples are converted to digital form and compressed for reading by the host. AT commands control the codec bits-per-sample rate.

Received analog mono audio samples are converted to digital form and formatted into 8-bit unsigned linear PCM format for reading by the host. AT commands control the bit length and sampling rate. Concurrent DTMF/tone detection is available at the 8 kHz sample rate.

2.10.3 Voice Transmit Mode

This mode is entered when the +VTX command is active in order to playback voice or audio data to the TXA output, typically to a speaker/handset or to the telephone line.

Digitized voice data is decompressed and converted to analog form at the original compression quantization sample-per-bits rate then output to the TXA output.

Digitized audio data is converted to analog form then output to the TXA output.

2.10.4 Audio Mode

The audio mode enables the host to transmit and receive 8-bit audio signals. In this mode, the modem directly accesses the internal analog-to-digital (A/D) converter (ADC) and the digital-to-analog (D/A) converter (DAC). Incoming analog audio signals can then be converted to digital format and digital signals can be converted to analog audio output.

2.10.5 Tone Detectors

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the configuration status. In Tone Mode, all three tone detectors are operational.

2.10.6 Speakerphone Modes

Speakerphone modes are controlled in voice mode with the following commands:

Use Speakerphone After Dialing or Answering (+VSP=1). +VSP=1 selects speakerphone mode while in +FCLASS=8 mode. Speakerphone operation is entered during Voice Online Command mode after completing dialing or answering.

Speakerphone Settings. The +VGM and +VGS commands can be used to control the microphone gain and speaker volume, respectively. The VGM and +VGS commands are valid only after the modem has entered the Voice Online mode while in the +VSP=1 setting.

2.11 Full-Duplex Speakerphone (FDSP) Mode (S Models)

The modem operates in FDSP mode when +FCLASS=8 and +VSP=1 (see Section 2.10.6).

In FDSP Mode, speech from a microphone or handset is converted to digital form, shaped, and output to the telephone line through the line interface circuit. Speech received from the telephone line is shaped, converted to analog form, and output to the speaker or handset. Shaping includes both acoustic and line echo cancellation.

2.12 Caller ID

Caller ID can be enabled/disabled using the +VCID command. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

2.13 Worldwide Country Support

Internal modem firmware supports 29 country profiles (see Section 1.3.2). These country profiles include the following country-dependent parameters:

- Dial tone detection levels and frequency ranges.
- DTMF dialing parameters: Transmit output level, DTMF signal duration, and DTMF interdigit interval.
- Pulse dialing parameters: Make/break times, set/clear times, and dial codes are programmable
- Ring detection frequency range.
- Blind dialing enabled/disable.
- Carrier transmit level (through S91 for data and S92 for fax). The maximum, minimum, and default values can be defined to match specific country and DAA requirements.
- Calling tone is generated in accordance with V.25. Calling tone may be toggled (enabled/disabled) by inclusion of a "^" character in a dial string. It may also be disabled.
- Frequency and cadence of tones for busy, ringback, congested, warble, dial tone 1, and dial tone 2.
- Answer tone detection period.
- Blacklist parameters. The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted").

These country profiles may be altered or customized by modifying the country-dependent parameters. Additional profiles may also be included. There are two ways to add or modify profiles:

- Linking additional or modified profiles from an external serial EEPROM.
- Incorporating additional or modified profiles into optional external flash ROM containing the entire modem firmware code.

Please contact an FAE at the local Conexant sales office if a country code customization is required.

2.14 Diagnostics

2.14.1 Commanded Tests

Diagnostics are performed in response to &T commands.

Analog Loopback (&T1 Command). Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

2.14.2 Power On Reset Tests

Upon power on, the modem performs tests of the modem, internal and external RAM, and NVRAM. If the modem, internal RAM, or external RAM test fails, the TMIND# output is pulsed (serial interface version) or the DCD bit in the parallel interface register is pulsed (parallel interface version) as follows:

Internal or external RAM test fails: One pulse cycle (pulse cycle = 0.5 sec. on, 0.5 sec. off) every 1.5 seconds.

Modem device test fails: Three pulse cycles every 1.5 seconds.

If the NVRAM test fails (due to NVRAM failure or if NVRAM is not installed), the test failure is reported by AT commands that normally use the NVRAM, e.g., the &V command.

2.15 Low Power Sleep Mode

Sleep Mode Entry. The modem enters the low power sleep mode when no line connection exists and no host activity occurs for the period of time specified in the S24 register. All modem circuits are turned off except the internal clock circuitry in order to consume reduced power while being able to immediately wake up and resume normal operation.

Wake-up. Wake-up occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface), or the DTE sends a character to the modem (serial interface).

2.16 GSM Operation

Once the modem is connected to the GSM phone and the phone is powered on, dial/answer functions will be routed through the phone instead of the wireline DAA. No special commands are needed to place or answer GSM calls and the same AT commands and software packages that are used for wireline communication sessions can be used.

While the modem is being used with a GSM phone, result messages are changed from wireline operation status to reflect GSM operation status as follows:

NO DIALTONE - Indicates that GSM service is not currently available or the cellular phone is powered off.

RING - Indicates that the GSM phone is receiving an incoming call.

BUSY - The network reports the number dialed is busy.

CARRIER - The carrier is established with the IWF (Interworking function) modem.

PROTOCOL RLP - The error corrected protocol on the radio link is established.

3 HARDWARE INTERFACE

3.1 CX88168 SCM Hardware Pins and Signals

3.1.1 Common to Parallel and Serial Interface Configurations

LSD Interface (Through DIB)

The DIB interface signals are:

- Clock and Power Positive (PWRCLKP); output
- Clock and Power Negative (PWRCLKN); output
- Data Positive (DIB_DATAP); input/output
- Data Negative (DIB_DATAN); input/output

Call Progress Speaker Interface

The call progress speaker interface signal is:

- Digital speaker output (DSPKOUT); output

DSPKOUT is a square wave output in Data/Fax mode used for call progress or carrier monitoring. This output can be optionally connected to a low-cost on-board speaker, e.g., a sounducer, or to an analog speaker circuit.

Voice Relay Interface (S Models)

The voice relay interface signal is:

- Voice Relay Control (VOICE#); output

Serial EEPROM Interface

A 2-line serial interface to an optional serial EEPROM is supported. The interface signals are:

- Bidirectional Data input/output (NVMDATA)
- Clock output (NVMCLK)

The EEPROM can hold information such as firmware customization, country code parameters, and cellular drivers. Data stored in EEPROM takes precedence over the factory default settings.

The EEPROM size can range from 2 kbits (256 x 8) to 256 kbits (32k x 8). A 2k EEPROM must be 100 kHz or 400 kHz; higher capacity EEPROMs must be 400 kHz.

External Bus Interface

The external bus can connect to optional OEM-supplied external memory:

- Up to 4 Mbits (512k x 8) ROM/flash ROM (1 Mbit is required for optional GSM)
- Up to 1 Mbit (128k x 8) RAM

The non-multiplexed external bus interface signals are:

- Eight bidirectional Data lines (D0-D7)
- 19 Address output lines (A0-A18)
- Read Enable output (READ#)
- Write Enable output (WRITE#)
- ROM Chip Select output (ROMSEL#)
- RAM Chip Select output (RAMSEL#)

Analog Cellular Phone Interface

Analog cellular operation is selected when the LINE/CELL input is low and a cellular firmware driver is loaded. Signals supported are:

- Cell RX Bias output (RXPAD#)
- Cell TX Bias output (TXPAD#)
- Cell bidirectional Serial Data line (CELDATA)
- Cell data Clock input (CELCLK)
- Cell Busy output (CELBSY)
- Cell Busy input (CELBSY#)

NOTE: The following analog cellular interface signals are supported by the CX20437 VC:

- *Cell receive analog input (CEL_RX)*
- *Cell transmit analog output (CEL_TX)*

3.1.2 Serial Interface Configuration Only

Serial DTE Interface and Indicator Outputs (PARIF = Low)

A V.24/EIA/TIA-232-E logic-compatible serial DTE interface is selected when the PARIF input is low.

The supported DTE interface signals are:

- Serial Transmit Data input (TXD#)
- Serial Receive Data output line (RXD#)
- Clear to Send output (CTS#)
- Data Set Ready output (DSR#)
- Received Line Signal Detector (RLSD#)
- Test Mode output (TM#)
- Ring Indicator (RI#)
- Data Terminal Ready control input (DTR#)
- Request to Send control input (RTS#)

The following indicator output lines are also supported:

- Auto Answer indicator output (AAIND#)
- Data Terminal Ready indicator output (DTRIND#)
- Test Mode indicator output (TMIND#)
- Off-hook indicator output (OHIND#) (supported in non-cellular mode)

3.1.3 Parallel Interface Configuration Only (PARIF = High)

A 16550A UART-compatible parallel host bus interface is selected when the PARIF input is high.

Parallel Host Bus Interface

The parallel host interface signals are:

- Host Reset control input line (RESET#)
- Host Chip Select control input (HCS#)
- Host Read control input (HRD#)
- Host Write control input (HWT#)
- Host Interrupt output line (HINT)
- Three Host Address input lines (HA0-HA2)
- Eight Host Data lines (HD0-HD7)

GSM Interface

GSM operation is selected when the LINE/GSM input is low and GSM firmware is loaded in external ROM/flash ROM. Signals supported are:

- GSM TX Bias output (TXPAD#)
- GSM RX Bias output (RXPAD#)
- GSM Control input (GSMINP0)
- GSM serial Transmit Data output (GSMTXD)
- GSM serial Receive Data input (GSMRXD)

3.1.4 CX88168 SCM Interface Signals

SCM 128-pin TQFP hardware interface signals for parallel interface are shown by major interface in Figure 3-1, are shown by pin number in Figure 3-2, and are listed by pin number in Table 3-1. The SCM hardware interface signals for parallel interface are defined in Table 3-2.

SCM 128-pin TQFP hardware interface signals for serial interface are shown by major interface in Figure 3-3, are shown by pin number in Figure 3-4, and are listed by pin number in Table 3-3. The SCM hardware interface signals for serial interface are defined in Table 3-4.

SCM I/O types are defined in Table 3-5.

SCM DC electrical characteristics are listed in Table 3-6.

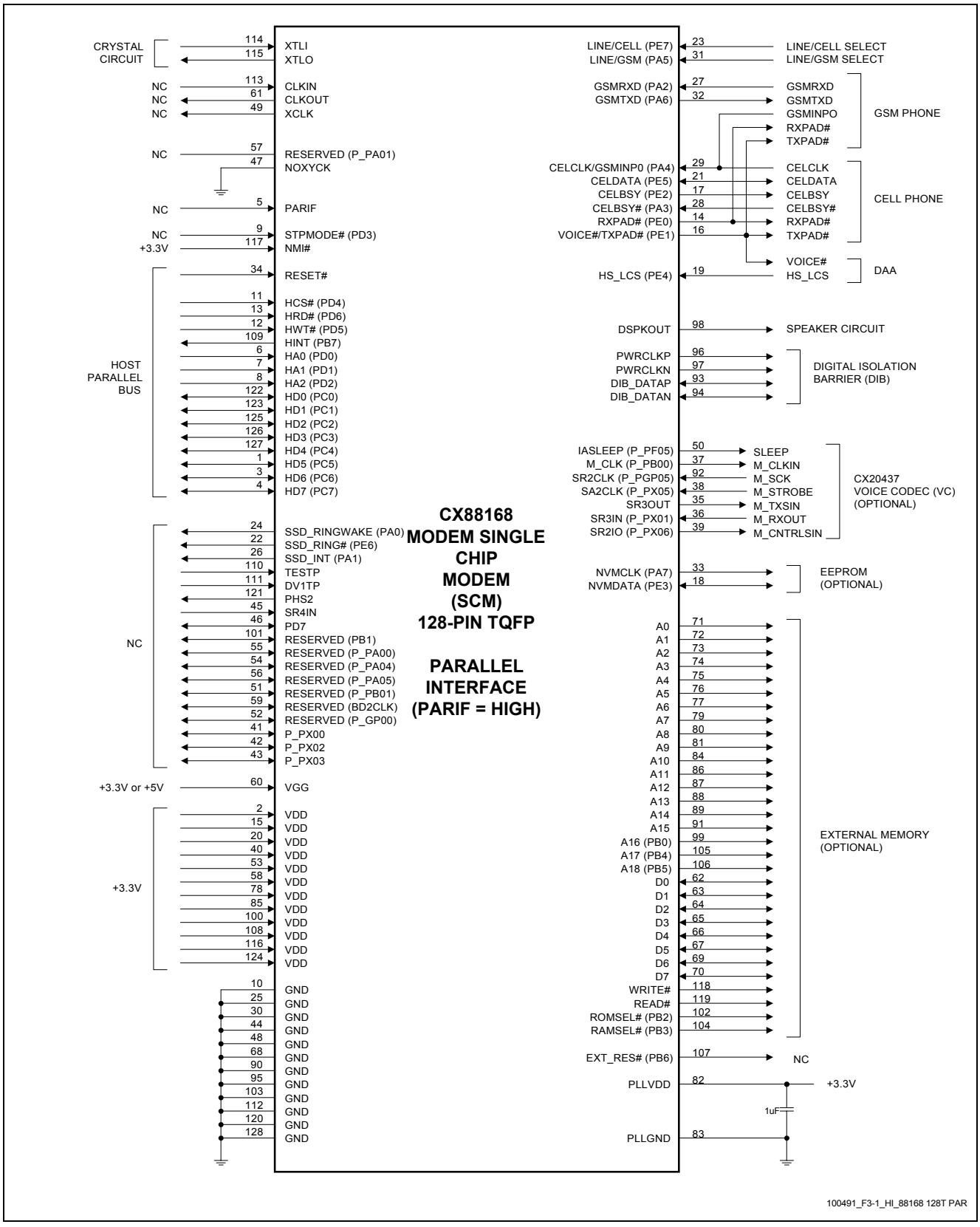


Figure 3-1. CX88168 SCM Hardware Signals for Parallel Interface (PARIF = High)

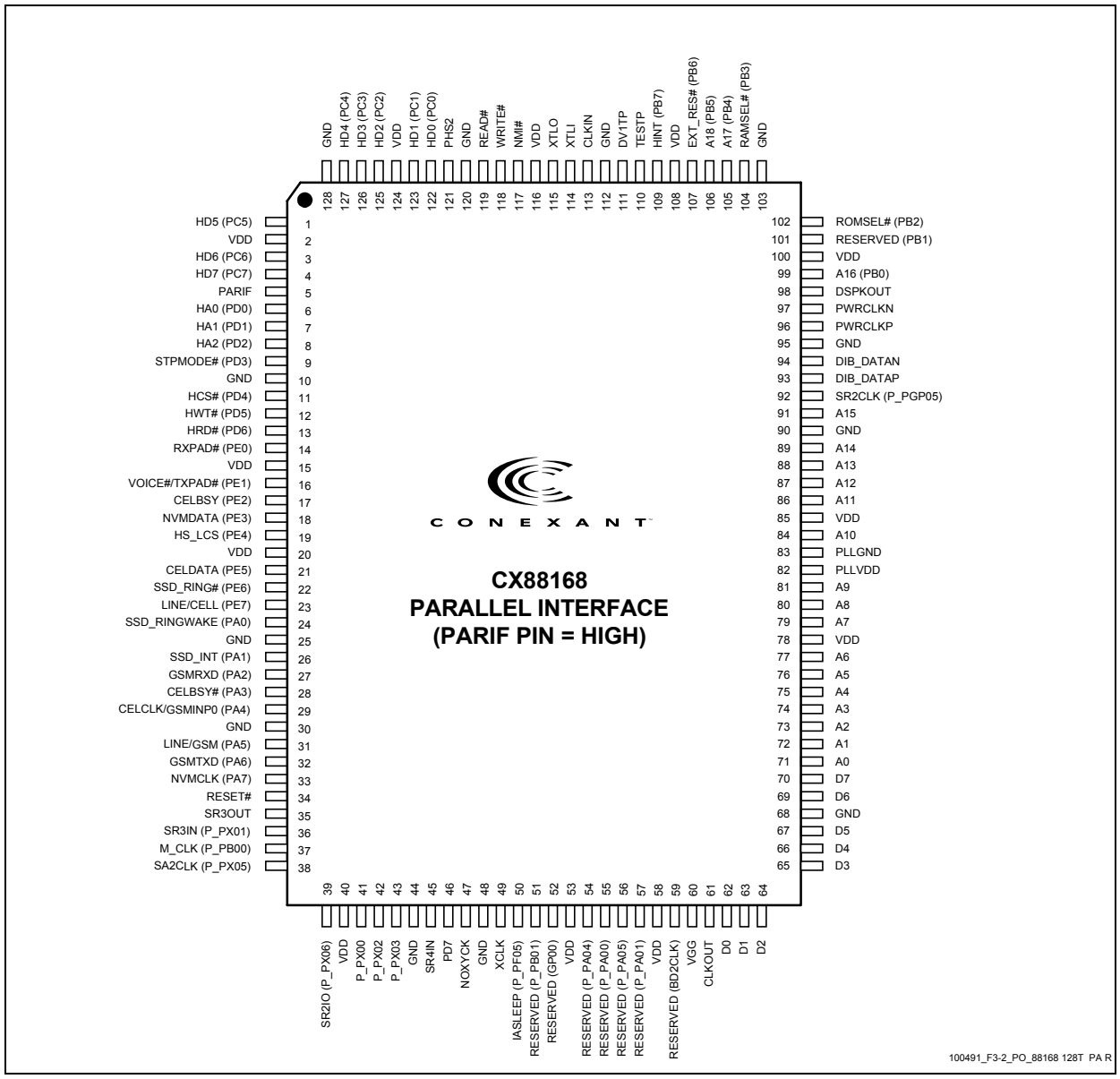


Figure 3-2. CX88168 SCM 128-Pin TQFP Pin Signals for Parallel Interface (PARIF = High)

Table 3-1. CX88168 SCM 128-Pin TQFP Pin Signals for Parallel Interface (PARIF = High)

Pin	Signal Label	I/O	I/O Type	Interface	Pin	Signal Label	I/O	I/O Type	Interface
1	HD5 (PC5)	I/O	Ith/Ot8	HB: HD5	65	D3	I/O	Ith/Ot2	EB: D3
2	VDD	P	PWR	+3.3V	66	D4	I/O	Ith/Ot2	EB: D4
3	HD6 (PC6)	I/O	Ith/Ot8	HB: HD6	67	D5	I/O	Ith/Ot2	EB: D5
4	HD7 (PC7)	I/O	Ith/Ot8	HB: HD7	68	GND	G	GND	GND
5	PARIF	I	Itpu	NC (parallel interface)	69	D6	I/O	Ith/Ot2	EB: D6
6	HA0 (PD0)	I	Ithpd/Ot2	HB: HA0	70	D7	I/O	Ith/Ot2	EB: D7
7	HA1 (PD1)	I	Ithpd/Ot2	HB: HA1	71	A0	O	It/Ot8	EB: A0
8	HA2 (PD2)	I	Ithpd/Ot2	HB: HA2	72	A1	O	It/Ot8	EB: A1
9	STPMODE# (PD3)	I	Ith/Ot2	NC	73	A2	O	It/Ot8	EB: A2
10	GND	G	GND	GND	74	A3	O	It/Ot8	EB: A3
11	HCS# (PD4)	I	It	HB: CS#	75	A4	O	It/Ot8	EB: A4
12	HWT# (PD5)	I	Ithpu	HB: WT#	76	A5	O	It/Ot8	EB: A5
13	HRD# (PD6)	I	Ithpu	HB: RD#	77	A6	O	It/Ot8	EB: A6
14	RXPAD# (PE0)	O	It/Ot8	CELL/GSM: RXPAD#	78	VDD	P	PWR	+3.3V
15	VDD	P	PWR	+3.3V	79	A7	O	It/Ot8	EB: A7
16	VOICE#/TXPAD# (PE1)	O	It/Ot2	DAA: VOICE#; CELL/GSM:TXPAD#	80	A8	O	It/Ot8	EB: A8
17	CELBSY (PE2)	O	It/Ot2	CELL: CELBSY	81	A9	O	It/Ot8	EB: A9
18	NVMDATA (PE3)	I/O	It/Ot2	NVRAM: SDA	82	PLLVDD	P	PWR	+3.3V and GND through 1 uF
19	HS_LCS (PE4)	I	It/Ot2	GND through 47 KΩ	83	PLLGND	G	GND	GND
20	VDD	P	PWR	+3.3V	84	A10	O	It/Ot8	EB: A10
21	CELDATA (PE5)	I/O	It/Ot2	CELL: CEL_DATA	85	VDD	P	PWR	+3.3V
22	SSD_RING# (PE6)	O	It/Ot2	NC	86	A11	O	It/Ot8	EB: A11
23	LINE/CELL (PE7)	I	It/Ot8	Line/Cell select	87	A12	O	It/Ot8	EB: A12
24	SSD_RINGWAKE (PA0)	O	It/Ot2	NC	88	A13	O	It/Ot8	EB: A13
25	GND	G	GND	GND	89	A14	O	It/Ot8	EB: A14
26	SSD_INT (PA1)	O	It/Ot2	NC	90	GND	G	GND	GND
27	GSMRXD (PA2)	I/O	It/Ot2	GSM: GSMRXD	91	A15	O	It/Ot8	EB: A15
28	CELBSY# (PA3)	I	Itpu/Ot2	CELL: CELBSY#	92	SR2CLK (P_PGP05)	I	Itpu/Ot2	VC: M_SCK
29	CELCLK/GSMINP0 (PA4)	I	Itpu/Ot2	CELL: CELCLK; GSM: GSMINP0	93	DIB_DATAP	I/O	Idd/Odd	DIB: Data Pos. Channel
30	GND	G	GND	GND	94	DIB_DATAN	I/O	Idd/Odd	DIB: Data Neg. Channel
31	LINE/GSM (PA5)	I	It/Ot2	Line/GSM select	95	GND	G	GND	GND
32	GSMTXD (PA6)	I/O	It/Ot2	GSM: GSMTXD	96	PWRCLKP	O	Odpc	DIB: Transformer primary winding non-dotted terminal
33	NVMCLK (PA7)	O	It/Ot2	NVRAM: SCL	97	PWRCLKN	O	Odpc	DIB: Transformer primary winding dotted terminal
34	RESET#	I	It	HB: RESET#	98	DSPKOUT	O	It/Ot2	Speaker Circuit
35	SR3OUT	O	Ot2	VC: M_TXSIN	99	A16 (PB0)	O	It/Ot2	EB: A16
36	SR3IN (P_PX01)	I	Itk/Ot2	VC: M_RXOUT	100	VDD	P	PWR	+3.3V
37	M_CLK (P_PB00)	O	It/Ot2	VC: M_CLKIN	101	RESERVED (PB1)	O	It/Ot2	NC
38	SA2CLK (P_PX05)	I	Itpu/Ot2	VC: M_STROBE	102	ROMSEL# (PB2)	O	Ot2	EB: ROM CE#
39	SR2IO (P_PX06)	O	It/Ot2	VC: M_CNTRLSIN	103	GND	G	GND	GND
40	VDD	P	PWR	+3.3V	104	RAMSEL# (PB3)	O	It/Ot2	EB: RAM CS#
41	P_PX00	I/O	It/Ot8	NC	105	A17 (PB4)	O	It/Ot2	EB: A17
42	P_PX02	I/O	Itpu/Ot2	NC	106	A18 (PB5)	O	It/Ot2	EB: A18
43	P_PX03	I/O	Itpu/Ot2	NC	107	EXT_RES# (PB6)	O	It/Ot2	NC
44	GND	G	GND	GND	108	VDD	P	PWR	+3.3V
45	SR4IN	I	Itk	NC	109	HINT (PB7)	O	It/Ot8	HB: HINT
46	PD7	I/O	It/Ot2	NC	110	TESTP	I	Itpu	NC
47	NOXYCK	I	Itpu	GND	111	DV1TP	I	Itpu	NC
48	GND	G	GND	GND	112	GND	G	GND	GND
49	XCLK	O	It/Ot2	NC	113	CLKIN	I	It	NC
50	IASLEEP (P_PF05)	O	Ot2	VC: SLEEP	114	XTLI	I	Ix	Crystal Circuit

Table 3-1. CX88168 SCM 128-Pin TQFP Pin Signals for Parallel Interface (PARIF = High) (Continued)

Pin	Signal Label	I/O	I/O Type	Interface	Pin	Signal Label	I/O	I/O Type	Interface
51	RESERVED (P_PB01)	I/O	Itpu/Ot2	NC	115	XTLO	O	Ox	Crystal Circuit
52	RESERVED (GP00)	I/O	It/Ot2	NC	116	VDD	P	PWR	+3.3V
53	VDD	P	PWR	+3.3V	117	NMI#	I	Ithpu	+3.3V
54	RESERVED (P_PA04)	I/O	Itpu/Ot2	NC	118	WRITE#	O	It/Ot2	EB: WRITE#
55	RESERVED (P_PA00)	I/O	Itpu/Ot2	NC	119	READ#	O	It/Ot2	EB: READ#
56	RESERVED (P_PA05)	I/O	Itk/Ot2	NC	120	GND	G	GND	GND
57	RESERVED (P_PA01)	I/O	Itpu/Ot2	NC	121	PHS2	O	Ot2	NC
58	VDD	P	PWR	+3.3V	122	HD0 (PC0)	I/O	Ith/Ot8	HB: HD0
59	RESERVED (BD2CLK)	O	Itpu/Ot2	NC	123	HD1 (PC1)	I/O	Ith/Ot8	HB: HD1
60	VGG	P	PWRG	+3.3V or +5V	124	VDD	P	PWR	+3.3V
61	CLKOUT	O	It/Ot2	NC	125	HD2 (PC2)	I/O	Ith/Ot8	HB: HD2
62	D0	I/O	Ith/Ot2	EB: D0	126	HD3 (PC3)	I/O	Ith/Ot8	HB: HD3
63	D1	I/O	IthOt2	EB: D1	127	HD4 (PC4)	I/O	Ith/Ot8	HB: HD4
64	D2	I/O	Ith/Ot2	EB: D2	128	GND	G	GND	GND

Notes:

1. I/O Types: See Table 3-5.
2. Interface Legend:

DIB	Digital Isolation Barrier
EB	Expansion Bus
HB	Host Bus
NC	No internal pin connection
VC	Voice Codec

Table 3-2. CX88168 SCM Pin Signal Definitions for Parallel Interface (PARIF = High)

Label	Pin	I/O	I/O Type	Signal Name/Description
System				
XTLI, XTLO	114, 115	I, O	Ix, Ox	**Crystal In and Crystal Out.** If an external 28.224 MHz crystal circuit is used instead of an external clock circuit, connect XTLI and XTLO to the external crystal circuit and leave CLKIN open.
CLKIN	113	I	It	**Clock In.** If an external 28.224 MHz clock circuit is used instead of an external crystal circuit, connect CLKIN to the clock output and leave XTLI and XTLO open.
CLKOUT	61	O	It/Ot2	**Clock Out.** 28.224 MHz output clock. Leave open.
PARIF	5	I	Itpu	**Parallel/Serial Interface Select.** PARIF input high (open) selects parallel host interface operation (see this table); PARIF low (GND) selects serial DTE interface operation (see Table 3-4).
STPMODE# (PD3)	9	I	Ith/Ot2	**Stop Mode.** Not used. Leave open.
NMI#	117	I	Ithpu	**Non-Maskable Interrupt.** Not used. Connect to +3.3V.
RESET#	34	I	It	**Reset.** The active low RESET# input resets the SCM logic, and restores the saved configuration from serial EEPROM or returns the modem to the factory default values if NVRAM is not present. RESET# low holds the modem in the reset state; RESET# going high releases the modem from the reset state. After application of VDD, RESET# must be held low for at least 15 ms after the VDD power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of RESET#. For parallel Interface, connect RESET# input to the host bus RESET line through an inverter.
VGG	60	P	PWRG	**I/O Signaling Voltage Source.** Connect to +3.3V for +3.3V inputs or +5V for +5V inputs.
VDD	2, 15, 20, 40, 53, 58, 78, 85, 100, 108, 116, 124	P	PWR	**Digital Supply Voltage.** Connect to VCC (+3.3V, filtered).
GND	10, 25, 30, 44, 48, 68, 90, 95, 103, 112, 120, 128	G	GND	**Digital Ground.** Connect to digital ground (GND).
SSD_RING# (PE6)	22	O	It/Ot2	**SmartDAA Raw Ring.** A toggling edge used to indicate presence of a ring frequency. The idle state (no ringing) output of the ring detect circuit is high.
SSD_INT (PA1)	26	O	It/Ot2	**SmartDAA Interface Interrupt.** Active low output used to indicate to the host when the SmartDAA Interface needs servicing.
SSD_RINGWAKE (PA0)	24	O	It/Ot2	**SmartDAA Ring Wake.** Active high output used to indicate to the host that a valid ring or line polarity reversal has been detected.
PLLVDD	82	P	PWR	**PLL Circuit Digital Supply Voltage.** Connect to +3.3V and to GND through 1 μF.
PLLGND	83	G	GND	**PLL Circuit Digital Ground.** Connect to GND.
Serial EEPROM (NVRAM) Interface				
NVMCLK (PA7)	33	O	It/Ot2	**NVRAM Clock.** NVMCLK output high enables the EEPROM. Connect to EEPROM SCL pin.
NVMDATA (PE3)	18	I/O	It/Ot2	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the EEPROM. Connect to EEPROM SDA pin and to +3.3V through 10 KΩ.

Table 3-2. CX88168 SCM Pin Signal Definitions for Parallel Interface (PARIF = High) (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Speaker Interface				
DSPKOUT	98	O	It/Ot2	**Modem Speaker Digital Output.** The DSPKOUT digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator.
DIB Interface				
PWRCLKP	96	O	Odpc	**Clock and Power Positive.** Provides clock and power to the LSD. Connect to DIB transformer primary winding non-dotted terminal.
PWRCLKN	97	O	Odpc	**Clock and Power Negative.** Provides clock and power to the LSD. Connect to DIB transformer primary winding dotted terminal.
DIB_DATAP	93	I/O	Idd/Odd	**Data Positive.** Transfers data, control, and status information between the SCM and the LSD. Connect to LSD through DIB data positive channel components.
DIB_DATAN	94	I/0	Idd/Odd	**Data Negative.** Transfers data, control, and status information between the SCM and the LSD. Connect to LSD through DIB data negative channel components.
External Bus Interface				
A0-A9, A10-A15, A16 (PB0), A17 (PB4), A18 (PB5)	71-77, 79-81, 84, 86-89, 91, 99, 105, 106	O, O, O, O, O	It/Ot8, It/Ot8, It/Ot2, It/Ot2, It/Ot2	**Address Lines 0-18.** A0-A18 are the address output lines used to access optional external memory; up to 4 Mbits (512k bytes) ROM/flash ROM using A0-A18 and up to 1 Mbit (128k bytes) RAM using A0-A16. If internal ROM is used for the 256k-byte base modem ROM code and external ROM/flash ROM is used only for the additional GSM ROM code, the 128k-byte GSM ROM code is located in the upper-most portion of the 512k-byte address range with A17 used as GSM ROM select. If external ROM/flash ROM is used for the base modem ROM, the 256k-byte base modem ROM code is located in the 0-256k-byte address range. If included, the 128k-byte GSM ROM code is located in the upper-most portion of the 512k-byte address range.
D0-D7	62-67, 69-70	I/O	Ith/Ot2	**Data Line 0-7.** D0-D7 are the bidirectional external memory bus data lines.
READ#	119	O	It/Ot2	**Read Enable.** READ# output low enables data transfer from the selected device to the D0-D7 lines.
WRITE#	118	O	It/Ot2	**Write Enable.** WRITE# output low enables data transfer from the D0-D7 lines to the selected device.
ROMSEL# (PB2)	102	O	Ot2	**ROM Select**. ROMSEL# (PB2, ES3) output low selects the external ROM/flash ROM.
RAMSEL# (PB3)	104	O	It/Ot2	**RAM Select.** RAMSEL#, PB3 (ES2) output low selects the external RAM.
RESERVED (PB1)	101	O	It/Ot2	**Reserved.** PB1 (ES4) is used internally. Leave open.
EXT_RES# (PB6)	107	O	It/Ot2	**External Device Reset.** Active low reset for external devices. Leave open if not used.
CX20437 VC Interface				
IASLEEP (P_PF05)	50	O	Ot2	**Modem Sleep.** Connect to VC SLEEP pin.
M_CLK (P_PB00)	37	O	It/Ot2	**Master Clock Output**. Connect to VC M_CLKIN pin.
SR2CLK (P_PGP05)	92	I	Itpu/Ot2	**Voice Serial Clock input.** Connect to VC M_SCK pin.
SA2CLK (P_PX05)	38	I	Itpu/Ot2	**Voice Serial Frame Sync Input.** Connect to VC M_STROBE pin.
SR3OUT	35	O	Ot2	**Voice Serial Transmit Data Output.** Connect to VC M_TXSIN pin.
SR3IN (P_PX01)	36	I	Itk/Ot2	**Voice Serial Receive Data Input.** Connect to VC M_RXOUT pin.
SR2IO (P_PX06)	39	O	It/Ot2	**Voice Control Output.** Connect to VC M_CNTRLSIN pin.

Table 3-2. CX88168 SCM Pin Signal Definitions for Parallel Interface (PARIF = High) (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Telephone Line/Analog Cellular Phone/GSM Phone Interface Select				
LINE/GSM (PA5)	31	I	It/Ot2	**Line/GSM Interface Select.** In conjunction with the LINE/CELL input, selects telephone line, cellular phone (AMPS), or GSM phone interface.
LINE/CELL (PE7)	23	I	It/Ot8	**Line/Cellar Interface Select.** In conjunction with the LINE/GSM input, selects telephone line, cellular phone (AMPS), or GSM phone interface, as follows: **LINE/CELL** / **LINE/GSM** / **Interface Selected** H / H / Telephone Line L / H / Cellular (AMPS) H / L / GSM L / L / Invalid The following ports operate as indicated for the selected interface: **Port** / **Telephone Line** / **Analog Cellular** / **GSM** PE0 / — / RXPAD# / RXPAD# PE1 / VOICE# / TXPAD# / TXPAD# PE2 / — / CELBSY / — PE5 / — / CELDATA / — PA2 / — / — / GSMRXD PA3 / — / CELBSY# / — PA4 / — / CELCLK / GSMINP0 PA6 / — / — / GSMTXD **Note:** Ports marked "—" are not used.
Parallel Host Interface				
HCS# (PD4)	11	I	It	**Host Bus Chip Select.** HCS# input low enables the MCU host bus interface.
HWT# (PD5)	12	I	Ithpu	**Host Bus Write.** HWT# is an active low, write control input. When HCS# is low, HWT# low allows the host to write data or control words into a selected MCU register.
HRD# (PD6)	13	I	Ithpu	**Host Bus Read.** HRD# is an active low, read control input. When HCS# is low, HRD# low allows the host to read status information or data from a selected MCU register.
HINT (PB7)	109	O	It/Ot8	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt is asserted. HINT is reset low upon the appropriate interrupt service or master reset operation.
HA0-HA2 (PD0-PD2)	6-8	I	Ithpd/Ot2	**Host Bus Address Lines 0-2.** During a host read or write operation with HCS# low, HA0-HA2 select an internal MCU 16550A-compatible register.
HD0-HD7 (PC0-PC7)	122-123, 125-127, 1, 3-4	I/O	Ith/Ot8	**Host Bus Data Lines 0-7**. HD0-HD7 are three-state input/output lines providing bidirectional communication between the host and the MCU. Data, control words, and status information are transferred over HD0-HD7.
Analog Cellular Phone Interface (LINE/CELL = Low and LINE/GSM = High)				
CELCLK/GSMINP0 (PA4)	29	I	Itpu/Ot2	**Cellular Clock.** Defined by the cellular firmware driver.
CELDATA (PE5)	21	I/O	It/Ot2	**Cellular Data**. Defined by the cellular firmware driver.
CELBSY (PE2)	17	O	It/Ot2	**Cellular Busy.** Defined by the cellular firmware driver.
CELBSY# (PA3)	28	I	Itpu/Ot2	**Cellular Not Busy.** Defined by the cellular firmware driver.
RXPAD# (PE0)	14	O	It/Ot8	**Cellular RX Bias.** Defined by the cellular firmware driver.
VOICE#/TXPAD# (PE1)	16	O	It/Ot2	**Cellular TX Bias.** Defined by the cellular firmware driver.

Table 3-2. CX88168 SCM Pin Signal Definitions for Parallel Interface (PARIF = High) (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Telephone Interface (LINE/CELL = High and LINE/GSM = High)				
VOICE#/TXPAD# (PE1)	16	O	It/Ot2	**Voice Relay Control.** When the LINE/CELL input is high, this output (typically active low) used to control the normally open voice relay. See cellular interface signals for TXPAD# usage.
HS_LCS (PE4)	19	I	It/Ot2	**Handset Line Current Sense.** LCS is an active high input that indicates a handset off-hook status. Not required for data/fax/voice/speakerphone operation. If not used, connect to GND through 47 KΩ.
GSM Cellular Phone Interface (LINE/CELL = High and LINE/GSM = Low)				
CELCLK/GSMINP0 (PA4)	29	I	Itpu/Ot2	**GSM Input Control.** Defined by the GSM firmware driver.
GSMRXD (PA2)	27	I	It/Ot2	**GSM Serial Receive Data.** Defined by the GSM firmware driver.
GSMTXD (PA6)	32	O	It/Ot2	**GSM Serial Transmit Data.** Defined by the GSM firmware driver.
RXPAD# (PE0)	14	O	It/Ot8	**GSM RX Bias.** Defined by the GSM firmware driver.
VOICE#/TXPAD# (PE1)	16	O	It/Ot2	**GSM TX Bias.** Defined by the GSM firmware driver.
Not Used				
NOXYCK	47	I	Itpu	**Disable XCLK Output**. When low, disables XCLK output (reduces internal power consumption). When high, enables XCLK output. Connect to GND.
TESTP	110	I	Itpu	**Test.** Used for factory test only. Leave open.
DV1TP	111	I	Itpu	**Test.** Used for factory test only. Leave open.
XCLK	49	O	It/Ot2	**Not Used.** Leave open.
PHS2	121	O	Ot2	**Not Used.** Leave open.
SR4RIN	45	I	Itk	**Not Used.** Leave open.
PD7	46	I/O	It/Ot2	**Not Used.** Leave open.
P_PX00	41	I/O	It/Ot8	**Not Used.** Leave open.
P_PX02	42	I/O	Itpu/Ot2	**Not Used.** Leave open.
P_PX03	43	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (GP00)	52	I/O	It/Ot2	**Not Used.** Leave open.
RESERVED (P_PA00)	55	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (P_PA01)	57	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (P_PA04)	54	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (P_PA05)	56	I/O	Itk/Ot2	**Not Used.** Leave open.
RESERVED (P_PB01)	51	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (P_BD2CLK)	59	I/O	Itpu/Ot2	**Not Used.** Leave open.

Notes:

1. I/O Types: See Table 3-5.
2. Interface Legend:

DIB	Digital Isolation Barrier
EB	Expansion Bus
HB	Host Bus
NC	No internal pin connection
VC	Voice Codec

RESERVED = No external connection allowed (may have internal connection).

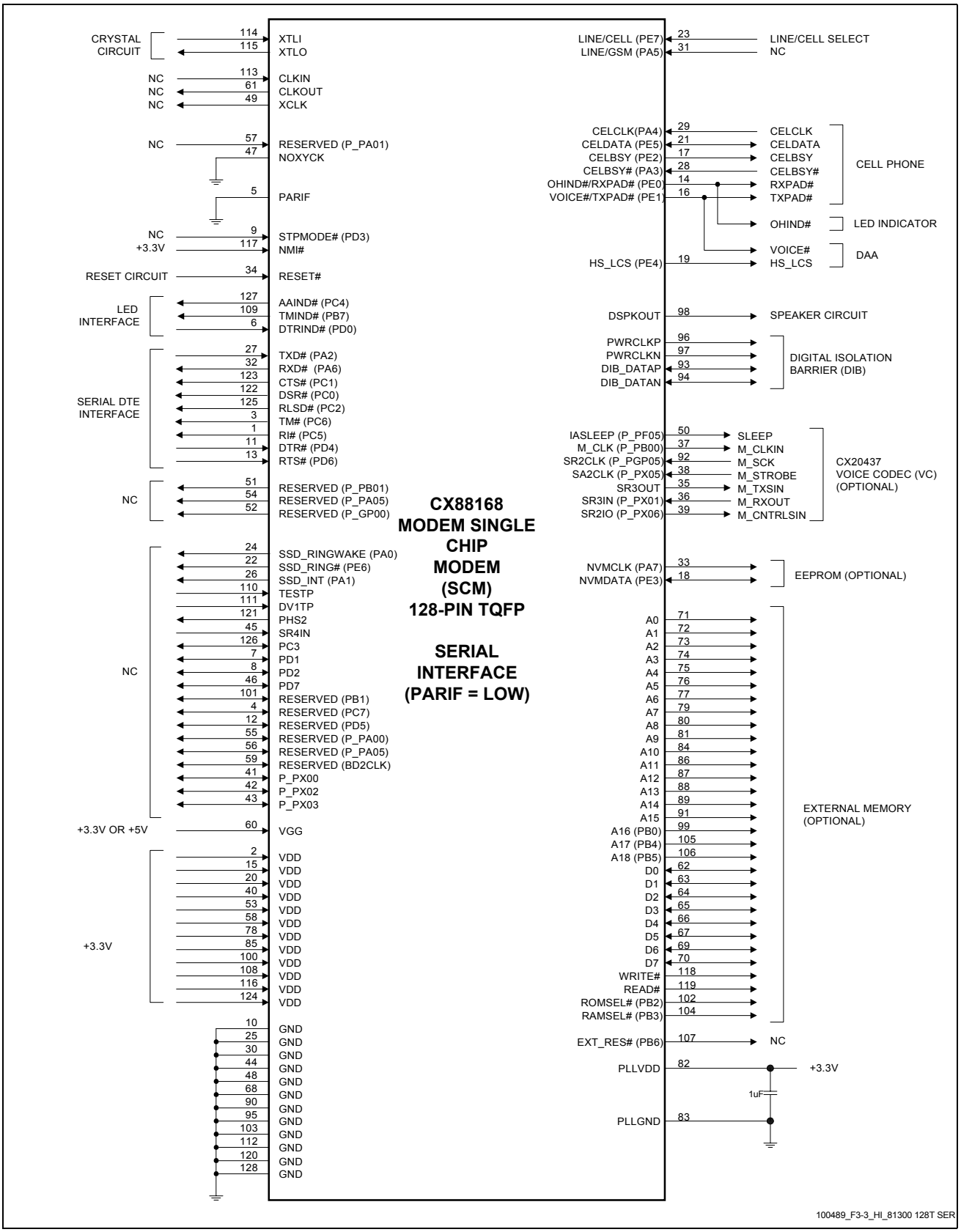


Figure 3-3. CX88168 SCM Hardware Signals for Serial Interface (PARIF = Low)

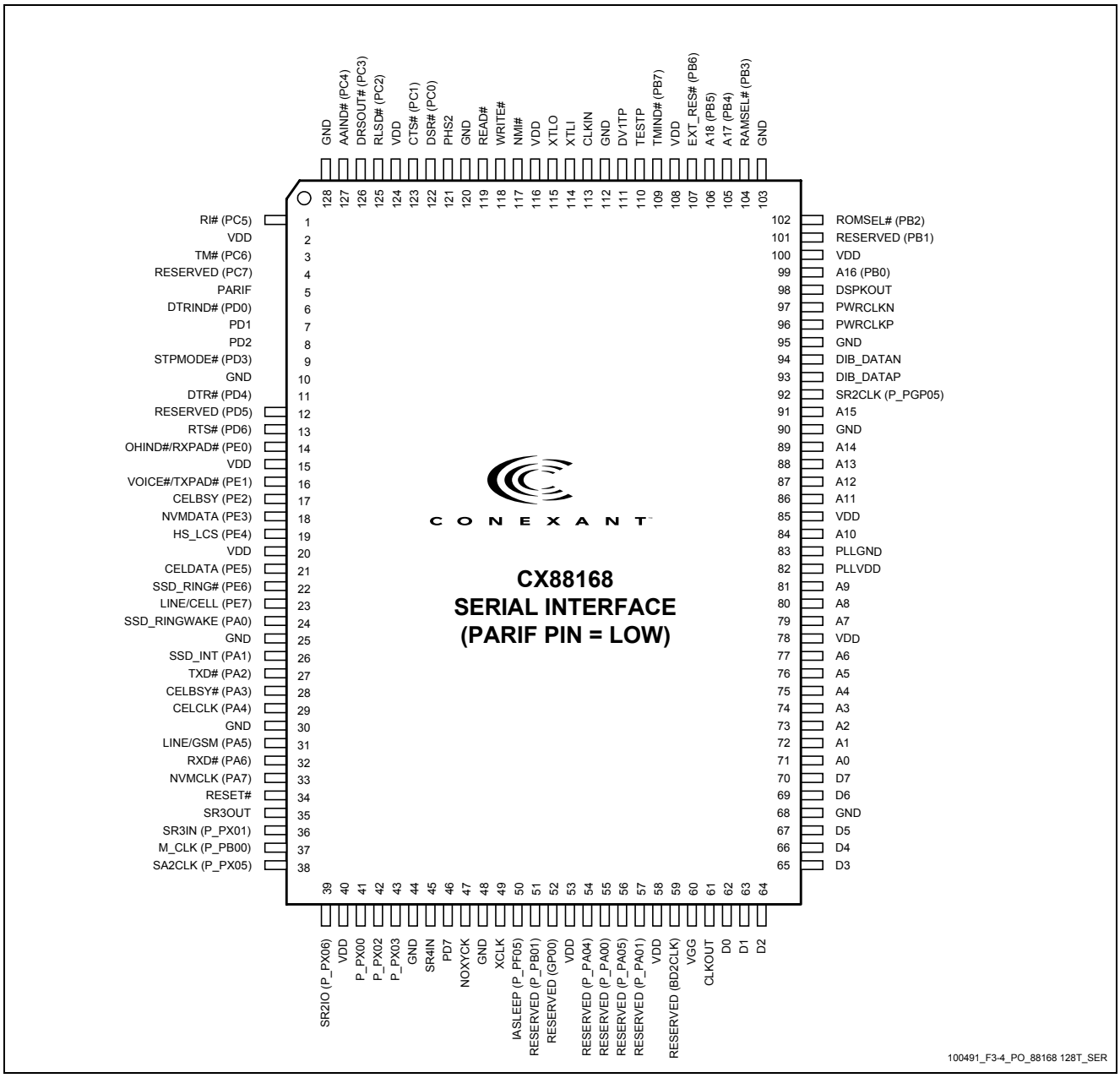


Figure 3-4. CX88168 SCM 128-Pin TQFP Pin Signals for Serial Interface (PARIF = Low)

Table 3-3. CX88168 SCM 128-Pin TQFP Pin Signals for Serial Interface (PARIF = Low)

Pin	Signal Label	I/O	I/O Type	Interface	Pin	Signal Label	I/O	I/O Type	Interface
1	RI# (PC5)	O	Ith/Ot8	DTE IF: RI#	65	D3	I/O	Ith/Ot2	EB: D3
2	VDD	P	PWR	+3.3V	66	D4	I/O	Ith/Ot2	EB: D4
3	TM# (PC6)	O	Ith/Ot8	DTE IF: TM#	67	D5	I/O	Ith/Ot2	EB: D5
4	RESERVED (PC7)	I	Ith/Ot8	+3.3V through 47K Ω	68	GND	G	GND	GND
5	PARIF	I	Itpu	GND (serial interface)	69	D6	I/O	Ith/Ot2	EB: D6
6	DTRIND# (PD0)	O	Ithpd/Ot2	LED: DTRIND#	70	D7	I/O	Ith/Ot2	EB: D7
7	PD1	I/O	Ithpd/Ot2	NC	71	A0	O	It/Ot8	EB: A0
8	PD2	I/O	Ithpd/Ot2	NC	72	A1	O	It/Ot8	EB: A1
9	STPMODE# (PD3)	I	Ith/Ot2	NC	73	A2	O	It/Ot8	EB: A2
10	GND	G	GND	GND	74	A3	O	It/Ot8	EB: A3
11	DTR# (PD4)	I	It	DTE IF: DTR#	75	A4	O	It/Ot8	EB: A4
12	RESERVED (PD5)	I	Ithpu	NC	76	A5	O	It/Ot8	EB: A5
13	RTS# (PD6)	I	Ithpu	DTE IF: RTS#	77	A6	O	It/Ot8	EB: A6
14	OHIND#/RXPAD# (PE0)	O	It/Ot8	LED: OHIND# CELL: RXPAD#	78	VDD	P	PWR	+3.3V
15	VDD	P	PWR	+3.3V	79	A7	O	It/Ot8	EB: A7
16	VOICE#/ TXPAD# (PE1)	O	It/Ot2	DAA: VOICE#; CELL:TXPAD#	80	A8	O	It/Ot8	EB: A8
17	CELBSY (PE2)	O	It/Ot2	CELL: CELBSY	81	A9	O	It/Ot8	EB: A9
18	NVMDATA (PE3)	I/O	It/Ot2	NVRAM: SDA	82	PLLVDD	P	PWR	+3.3V and GND through 1 uF
19	HS_LCS (PE4)	I	It/Ot2	GND through 47 KΩ	83	PLLGND	G	GND	GND
20	VDD	P	PWR	+3.3V	84	A10	O	It/Ot8	EB: A10
21	CELDATA (PE5)	I/O	It/Ot2	CELL: CEL_DATA	85	VDD	P	PWR	+3.3V
22	SSD_RING# (PE6)	O	It/Ot2	NC	86	A11	O	It/Ot8	EB: A11
23	LINE/CELL (PE7)	I	It/Ot8	Line/Cell select	87	A12	O	It/Ot8	EB: A12
24	SSD_RINGWAKE (PA0)	O	It/Ot2	NC	88	A13	O	It/Ot8	EB: A13
25	GND	G	GND	GND	89	A14	O	It/Ot8	EB: A14
26	SSD_INT (PA1)	O	It/Ot2	NC	90	GND	G	GND	GND
27	TXD# (PA2)	I	It/Ot2	DTE IF: TXD#	91	A15	O	It/Ot8	EB: A15
28	CELBSY# (PA3)	I	Itpu/Ot2	CELL: CELBSY#	92	SR2CLK (P_PGP05)	I	Itpu/Ot2	VC: M_SCK
29	CELCLK/GSMINP0 (PA4)	I	Itpu/Ot2	CELL: CELCLK	93	DIB_DATAP	I/O	Idd/Odd	DIB: Data Pos. Channel
30	GND	G	GND	GND	94	DIB_DATAN	I/O	Idd/Odd	DIB: Data Neg. Channel
31	LINE/GSM (PA5)	I	It/Ot2	NC	95	GND	G	GND	GND
32	RXD# (PA6)	O	It/Ot2	DTE IF: RXD#	96	PWRCLKP	O	Odpc	DIB: Transformer primary winding non-dotted terminal
33	NVMCLK (PA7)	O	It/Ot2	NVRAM: SCL	97	PWRCLKN	O	Odpc	DIB: Transformer primary winding dotted terminal
34	RESET#	I	It	Reset Circuit	98	DSPKOUT	O	It/Ot2	Speaker Circuit
35	SR3OUT	O	Ot2	VC: M_TXSIN	99	A16 (PB0)	O	It/Ot2	EB: A16
36	SR3IN (P_PX01)	I	Itk/Ot2	VC: M_RXOUT	100	VDD	P	PWR	+3.3V
37	M_CLK (P_PB00)	O	It/Ot2	VC: M_CLKIN	101	RESERVED (PB1)	O	It/Ot2	NC
38	SA2CLK (P_PX05)	I	Itpu/Ot2	VC: M_STROBE	102	ROMSEL# (PB2)	O	Ot2	EB: ROM CE#
39	SR2IO (P_PX06)	O	It/Ot2	VC: M_CNTRLSIN	103	GND	G	GND	GND
40	VDD	P	PWR	+3.3V	104	RAMSEL# (PB3)	O	It/Ot2	EB: RAM CS#
41	P_PX00	I/O	It/Ot8	NC	105	A17 (PB4)	O	It/Ot2	EB: A17
42	P_PX02	I/O	Itpu/Ot2	NC	106	A18 (PB5)	O	It/Ot2	EB: A18
43	P_PX03	I/O	Itpu/Ot2	NC	107	EXT_RES# (PB6)	O	It/Ot2	NC
44	GND	G	GND	GND	108	VDD	P	PWR	+3.3V
45	SR4IN	I	Itk	NC	109	TMIND# (PB7)	O	It/Ot8	LED: TMIND#
46	PD7	I/O	It/Ot2	NC	110	TESTP	I	Itpu	NC
47	NOXYCK	I	Itpu	GND	111	DV1TP	I	Itpu	NC
48	GND	G	GND	GND	112	GND	G	GND	GND
49	XCLK	O	It/Ot2	NC	113	CLKIN	I	It	NC
50	IASLEEP (P_PF05)	O	Ot2	VC: SLEEP	114	XTLI	I	Ix	Crystal Circuit

Table 3-3. CX88168 SCM 128-Pin TQFP Pin Signals for Serial Interface (PARIF = Low) (Continued)

Pin	Signal Label	I/O	I/O Type	Interface	Pin	Signal Label	I/O	I/O Type	Interface
51	RESERVED (P_PB01)	I/O	Itpu/Ot2	NC	115	XTLO	O	Ox	Crystal Circuit
52	RESERVED (GP00)	I/O	It/Ot2	NC	116	VDD	P	PWR	+3.3V
53	VDD	P	PWR	+3.3V	117	NMI#	I	Ithpu	+3.3V
54	RESERVED (P_PA04)	I/O	Itpu/Ot2	NC	118	WRITE#	O	It/Ot2	EB: WRITE#
55	RESERVED (P_PA00)	I/O	Itpu/Ot2	NC	119	READ#	O	It/Ot2	EB: READ#
56	RESERVED (P_PA05)	I/O	Itk/Ot2	NC	120	GND	G	GND	GND
57	RESERVED (P_PA01)	I/O	Itpu/Ot2	NC	121	PHS2	O	Ot2	NC
58	VDD	P	PWR	+3.3V	122	DSR# (PC0)	I/O	Ith/Ot8	DTE IF: DSR#
59	RESERVED (BD2CLK)	O	Itpu/Ot2	NC	123	CTS# (PC1)	I/O	Ith/Ot8	DTE IF: CTS#
60	VGG	P	PWRG	+3.3V or +5V	124	VDD	P	PWR	+3.3V
61	CLKOUT	O	It/Ot2	NC	125	RLSD# (PC2)	I/O	Ith/Ot8	DTE IF: RLSD#
62	D0	I/O	Ith/Ot2	EB: D0	126	PC3	I/O	Ith/Ot8	NC
63	D1	I/O	IthOt2	EB: D1	127	AAIND# (PC4)	O	Ith/Ot8	LED: AAIND#
64	D2	I/O	Ith/Ot2	EB: D2	128	GND	G	GND	GND

Notes:

1. I/O Types: See Table 3-5.
2. Interface Legend:

DIB	Digital Isolation Barrier
EB	Expansion Bus
HB	Host Bus
NC	No internal pin connection
VC	Voice Codec

Table 3-4. CX88168 SCM Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
System				
XTLI, XTLO	114, 115	I, O	Ix, Ox	**Crystal In and Crystal Out.** If an external 28.224 MHz crystal circuit is used instead of an external clock circuit, connect XTLI and XTLO to the external crystal circuit and leave CLKIN open.
CLKIN	113	I	It	**Clock In.** If an external 28.224 MHz clock circuit is used instead of an external crystal circuit, connect CLKIN to the clock output and leave XTLI and XTLO open.
CLKOUT	61	O	It/Ot2	**Clock Out.** 28.224 MHz output clock. Leave open.
PARIF	5	I	Itpu	**Parallel/Serial Interface Select.** PARIF input high (open) selects parallel host interface operation (see signal definitions in Table 3-2); PARIF low (GND) selects serial DTE interface operation (see signal definitions in this table).
STPMODE# (PD3)	9	I	Ith/Ot2	**Stop Mode.** Not used. Leave open.
NMI#	117	I	Ithpu	**Non-Maskable Interrupt.** Not used. Connect to +3.3V.
RESET#	34	I	It	**Reset.** The active low RESET# input resets the SCM logic, and restores the saved configuration from serial EEPROM or returns the modem to the factory default values if NVRAM is not present. RESET# low holds the modem in the reset state; RESET# going high releases the modem from the reset state. After application of VDD, RESET# must be held low for at least 15 ms after the VDD power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of RESET#. For serial Interface, the RESET# input is typically connected to a reset switch circuit.
VGG	60	P	PWRG	**I/O Signaling Voltage Source.** Connect to +3.3V.
VDD	2, 15, 20, 40, 53, 58, 78, 85, 100, 108, 116, 124	P	PWR	**Digital Supply Voltage.** Connect to VCC (+3.3V, filtered).
GND	10, 25, 30, 44, 48, 68, 90, 95, 103, 112, 120, 128	G	GND	**Digital Ground.** Connect to digital ground (GND).
SSD_RING# (PE6)	22	O	It/Ot2	**SmartDAA Raw Ring.** A toggling edge used to indicate presence of a ring frequency. The idle state (no ringing) output of the ring detect circuit is high.
SSD_INT (PA1)	26	O	It/Ot2	**SmartDAA Interface Interrupt.** Active low output used to indicate to the host when the SmartDAA Interface needs servicing.
SSD_RINGWAKE (PA0)	24	O	It/Ot2	**SmartDAA Ring Wake.** Active high output used to indicate to the host that a valid ring or line polarity reversal has been detected.
PLLVDD	82	P	PWR	**PLL Circuit Digital Supply Voltage.** Connect to +3.3V and to GND through 1 μF.
PLLGND	83	G	GND	**PLL Circuit Digital Ground.** Connect to GND.
Serial EEPROM (NVRAM) Interface				
NVMCLK (PA7)	33	O	It/Ot2	**NVRAM Clock.** NVMCLK output high enables the EEPROM. Connect to EEPROM SCL pin.
NVMDATA (PE3)	18	I/O	It/Ot2	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the EEPROM. Connect to EEPROM SDA pin and to +3.3V through 10 KΩ..

Table 3-4. CX88168 SCM Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
Speaker Interface				
DSPKOUT	98	O	It/Ot2	**Modem Speaker Digital Output.** The DSPKOUT digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator.
DIB Interface				
PWRCLKP	96	O	Odpc	**Clock and Power Positive.** Provides clock and power to the LSD. Connect to DIB transformer primary winding non-dotted terminal.
PWRCLKN	97	O	Odpc	**Clock and Power Negative.** Provides clock and power to the LSD. Connect to DIB transformer primary winding dotted terminal.
DIB_DATAP	93	I/O	Idd/Odd	**Data Positive.** Transfers data, control, and status information between the SCM and the LSD. Connect to LSD through DIB data positive channel components.
DIB_DATAN	94	I/0	Idd/Odd	**Data Negative.** Transfers data, control, and status information between the SCM and the LSD. Connect to LSD through DIB data negative channel components.
External Bus Interface				
A0-A9, A10-A15, A16 (PB0), A17 (PB4), A18 (PB5)	71-77, 79-81, 84, 86-89, 91, 99, 105, 106	O, O, O, O, O	It/Ot8, It/Ot8, It/Ot2, It/Ot2, It/Ot2	**Address Lines 0-18.** A0-A18 are the address output lines used to access optional external memory; up to 4 Mbits (512k bytes) ROM/flash ROM using A0-A18 and up to 1 Mbit (128k bytes) RAM using A0-A16. If internal ROM is used for the base modem ROM code and external ROM/flash ROM is used only for the additional GSM ROM code, the 128k-byte GSM ROM code is located in the upper-most portion of the 512k-byte address range with A17 used as GSM ROM select. If external ROM/flash ROM is used for the base modem ROM, the 256k-byte base modem ROM code is located in the 0-256k-byte address range. If included, the 128k-byte GSM ROM code is located in the upper-most portion of the 512k-byte address range.
D0-D7	62-67, 69-70	I/O	Ith/Ot2	**Data Line 0-7.** D0-D7 are bidirectional external memory bus data lines.
READ#	119	O	It/Ot2	**Read Enable.** READ# output low enables data transfer from the selected device to the D0-D7 lines.
WRITE#	118	O	It/Ot2	**Write Enable.** WRITE# output low enables data transfer from the D0-D7 lines to the selected device.
ROMSEL# (PB2)	102	O	Ot2	**ROM Select**. ROMSEL# (PB2, ES3) output low selects the external ROM/flash ROM.
RAMSEL# (PB3)	104	O	It/Ot2	**RAM Select.** RAMSEL#, PB3 (ES2) output low selects the external RAM.
RESERVED (PB1)	101	O	It/Ot2	**Reserved.** PB1 (ES4) is used internally. Leave open.
EXT_RES# (PB6)	107	O	It/Ot2	**External Device Reset.** Active low reset for external devices. Leave open if not used.
CX20437 VC Interface				
IASLEEP (P_PF05)	50	O	Ot2	**Modem Sleep.** Connect to VC SLEEP pin.
M_CLK (P_PB00)	37	O	It/Ot2	**Master Clock Output**. Connect to VC M_CLKIN pin.
SR2CLK (P_PGP05)	92	I	Itpu/Ot2	**Voice Serial Clock input.** Connect to VC M_SCK pin.
SA2CLK (P_PX05)	38	I	Itpu/Ot2	**Voice Serial Frame Sync Input.** Connect to VC M_STROBE pin.
SR3OUT	35	O	Ot2	**Voice Serial Transmit Data Output.** Connect to VC M_TXSIN pin.
SR3IN (P_PX01)	36	I	Itk/Ot2	**Voice Serial Receive Data Input.** Connect to VC M_RXOUT pin.
SR2IO (P_PX06)	39	O	It/Ot2	**Voice Control Output.** Connect to VC M_CNTRLSIN pin.

Table 3-4. CX88168 SCM Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
V.24 (EIA/TIA-232-E) DTE Serial Interface				
These signals correspond functionally to V.24/EIA/TIA-232-E signals but are logically inverted.				
TXD# (PA2)	27	I	It/Ot2	**Transmitted Data (EIA BA/ITU-T CT103).** The DTE uses the TXD# line to send data to the modem for transmission over the telephone line or to transmit commands to the modem.
RXD# (PA6)	32	O	It/Ot2	**Received Data (EIA BB/ITU-T CT104).** The modem uses the RXD# line to send data received from the telephone line to the DTE and to send modem responses to the DTE. During command mode, RXD# data represents the modem responses to the DTE.
CTS# (PC1)	123	O	Ith/Ot8	**Clear To Send (EIA CB/ITU-T CT106).** CTS# output ON (low) indicates that the modem is ready to accept data from the DTE. In asynchronous operation, in error correction or normal mode, CTS# is always ON (low) unless RTS/CTS flow control is selected by the &Kn command. In synchronous operation, the modem also holds CTS# ON during asynchronous command state. The modem turns CTS# OFF immediately upon going off-hook and holds CTS# OFF until both DSR# and RLSD# are ON and the modem is ready to transmit and receive synchronous data. The modem can also be commanded by the &Rn command to turn CTS# ON in response to an RTS# OFF-to-ON transition.
DSR# (PC0)	122	O	Ith/Ot8	**Data Set Ready (EIA CC/ITU-T CT107).** DSR# indicates modem status to the DTE. DSR# OFF (high) indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (RI#). DSR# output is controlled by the AT&Sn command.
RLSD# (PC2)	125	O	Ith/Ot8	**Received Line Signal Detector (EIA CF/ITU-T CT109).** When AT&C0 command is not in effect, RLSD# output is ON when a carrier is detected on the telephone line or OFF when carrier is not detected.
TM# (PC6)	3	O	Ith/Ot8	**Test Mode (EIA TM/ITU-T CT142).** The TM# output indicates the modem is in test mode (low) or in any other mode (high).
RI# (PC5)	1	O	Ith/Ot8	**Ring Indicator (EIA CE/ITU-T CT125).** RI# output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line.
DTR# (PD4)	11	I	It	**Data Terminal Ready (EIA CD/ITU-T CT108).** The DTR# input is turned ON (low) by the DTE when the DTE is ready to transmit or receive data. DTR# ON prepares the modem to be connected to the telephone line, and maintains the connection established by the DTE (manual answering) or internally (automatic answering). DTR# OFF places the modem in the disconnect state under control of the &Dn and &Qn commands.
RTS# (PD6)	13	I	Ithpu	**Request To Send (EIA CA/ITU-T CT105).** RTS# input ON (low) indicates that the DTE is ready to send data to the modem. In the command state, the modem ignores RTS#. In asynchronous operation, the modem ignores RTS# unless RTS/CTS flow control is selected by the &Kn command. In synchronous on-line operation, the modem can be commanded by the &Rn command to ignore RTS# or to respond to RTS# by turning on CTS# after the delay specified by Register S26.

Table 3-4. CX88168 SCM Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
LED Indicator Interface				
AAIND# (PC4)	127	O	Ith/Ot8	**Auto Answer Indicator.** AAIND# output ON (low) corresponds to the indicator on. AAIND# output is active when the modem is configured to answer the ring automatically (ATS0 command ≠ 0).
TMIND# (PB7)	109	O	It/Ot8	**Test Mode Indicator.** TMIND# output ON (low) corresponds to the indicator on. TMIND# output pulses (indicator flashes) when the modem is in test mode and if an error is detected.
DTRIND# (PD0)	6	O	Ithpd/Ot2	**DTR Indicator.** DTRIND# output ON (low) corresponds to the indicator on. The DTRIND# state reflects the DTR# output state except when the &D0 command is active, in which case DTRIND# is low.
OHIND#/RXPAD# (PE0)	14	O	It/Ot8	**Cellular RX Bias.** In Line Mode (LINE/CELL = high), OHIND#/RXPAD# (PE0) indicates the status of the off-hook relay. In Cell Mode (LINE/CELL = low), this signal is defined by the cellular firmware driver.
Telephone Line/Analog Cellular Phone Interface Select				
LINE/GSM (PA5)	31	I	It/Ot2	**Line/GSM Interface Select.** Not used. Leave open.
LINE/CELL (PE7)	23	I	It/Ot8	**Line/Cellar Interface Select.** Selects telephone line or cellular phone (AMPS) interface, as follows: **LINE/CELL** — **Interface Selected** H — Telephone Line L — Cellular (AMPS) The following ports operate as indicated for the selected interface: **Port*** — **Telephone Line** — **Analog Cellular** PE0 — OHIND# — RXPAD# PE1 — — — TXPAD# PE2 — — — CELBSY PE5 — — — CELDATA PA2 — — — — PA3 — — — CELBSY# PA4 — — — CELCLK PA6 — — — GSMTXD * Ports marked "—" are not used.
Analog Cellular Phone Interface (LINE/CELL = Low)				
CELCLK/GSMINP0 (PA4)	29	I	Itpu/Ot2	**Cellular Clock.** Defined by the cellular firmware driver.
CELDATA (PE5)	21	I/O	It/Ot2	**Cellular Data**. Defined by the cellular firmware driver.
CELBSY (PE2)	17	O	It/Ot2	**Cellular Busy.** Defined by the cellular firmware driver.
CELBSY# (PA3)	28	I	Itpu/Ot2	**Cellular Not Busy.** Defined by the cellular firmware driver.
OHIND#/RXPAD# (PE0)	14	O	It/Ot8	**Cellular RX Bias.** In Line Mode (LINE/CELL = high), OHIND#/RXPAD# (PE0) indicates the status of the off-hook relay. In Cell Mode (LINE/CELL = low), this signal is defined by the cellular firmware driver.
VOICE#/TXPAD# (PE1)	16	O	It/Ot2	**Cellular TX Bias.** Defined by the cellular firmware driver.
Telephone Interface (LINE/CELL = High and LINE/GSM = High)				
VOICE#/TXPAD# (PE1)	16	O	It/Ot2	**Voice Relay Control.** When the LINE/CELL input is high, this output (typically active low) used to control the normally open voice relay. See cellular interface signals for TXPAD# usage.
HS_LCS (PE4)	19	I	It/Ot2	**Handset Line Current Sense.** LCS is an active high input that indicates a handset off-hook status. Not required for data/fax/voice/speakerphone operation. If not used, connect to GND through 47 KΩ.

Table 3-4. CX88168 SCM Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
Not Used				
RESERVED (PC7)	4	I	Ith/Ot8	**Reserved**. Connect to +3.3V through 47 KΩ.
RESERVED (PD5)	12	I	Ithpu	**Reserved**. Leave open.
NOXYCK	47	I	Itpu	**Disable XCLK Output**. When low, disables XCLK output (reduces internal power consumption). When high, enables XCLK output. Connect to GND.
TESTP	110	I	Itpu	**Test.** Used for factory test only. Leave open.
DV1TP	111	I	Itpu	**Test.** Used for factory test only. Leave open.
XCLK	49	O	It/Ot2	**Not Used.** Leave open.
S4RIN	45	I	Itk	**Not Used.** Leave open.
PHS2	121	O	Ot2	**Not Used.** Leave open.
PC3	126	I/O	Ith/Ot8	**Not Used.** Leave open.
PD1	7	I/O	Ithpd/Ot2	**Not Used.** Leave open.
PD2	8	I/O	Ithpd/Ot2	**Not Used.** Leave open.
PD7	46	I/O	It/Ot2	**Not Used.** Leave open.
P_PX00	41	I/O	It/Ot8	**Not Used.** Leave open.
P_PX02	42	I/O	Itpu/Ot2	**Not Used.** Leave open.
P_PX03	43	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (GP00)	52	I/O	It/Ot2	**Not Used.** Leave open.
RESERVED (P_PA00)	55	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (P_PA01)	57	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (P_PA04)	54	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (P_PA05)	56	I/O	Itk/Ot2	**Not Used.** Leave open.
RESERVED (P_PB01)	51	I/O	Itpu/Ot2	**Not Used.** Leave open.
RESERVED (P_BD2CLK)	59	I/O	Itpu/Ot2	**Not Used.** Leave open.

Notes:
1. I/O Types: See Table 3-5.
2. Interface Legend:
   - DIB Digital Isolation Barrier
   - EB Expansion Bus
   - HB Host Bus
   - NC No internal pin connection
   - VC Voice Codec

   RESERVED = No external connection allowed (may have internal connection).

Table 3-5. CX88168 SCM I/O Type Definitions

I/O Type	Description
Idd/Odd	Digital input/output, DIB data transceiver
Ix/Ox	I/O, wire
It/Ot2	Digital input, +5V tolerant/ Digital output, 2 mA, Z_{INT} = 120 Ω
Itk/Ot2	Digital input, +5V tolerant, keeper/ Digital output, 2 mA, Z_{INT} = 120 Ω
Itpu/Ot2	Digital input, +5V tolerant, 75k Ω pull up/ Digital output, 2 mA, Z_{INT} = 120 Ω
It/Ot8	Digital input, +5V tolerant,/ Digital output, 8 mA, Z_{INT} = 50 Ω
Ithpd/Ot2	Digital input, +5V tolerant, hysteresis, 75k Ω pull down/ Digital output, 2 mA, Z_{INT} = 120 Ω
Ith/Ot2	Digital input, +5V tolerant, hysteresis/Digital output, 2 mA, Z_{INT} = 120 Ω
Ith/Ot8	Digital input, +5V tolerant, hysteresis/Digital output, 8 mA, Z_{INT} = 50 Ω
It	Digital input, +5V tolerant
Itk	Digital input, +5V tolerant, keeper
Itkpu	Digital input, +5V tolerant, keeper, 75k Ω pull up
Itpu	Digital input, +5V tolerant, 75k Ω pull up
Ithpu	Digital input, +5V tolerant, hysteresis, 75k Ω pull up
Odpc	Digital output with adjustable drive, DIB clock and power
Ot2	Digital output, three-state, 2 mA, Z_{INT} = 120 Ω
PWR	VCC Power
PWRG	VGG Power
GND	Ground

NOTES:

1. See DC characteristics in Table 3-6.
2. I/O Type corresponds to the device Pad Type. The I/O column in signal interface tables refers to signal I/O direction used in the application.

Table 3-6. CX88168 SCM DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	VIL					
+5V tolerant		0	–	0.8	V	
+5V tolerant hysteresis		0	–	0.3 *VGG	V	
Input Voltage High	VIH		–		V	
+5V tolerant		2	–	5.25	V	
+5V tolerant hysteresis		0.7 * VDD	–	5.25	V	
Input Hysteresis	VH		–		V	
+3V hysteresis		0.5	–		V	
+5V tolerant, hysteresis		0.3	–		V	
Output Voltage Low	VOL					
Z_{INT} = 120 Ω		0	–	0.4	V	IOL = 2 mA
Z_{INT} = 50 Ω		0	–	0.4	V	IOL = 8 mA
Output Voltage High	VOH		–		V	
Z_{INT} = 120 Ω		2.4	–	VDD	V	IOL = -2 mA
Z_{INT} = 50 Ω		2.4	–	VDD	V	IOL = -8 mA
Pull-Up Resistance	Rpu	50	–	200	kΩ	
Pull-Down Resistance	Rpd	50	–	200	kΩ	

Test conditions unless otherwise noted:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF.

3.2 CX20463 SmartDAA LSD Hardware Pins and Signals

3.2.1 General

3.2.2 SCM Interface (Through DIB)

The DIB interface signals are:

- Clock (CLK); input
- Digital Power (PWR+); input power
- Digital Ground (DGND); digital ground
- Data Positive (DIB_P); input
- Data Negative (DIB_N); input

3.2.3 Telephone Line Interface

The telephone line interface signals are:

- RING AC Coupled (RAC1); input
- TIP AC Coupled (TAC1); input
- Electronic Inductor Resistor (EIR); output
- TIP and RING DC Measurement (TRDC); input
- DAC Output Voltage (DAC); output
- Electronic Inductor Capacitor (EIC)
- Electronic Inductor Output (EIO)
- Electronic Inductor Feedback (EIF)
- Resistive Divider Midpoint (DCF)
- Transmit Analog Output (TXA); output
- Receive Analog Input (RXI); input
- Receiver Gain (RXG); output
- MOV Enable (MOVEN); output
- Worldwide Impedance 0 (ZW0); input
- US Impedance 0 (ZUS0); input
- Transmit Feedback (TXF); input
- Transmit Output (TXO); output

3.2.4 CX20463 LSD Pin Assignments and Signal Definitions

LSD 32-pin TQFP hardware interface signals are shown by major interface in Figure 3-5, are shown by pin number in Figure 3-6, and are listed by pin number in Table 3-7.

LSD pin signals are defined in Table 3-8.

LSD pin signal digital electrical characteristics are defined in Table 3-9.

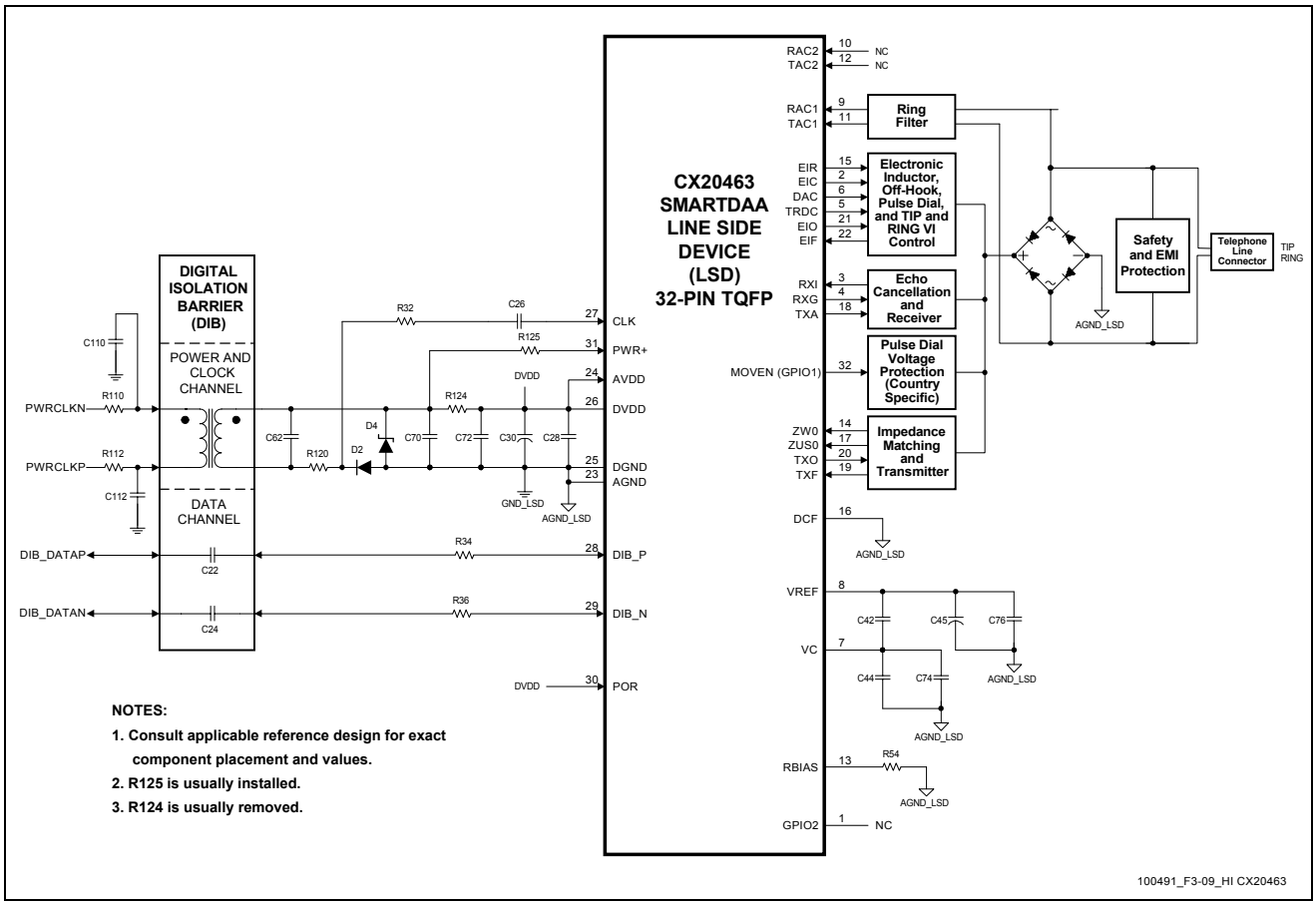


Figure 3-5. CX20463 LSD Hardware Interface Signals

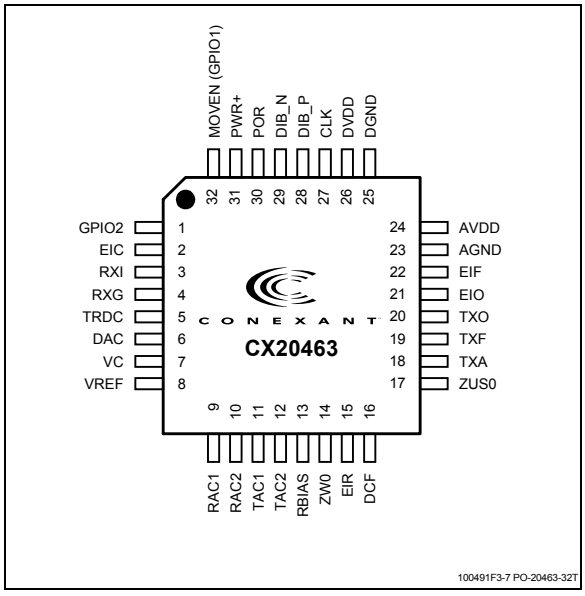


Figure 3-6. CX20463 LSD 32-Pin TQFP Pin Signals

Table 3-7. CX20463 LSD 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface
1	GPIO2	It/Ot12	NC
2	EIC	Oa	Telephone Line Interface Components
3	RXI	Ia	Telephone Line Interface Components
4	RXG	Oa	Telephone Line Interface Components
5	TRDC	Oa	Telephone Line Interface Components
6	DAC	Oa	Telephone Line Interface Components
7	VC	REF	VREF through C42 and to AGND_LSD through C44 and C74
8	VREF	REF	VC through C42 and to AGND_LSD through C45 and C76
9	RAC1	Ia	Diode bridge top AC connection (RING) through R2 and C2
10	RAC2	Ia	NC
11	TAC1	Ia	Diode bridge bottom AC connection (TIP) through R4 and C4
12	TAC2	Ia	NC
13	RBIAS	Ia	AGND_LSD through R54
14	ZW0	Ia	Telephone Line Interface Components
15	EIR	Ot12	Telephone Line Interface Components
16	DCF	Ia	AGND_LSD
17	ZUS0	Ia	Telephone Line Interface Components
18	TXA	Oa	Telephone Line Interface Components
19	TXF	Ia	Telephone Line Interface Components
20	TXO	Oa	Telephone Line Interface Components
21	EIO	Oa	Telephone Line Interface Components
22	EIF	Ia	Telephone Line Interface Components
23	AGND	AGND_LSD	AGND_LSD
24	AVDD	PWR	LSD DVDD pin
25	DGND	GND_LSD	DIB transformer secondary winding undotted terminal through diode D2 and R120 in series and to GND_LSD
26	DVDD	PWR	LSD AVDD pin, to GND_LSD through C28, C30, and C72 in parallel, and to DIB transformer secondary winding dotted terminal through R124.
27	CLK	I	DIB transformer secondary winding undotted terminal through C26 and R32 in series, and through R120 shared with LSD DGND pin through diode D2
28	DIB_P	I/O	DIB C22 through R34
29	DIB_N	I/O	DIB C24 through R36
30	POR	It	LSD DVDD pin
31	PWR+	PWR	DIB transformer secondary winding dotted terminal through R125 and to GND_LSD through zener diode D4 and C70 in parallel
32	MOVEN (GPIO1)	Ot12	Telephone Line Interface Components

Notes:

1. I/O types:
   - Ia — Analog input
   - It — Digital input, TTL-compatible, (See Table 3-9)
   - Oa — Analog output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω (See Table 3-9)
   - AGND_LSD — Isolated LSD Analog Ground
   - GND_LSD — Isolated LSD Digital Ground
2. Interface components may vary (see reference design for exact components and values).

Table 3-8. CX20463 LSD Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
SYSTEM SIGNALS			
AVDD	24	PWR	**Analog Power Supply.** Connect to the LSD DVDD pin.
AGND	23	AGND_LSD	**LSD Analog Ground. LSD Analog Ground.** Connect to AGND_LSD at the GND_LSD/AGND_LSD tie point and to the analog ground plane.
POR	30	It	**Power-On Reset.** Connect to LSD DVDD pin.
VREF	8	REF	**Output Reference Voltage.** Connect to VC through C42 and to AGND_LSD through C45 and C76. Ensure a very close proximity between C42 and C45 and the VREF pin.
VC	7	REF	**Output Middle Reference Voltage.** Connect to VREF through V42 and to AGND_LSD through C44 and C74. Ensure a very close proximity between C44 and the VC pin. Use a short path and a wide trace to AGND_LSD pin.
DIB INTERFACE SIGNALS			
CLK	27	I	**Clock.** Provides input clock, AC-coupled, to the LSD**.** Connect to DIB transformer secondary winding undotted terminal through R32 and C26 in series, and through R120 shared with LSD DGND pin through diode D2.
PWR+	31	PWR	**Digital Power Input**. Provides unregulated input digital power to the LSD. Connect to DIB transformer secondary winding dotted terminal through R125, and to GND_LSD though zener diode D4 and C70 in parallel.
DVDD	26	PWR	**Digital Power**. Connect to pin 24 (AVDD), to DIB transformer secondary winding dotted terminal through R124, and to GND_LSD through C28, C30, and C72 in parallel.
DGND	25	GND_LSD	**LSD Digital Ground.** Connect to DIB transformer secondary winding undotted terminal through diode D2 in series with R120, and to GND_LSD at the GND_LSD/AGND_LSD tie point.
DIB_P	28	I/O	**Data and Control Positive.** Connect to HSD DIB_DATAP through C22 in the DIB and R34 on the LSD side. DIB_P and DIB_N signals are differential, and ping-pong between DIB and HSD (half duplex).
DIB_N	29	I/O	**Data and Control Negative.** Connect to HSD DIB_DATAN through C24 in the DIB and R36 on LSD side. DIB_P and DIB_N signals are differential, and ping-pong between DIB and HSD (half duplex).
TIP AND RING INTERFACE			
RAC1, TAC1	9, 11	Ia, Ia	**RING1 AC Coupled and TIP1 AC Coupled.** AC-coupled voltage from telephone line used to detect ring. Connect RAC1 to the diode bridge AC top connection (RING) through R2 and C2. Connect TAC1 to the diode bridge AC bottom connection (TIP) through R4 and C4.
RAC2 TAC2	10, 12	Ia, Ia	**RING2 AC Coupled and TIP2 AC Coupled.** Not used. Leave open.
EIR	15	Oa	**Electronic Inductor Resistor.** Electronic inductor resistor switch.
EIC	2	Oa	**Electronic Inductor Capacitor Switch.** Internally switched to no connect when pulse dialing and to ground all other times. This is needed to eliminate pulse dial interference from the electronic inductor AC filter capacitor.
DAC	6	Oa	**DAC Output Voltage.** Output voltage of the reference DAC.
TRDC	5	Ia	**TIP and RING DC Measurement.** Input on-hook voltage (from a resistive divider). Used internally to extract TIP and RING DC voltage and Line Polarity Reversal (LPR) information.
EIO	21	Oa	**Electronic Inductor Output.** Calculated voltage is applied to this output to control offhook, pulse dial, and DC IV mask operation.
EIF	22	Ia	**Electronic Inductor Feedback.** Electronic inductor feedback.
RXG	4	Oa	**Receiver Gain.** Receiver operational amplifier output.
RXI	3	Ia	**Receive Analog Input.** Receiver operational amplifier inverting input.
TXA	18	Oa	**Transmit Analog Output.** Transmit signal used for canceling echo in the receive path.

Table 3-8. CX20463 LSD Pin Signal Definitions (Continued)

Label	Pin	I/O Type	Signal Name/Description
TELEPHONE LINE INTERFACE (CONTINUED)			
MOVEN (GPIO1)	32	Ot12	**MOV Enable**. Connect to pulse dial voltage protection circuit for Australia/Poland/Italy use. Leave open if the product is not intended for Australia, Poland, or Italy.
RBIAS	13	Ia	**Receiver Bias.** Connect to GND through R54.
DCF	16	Ia	**Resistive Divider Midpoint.** Connect to LSD analog ground.
ZW0	14	Ia	**Worldwide Impedance 0.** Input signal used to provide line complex impedance matching for worldwide countries.
ZUS0	17	Ia	**US Impedance 0.** Input signal used to provide line impedance matching for U.S.
TXO	20	Oa	**Transmit Output.** Outputs transmit signal and impedance matching signal; connect to transmitter transistor (Q6).
TXF	19	Ia	**Transmit Feedback.** Connect to emitter of transmitter transistor (Q6).
NOT USED			
GPIO2	1	It/Ot12	**General Purpose I/O 2**. Leave open if not used.

Notes:

1. I/O types:

Ia	Analog input
It	Digital input, TTL-compatible (See Table 3-9)
Oa	Analog output
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω (See Table 3-9)
AGND_LSD	Isolated LSD Analog Ground
GND_LSD	Isolated LSD Digital Ground

2. Interface components may vary (see reference design for exact components and values).

Table 3-9. CX20463 LSD DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IN}	-0.30	–	3.60	V	VDD = +3.6V
Input Voltage Low	V_{IL}	–	–	1.0	V	
Input Voltage High	V_{IH}	1.6	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.33	V	
Output Voltage High	V_{OH}	2.97	–	–	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	
GPIO Output Sink Current at 0.4 V maximum	–	2.4	–	-	mA	
GPIO Output Source Current at 2.97 V minimum	–	2.4	–	-	mA	
GPIO Rise Time/Fall Time		20		100	ns	

Test conditions unless otherwise noted:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF

3.3 CX20437 VC Hardware Pins and Signals (S Models)

3.3.1 General

Microphone and analog speaker interface signals, as well as telephone handset/headset interface signals are provided to support functions such as speakerphone mode, telephone emulation, microphone voice record, speaker voice playback, and call progress monitor.

Cellular analog transmit and receive interface signals are provided for direct connection to an analog cell phone.

Speakerphone Interface

The following signals are supported:

- Speaker Out (M_SPKR_OUT); analog output - Should be used in speakerphone designs where sound quality is important
- Microphone (M_MIC_IN); analog input

Telephone Handset/Headset Interface (In Lieu of Analog Cellular Connection)

The following interface signals are supported:

- Telephone Input (M_LINE_IN), input (TELIN) - Optional connection to a telephone handset interface circuit
- Telephone output (M_LINE_OUTP); output (TELOUT) - Optional connection to a telephone handset interface circuit
- Center Voltage (VC); output reference voltage

Analog Cellular Phone Interface (In Lieu of Telephone Handset/Headset Connection)

The following interface signals are supported:

- Cellular Analog Transmit (CEL_TX), output - Optional connection to an analog cell phone
- Cellular Analog Receive (CEL_RX), input - Optional connection to an analog cell phone

SCM Interface

The following interface signals are supported:

- Sleep (SLEEP); input
- Master Clock (M_CLKIN); input
- Serial Clock (M_SCK); output
- Control (M_CNTRLSIN); input
- Serial Frame Sync (M_STROBE); output
- Serial Transmit Data (M_TXSIN); input
- Serial Receive Data (M_RXOUT); output

Host Interface

The following interface signals are supported:

- Reset (POR); input

3.3.2 CX20437 VC Pin Assignments and Signal Definitions

VC 32-pin TQFP hardware interface signals are shown by major interface in Figure 3-7, are shown by pin number in Figure 3-8, and are listed by pin number in Table 3-10.

VC hardware interface signals are defined in Table 3-11.

VC pin signal DC electrical characteristics are defined in Table 3-12.

VC pin signal analog electrical characteristics are defined in Table 3-13.

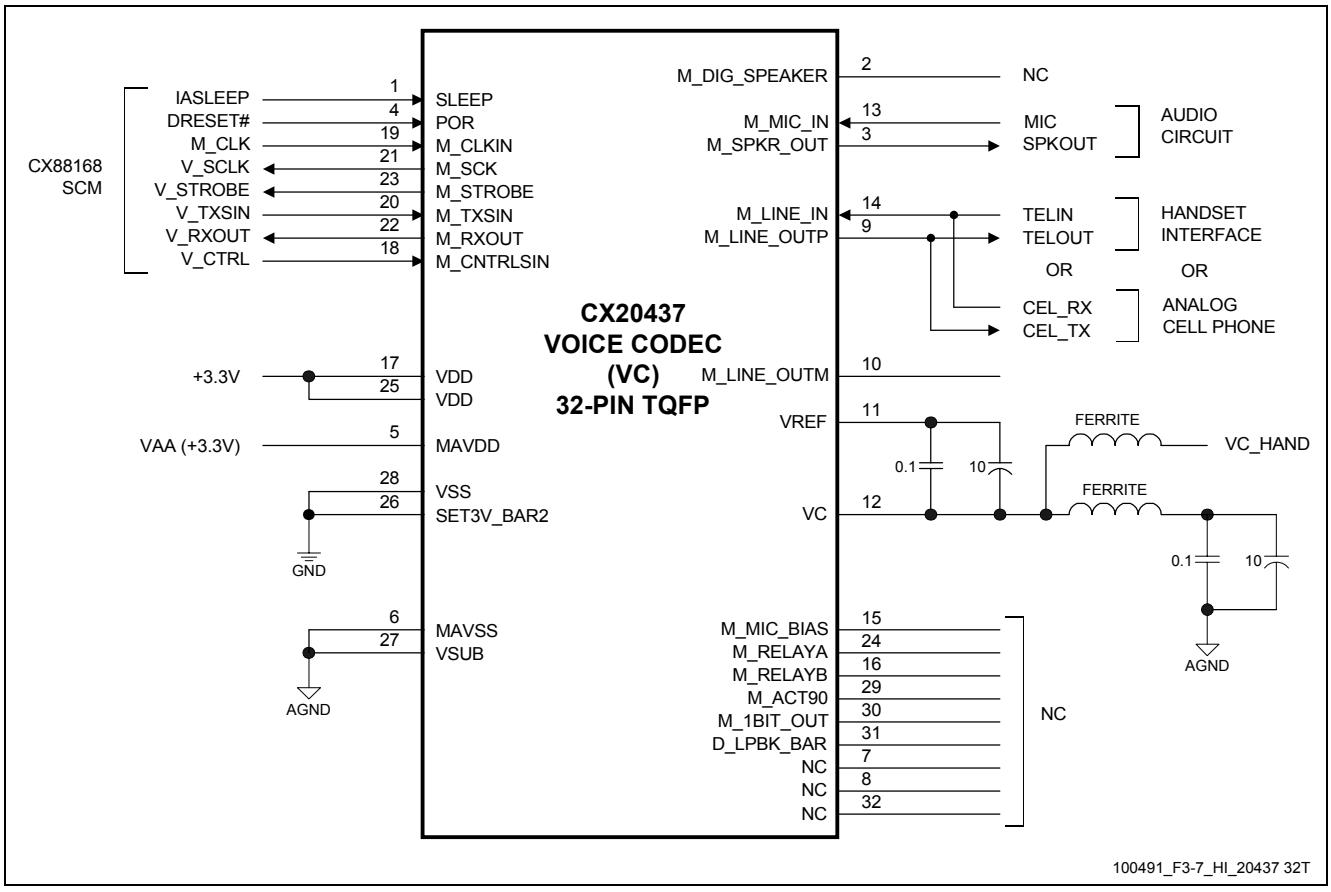


Figure 3-7. CX20437 VC Hardware Interface Signals

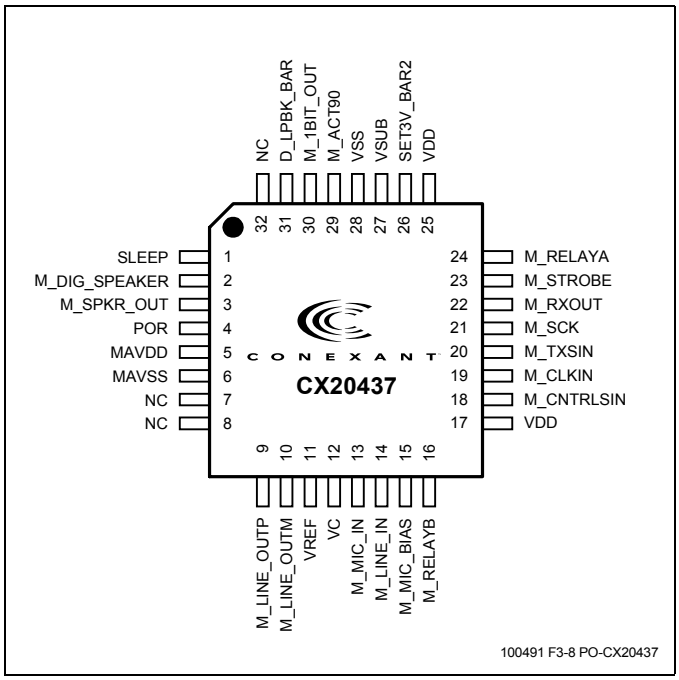


Figure 3-8. CX20437 VC 32-Pin TQFP Pin Signals

Table 3-10. CX20437 VC 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O	I/O Type	Interface
1	SLEEP	I	Itpd	SCM: IASLEEP
2	M_DIG_SPEAKER	O	Ot2	NC
3	M_SPKR_OUT	O	Oa	Speaker interface circuit
4	POR	I	Itpu	Host: RESET# or reset circuit
5	MAVDD		PWR	VAA (+3.3V)
6	MAVSS		AGND	AGND
7	NC			NC
8	NC			NC
9	M_LINE_OUTP	O	Oa	Handset interface circuit: TELOUT; or Cell Phone: CEL_TX
10	M_LINE_OUTM	O	Oa	NC
11	VREF		REF	VC through capacitors
12	VC		REF	AGND through ferrite bead and capacitors. For handset interface, connect also to VC_HAND through ferrite bead
13	M_MIC_IN	I	Ia	Microphone interface circuit
14	M_LINE_IN	I	Ia	Handset interface circuit: TELIN; or Cell Phone: CEL_RX
15	M_MIC_BIAS			NC
16	M_RELAYB			NC
17	VDD		PWR	+3.3V
18	M_CNTRLSIN	I	Itpd	SCM: V_CTRL
19	M_CLKIN	I	Itpd	SCM: M_CLK
20	M_TXSIN	I	Itpd	SCM: V_TXSIN
21	M_SCK	O	Ot2	SCM: V_SCLK
22	M_RXOUT	O	Ot2	SCM: V_RXOUT
23	M_STROBE	O	Ot2	SCM: V_STROBE
24	M_RELAYA	O	Ot2od	NC
25	VDD		PWR	+3.3V
26	M_SET3V_BAR2	I	Itpu	GND
27	VSUB		AGND	AGND
28	VSS		GND	GND
29	M_ACT90	I	Itpu	NC
30	M_1BIT_OUT	O	Ot2	NC
31	D_LPBK_BAR	I	Itpu	NC
32	NC			NC

Notes:

1. I/O types:

Ia	Analog input
It	Digital input, TTL-compatible
Itpd	Digital input, TTL-compatible, internal 75k $\pm$ 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k $\pm$ 25k Ω pull-up
Oa	Analog output
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot2od	Digital output, TTL-compatible, 2 mA, open drain, $Z_{INTERNAL}$ = 120 Ω
AGND	Analog Ground
GND	Digital Ground

*See CX20437 VC DC Electrical Characteristics (Table 3-12) and CX20437 VC Analog Electrical Characteristics Table 3-13.

Table 3-11. CX20437 VC Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
SYSTEM SIGNALS			
VDD	17, 25	PWR	**Digital Power Supply.** Connect to +3.3V and digital circuits power supply filter.
MAVDD	5	PWR	**Analog Power Supply.** Connect to +3.3V and analog circuits power supply filter.
VSS	28	GND	**Digital Ground.** Connect to GND.
MAVSS	6	AGND	**Analog Ground.** Connect to AGND.
VSUB	27	GND	**Analog Ground.** Connect to AGND.
POR	4	Itpu	**Power-On Reset.** Active low reset input. Connect to Host RESET# or reset circuit.
SET3V_BAR2	26	Itpu	**Set +3.3V Analog Reference.** Connect to GND.
SCM INTERCONNECT			
SLEEP	1	Itpd	**IA Sleep.** Active high sleep input. Connect to SCM IASLEEP pin.
M_CLKIN	19	Itpd	**Master Clock Input**. Connect to SCM M_CLK pin.
M_SCK	21	Ot2	**Serial Clock Output.** Connect to SCM V_SCLK pin.
M_CNTRL_SIN	18	Itpd	**Control Input.** Connect to SCM V_CTRL pin.
M_STROBE	23	Ot2	**Serial Frame Sync.** Connect to SCM V_STROBE pin.
M_TXSIN	20	Itpd	**Serial Transmit Data.** Connect to SCM V_TXSIN pin.
M_RXOUT	22	Ot2	**Serial Receive Data.** Connect to SCM V_RXOUT pin.
MICROPHONE/SPEAKER INTERFACE			
M_MIC_IN	13	I(DA)	**Microphone Input.** Single-ended analog input from the microphone circuit.
M_SPKR_OUT	3	O(DF)	**Modem Speaker Analog Output.** The M_SPKR_OUT analog output reflects the received analog input signal. The M_SPKR_OUT on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the M_SPKR_OUT output is clamped to the voltage at the VC pin. The M_SPKR_OUT output can drive an impedance as low as 300 ohms. In a typical application, the M_SPKR_OUT output is an input to an external LM386 audio power amplifier.
HANDSET/HEADSET INTERFACE (IN LIEU OF CELL PHONE CONNECTION)			
M_LINE_OUTP	9	O(DF)	**Telephone Handset Out (TELOUT).** Single-ended analog data output to the telephone handset circuit. The output can drive a 300 Ω load.
M_LINE_IN	14	I(DA)	**Telephone Handset Out (TELIN).** Single-ended analog data input from the telephone handset circuit.
CELL PHONE INTERFACE (IN LIEU OF HANDSET/HEADSET CONNECTION)			
M_LINE_OUTP	9	O(DF)	**Cellular Transmit (CEL_TX).** Single-ended analog transmit output. Connect to the analog cell phone transmit input. The output can drive a 300 Ω load. Leave open if not used.
M_LINE_IN	14	I(DA)	**Cellular Receive (CEL_RX).** Single-ended analog receive input. Connect to the analog cell phone receive output. Connect to AGND if not used.
REFERENCE VOLTAGE			
VREF	11	REF	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VREF pin.
VC	12	REF	**Low Voltage Reference.** Connect to analog ground through ferrite bead in series with 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VC pin. Use a short path and a wide trace to AGND pin. For handset interface, also connect to handset interface circuit (VC_HAND) through a ferrite bead.

Table 3-11. CX20437 VC Pin Signal Definitions (Continued)

Label	Pin	I/O Type	Signal Name/Description
NOT USED			
M_DIG_SPEAKER	2	Ot2	**Not Used.** Leave open.
M_LINE_OUTM	10	Oa	**Not Used.** Leave open.
M_RELAYA	24	Ot	**Not Used.** Leave open.
M_RELAYB	16	Ot	**Not Used.** Leave open.
M_MIC_BIAS	15	Oa	**Not Used.** Leave open.
M_ACT90	29	Itpu	**Not Used.** Leave open.
M_1BIT_OUT	30	Ot2	**Not Used.** Leave open.
D_LPBK_BAR	31	It	**Not Used.** Leave open.
NC	7, 8, 32	NC	**Internal No Connect.** Leave open.

Notes:

1. I/O types*:

Ia	Analog input
It	Digital input, TTL-compatible
Itpd	Digital input, TTL-compatible, internal 75k $\pm$ 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k $\pm$ 25k Ω pull-up
Oa	Analog output
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot2od	Digital output, TTL-compatible, 2 mA, open drain, $Z_{INTERNAL}$ = 120 Ω
AGND	Analog Ground
GND	Digital Ground

Table 3-12. CX20437 VC DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IN}	-0.30	–	VDD+0.3	V	
Input Voltage Low	V_{IL}	-0.30	–	VDD+0.3	V	
Input Voltage High	V_{IH}	0.4*VDD	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.4	V	
Output Voltage High	V_{OH}	0.8*VDD	–	VDD	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	
Test conditions unless otherwise noted: 1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF						

Table 3-13. CX20437 VC Analog Electrical Characteristics

Signal Name	Type	Characteristic	Value
M_LINE_IN, M_MIC_IN	I (DA)	Input Impedance AC Input Voltage Range Reference Voltage	> 70K Ω 1.1 VP-P +1.35 VDC
M_LINE_OUTP	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance AC Output Voltage Range Reference Voltage DC Offset Voltage	300 Ω 0 µF 10 Ω 1.4 VP-P (with reference to ground and a 600 Ω load) +1.35 VDC ± 200 mV
M_SPKR_OUT	O (DF)	Minimum Load Maximum Capacitive Load Output Impedance AC Output Voltage Range Reference Voltage DC Offset Voltage	300 Ω 0.01 µF 10 Ω 1.4 VP-P +1.35 VDC ± 20 mV
Test conditions unless otherwise noted: 1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; MAVDD = +3.3 ± 0.3 VDC, TA = 0°C to 70°C			

Parameter	Min	Typ	Max	Units
DAC to Line Driver output (600Ω load, 3dB in SCF and CTF) SNR/SDR at: 4Vp-p differential 2Vp-p differential -10dBm differential		 88/85 82/95 72/100		dB
DAC to Speaker Driver output (150Ω load, 3dB in SCF and CTF, -6dB in speaker driver) SNR/SDR at: 2Vp-p 1Vp-p -10dBm		 88/75 82/80 72/83		dB
Line Input to ADC (6dB in AAF) SNR/SDR at –10 dBm		80/95		dB
Input Leakage Current (analog inputs)	-10		10	µA
Output Leakage Current (analog outputs)	-10		10	µA

3.4 Electrical and Environmental Specifications

3.4.1 Operating Conditions, Absolute Maximum Ratings, and Power Requirements

The operating conditions are specified in Table 3-14.

The absolute maximum ratings are listed in Table 3-15.

The current and power requirements are listed in Table 3-16.

Table 3-14. Operating Conditions

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	+3.0 to +3.6	VDC
Operating Temperature Range	T_A	0 to +70	°C

Table 3-15. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	-0.5 to +4.0	VDC
Input Voltage	V_{IN}	-0.5 to (VGG +0.5)*	VDC
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (VAA + 0.5)	VDC
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VGG +0.5)*	VDC
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	VDC
Latch-up Current (25°C)	I_{TRIG}	±400	mA
* VGG = +3.3V ± 0.3V or +5V ± 5%.			

Table 3-16. Current and Power Requirements

Mode	Typical Current (Ityp) (mA)	Maximum Current (Imax) (mA)	Typical Power (Ptyp) (mW)	Maximum Power (Pmax) (mW)	Notes
CX88168 SCM and CX20463 LSD					
Normal Mode: Off-hook, normal data connection	142	156	470	562	f = 28.224 MHz
Normal Mode: On-hook, idle, waiting for ring	132	145	436	522	f = 28.224 MHz
Sleep Mode	42	46	140	166	f = 0 MHz
CX20437 VC (Optional)					
Normal Mode	1.5	2	5	7	

Notes:
1. Operating voltage: VDD = +3.3V ± 0.3V.
2. Test conditions: VDD = +3.3V for typical values; VDD = +3.6V for maximum values.
3. Input Ripple ≤ 0.1 Vpeak-peak.
4. f = Internal frequency.
5. Maximum current computed from Ityp: Imax = Ityp * 1.1.
6. Typical power (Ptyp) computed from Ityp: Ptyp = Ityp * 3.3V; Max power (Pmax) computed from Imax: Pmax = Imax * 3.6V.

3.4.2 Interface and Timing Waveforms

External Memory Bus Timing

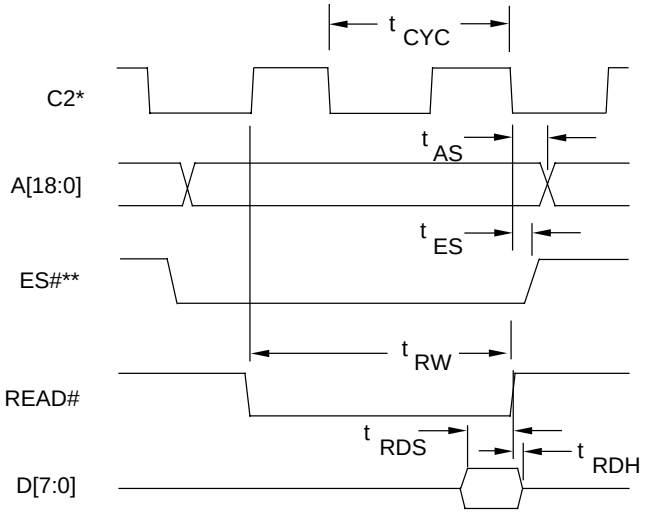
The external memory bus timing is listed in Table 3-17 and illustrated in Figure 3-9.

Table 3-17. Timing - External Memory Bus

Symbol	Parameter	Min	Typ.	Max	Units
t_{FI}	Internal Operating Frequency	28.224			MHz
t_{CYC}	Internal Operating Clock Cycle	35.43			ns
Read					
t_{AS}	READ# High to Address Valid	–	6.5	9	ns
t_{ES}	READ# High to ES Valid	–	8	11	ns
t_{RW}	READ# Pulse Width	17.72	–	–	ns
t_{RDS}	Read Data Valid to READ# High	6.1	–	–	ns
t_{RDH}	READ# High to Read Data Hold	0	0	–	ns
Write					
t_{AS}	WRITE# High to Address Valid	–	6.5	8	ns
t_{ES}	WRITE# High to ES Valid	–	8	11	ns
t_{WW}	WRITE# to WRITE# Pulse Width	17.72	–	124	ns
t_{WTD}	WRITE# Low to Write Data Valid	–	5	8.2	ns
t_{WTH}	WRITE# High to Write Data Hold	5.0	–	–	ns

Notes:

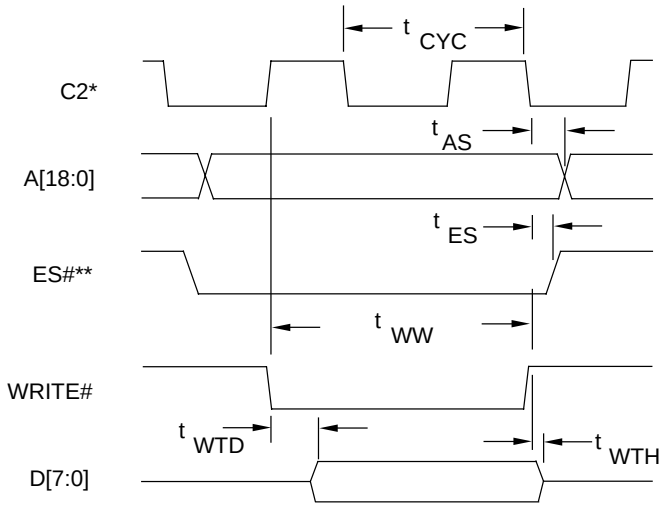
1. ES = RAMSEL# or ROMSEL#.
2. Read pulse width and write pulse width:
   RAM: t_{RW}, t_{WW} = 0.5 t_{CYC} = 17.72 ns for Non-Extended Cycle Timing
   ROM: t_{RW}, t_{WW} = 3.5 t_{CYC} = 124 ns for Extended Cycle Timing
3. Memory speed determination:
   RAM: $t_{ACCESS} = t_{CYC} - t_{ES} - t_{RDS}$ = 35.43 – 11 - 6.1 = 18.33 ns (i.e., use 15 ns memory)
   ROM: $t_{ACCESS} = 4(t_{CYC}) - t_{ES} - t_{RDS}$ = 4(35.43) – 11 - 6.1 = 124.62 ns (i.e., use 90 ns memory).
4. Output Enable to Output Delay Timing:
   RAM: $t_{OE} = t_{RW} - t_{RDS} = 0.5(t_{CYC}) - t_{RDS}$ = 17.72 - 6.1 = 11.62 ns
   ROM: $t_{OE} = t_{RW} - t_{RDS} = 3.5(t_{CYC}) - t_{RDS}$ = 124. - 6.1 = 117.90 ns.



* C2 = Internal Phase 2 clock.

** ES# = RAMSEL# or ROMSEL#.

Read Timing



* C2 = Internal Phase 2 clock.

** ES# = RAMSEL# or ROMSEL#.

Write Timing

100491 F3-09 WF EB

Figure 3-9. Waveforms - External Memory Bus

Parallel Host Bus Timing

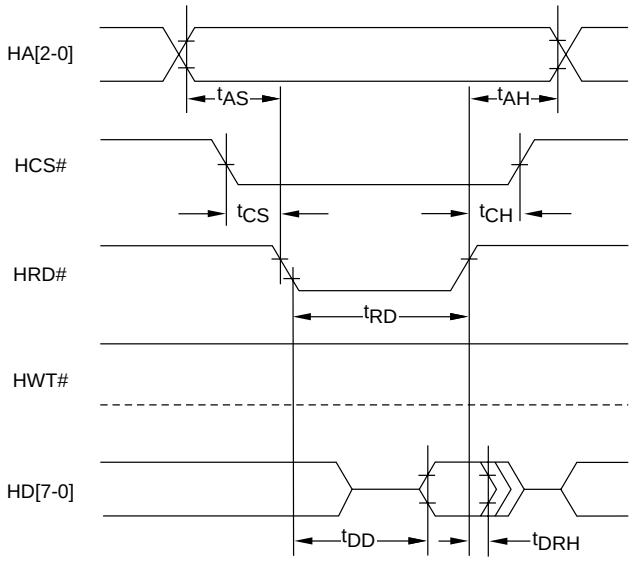
The parallel host bus timing is listed in Table 3-18 and illustrated in Figure 3-10.

Table 3-18. Timing - Parallel Host Bus

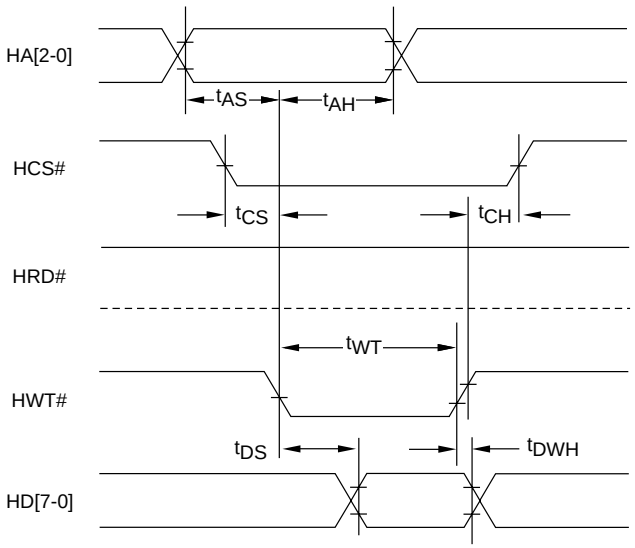
Symbol	Parameter	Min	Max	Units
	READ (See Notes 1, 2, 3, 4, 5, and 6)			
t_{AS}	Address Setup	5	–	ns
t_{AH}	Address Hold	10	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{RD}	HRD# Strobe Width	107	–	ns
t_{DD}	Read Data Delay	–	25	ns
t_{DRH}	Read Data Hold	5	–	ns
	WRITE (See Notes 1, 2, 3, 4, 5, and 6)			
t_{AS}	Address Setup	5	–	ns
t_{AH}	Address Hold	15	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{WT}	HWT# Strobe Width	178	–	ns
t_{DS}	Write Data Setup (see Note 4)	–	61	ns
t_{DWH}	Write Data Hold (see Note 5)	5	–	ns

Notes:

1. When the host executes consecutive Rx FIFO reads, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (85.86 ns at 28.224 MHz) is required from the falling edge of HRD# to the falling edge of the next Host Rx FIFO HRD# clock.
2. When the Host executes consecutive Tx FIFO writes, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (85.86 ns at 28.224 MHz) is required from the falling edge of HWT# to the falling edge of the next Host Tx FIFO HWT# clock.
3. t_{RD}, $t_{WT} = t_{CYC} + 15$ ns.
4. t_{DS} is measured from the point at which both HCS# and HWT# are active.
5. t_{DWH} is measured from the point at which either HCS# and HWT# become inactive.
6. Clock frequency = 28.224 MHz clock.



a. Host Read



b. Host Write

100491 F3-10 WF-HB

Figure 3-10. Waveforms - Parallel Host Bus

Serial DTE Interface

The serial DTE interface waveforms for 4800 and 9600 bps are illustrated in Figure 3-11.

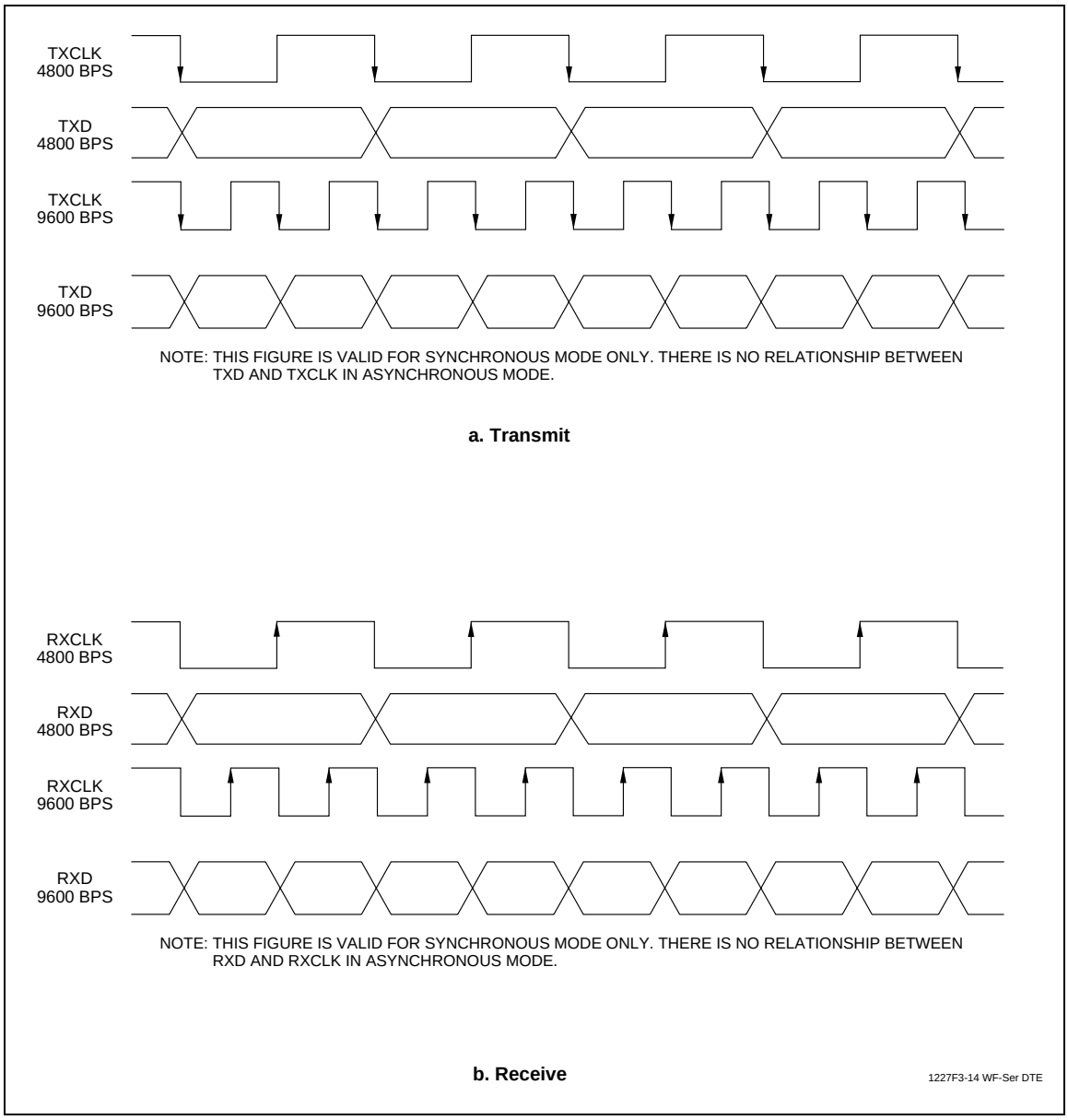


Figure 3-11. Waveforms - Serial DTE Interface

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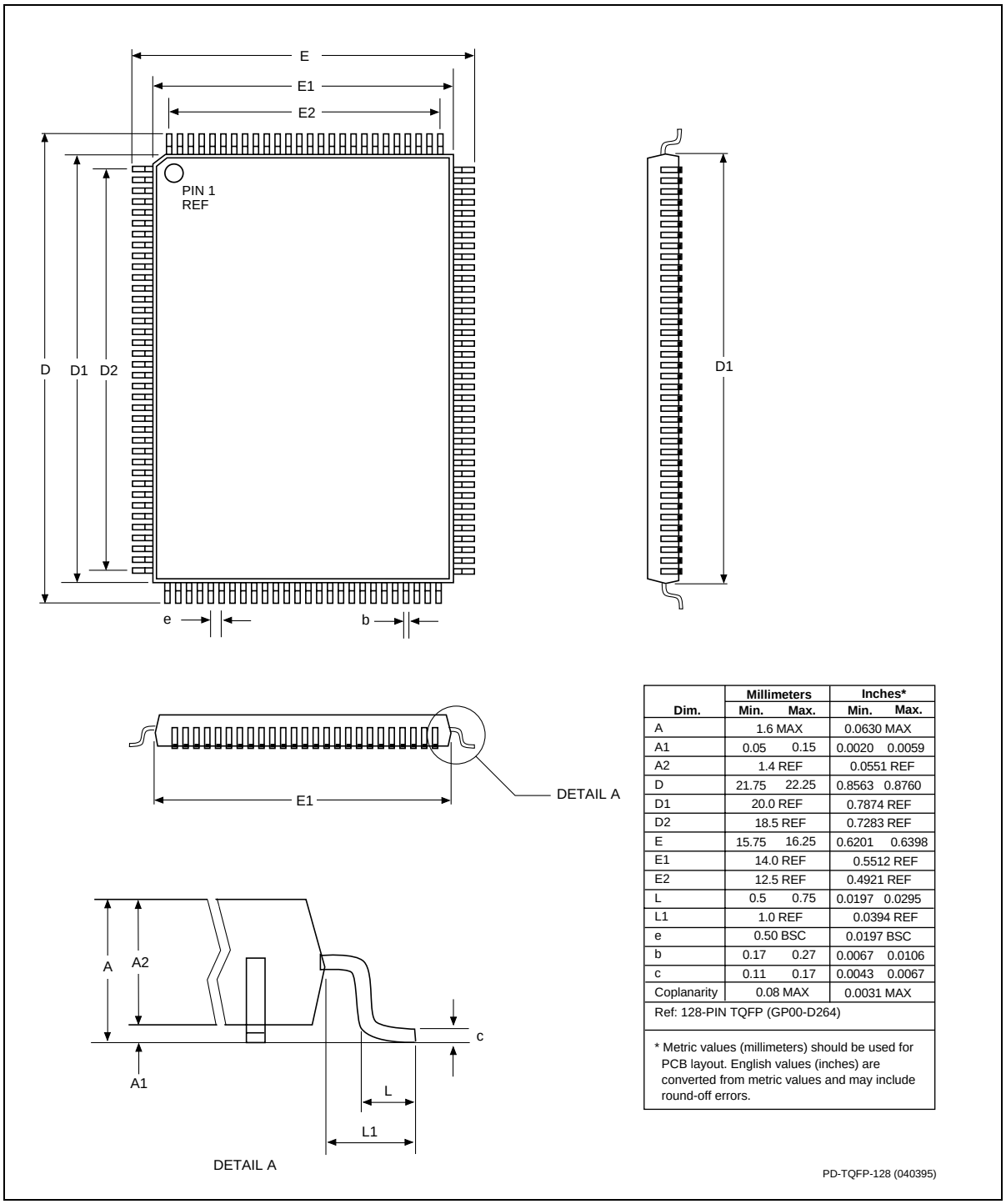
4 PACKAGE DIMENSIONS

The 128-pin TQFP package dimensions are shown in Figure 4-1.

The 32-pin TQFP package dimensions are shown in Figure 4-2.

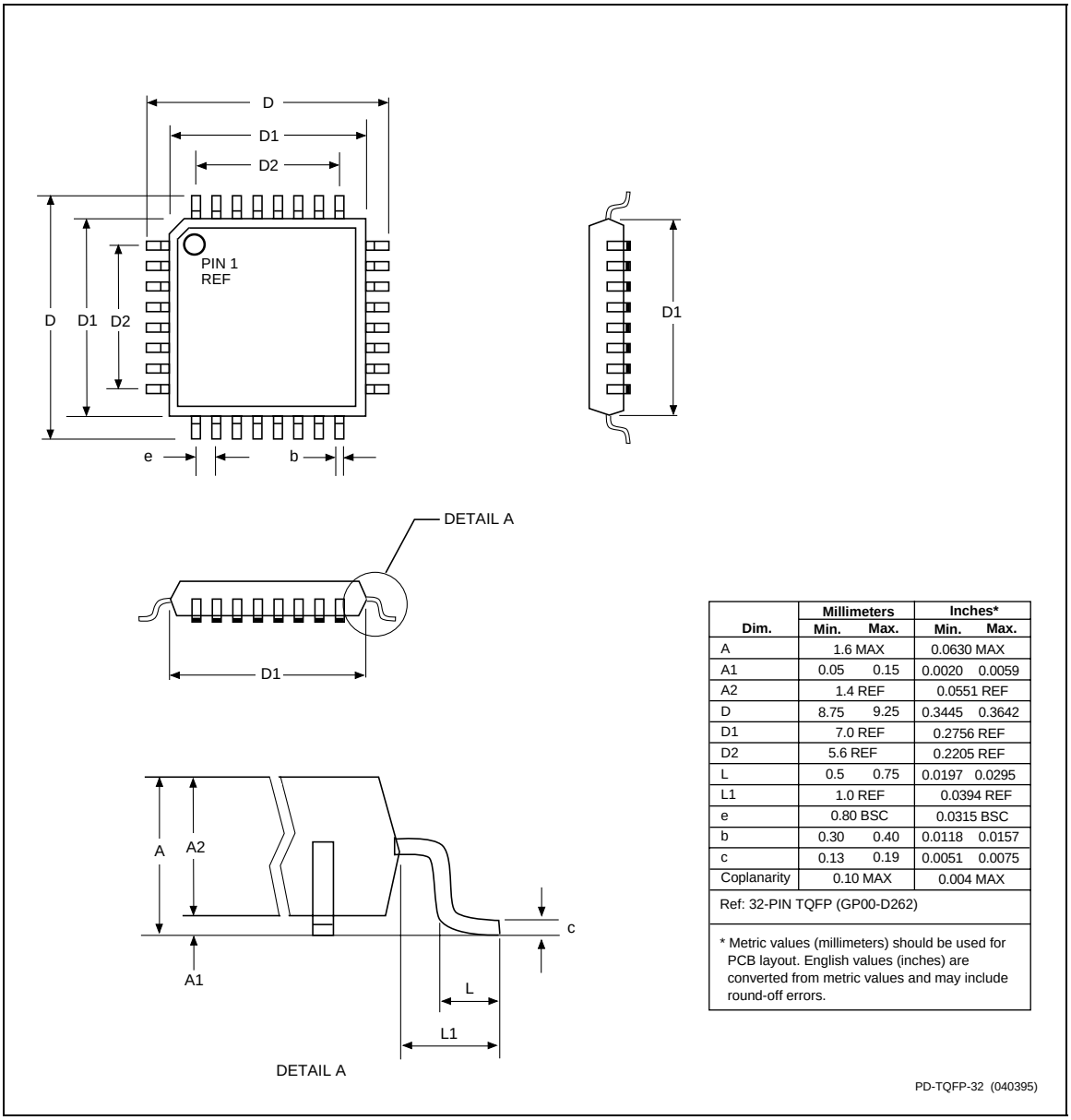


Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	21.75	22.25	0.8563	0.8760
D1		20.0 REF		0.7874 REF
D2		18.5 REF		0.7283 REF
E	15.75	16.25	0.6201	0.6398
E1		14.0 REF		0.5512 REF
E2		12.5 REF		0.4921 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX

Ref: 128-PIN TQFP (GP00-D264)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 4-1. Package Dimensions - 128-Pin TQFP



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	8.75	9.25	0.3445	0.3642
D1	7.0 REF		0.2756 REF	
D2	5.6 REF		0.2205 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX		0.004 MAX	

Ref: 32-PIN TQFP (GP00-D262)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 4-2. Package Dimensions - 32-pin TQFP

5 PARALLEL HOST INTERFACE

The modem supports a 16550A interface in parallel interface versions. The 16550A interface can operate in FIFO mode or non-FIFO mode. Non-FIFO mode is the same as 16450 interface operation. FIFO mode unique operations are identified.

5.1 Overview

The parallel interface registers and the corresponding bit assignments are shown in Table 5-1.

The modem emulates the 16450/16550A interface and includes both a 16-byte receiver data first-in first-out buffer (RX FIFO) and a 16-byte transmit data first-in first-out buffer (TX FIFO). When FIFO mode is selected in the FIFO Control Register (FCR0 = 1), both FIFOs are operative. Furthermore, when FIFO mode is selected, DMA operation of the FIFO can also be selected (FCR3 = 1). When FIFO mode is not selected, operation is restricted to 16450 interface operation.

The received data is read by the host from the Receiver Buffer (RX Buffer). The RX Buffer corresponds to the Receiver Buffer Register in a 16550A device. In FIFO mode, the RX FIFO operates transparently behind the RX Buffer. Interface operation is described with reference to the RX Buffer in both FIFO and non-FIFO modes.

The transmit data is loaded by the host into the Transmit Buffer (TX Buffer). The TX Buffer corresponds to the Transmit Holding Register in a 16550A device. In FIFO mode, the TX FIFO operates transparently behind the TX Buffer. Interface operation is described with reference to the TX Buffer in both FIFO and non-FIFO modes.

Table 5-1. Parallel Interface Registers

Register No.	Register Name	Bit No. 7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	RX FIFO Error	Transmitter Empty (TEMT)	Transmitter Buffer Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Receiver Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	Interrupt Identify Register (IIR) (Read Only)	FIFOs Enabled	FIFOs Enabled	0	0	Pending Interrupt ID Bit 2	Pending Interrupt ID Bit 1	Pending Interrupt ID Bit 0	“0" if Interrupt Pending
2	FIFO Control Register (FCR) (Write Only)	Receiver Trigger MSB	Receiver Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
1 (DLAB = 0)	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 (DLAB = 0)	Transmitter Buffer Register (THR)	Transmitter FIFO Buffer Register (Write Only)							
0 (DLAB = 0)	Receiver Buffer Register (RBR)	Receiver FIFO Buffer Register (Read Only)							
1 (DLAB = 1)	Divisor Latch MSB Register (DLM)	Divisor Latch MSB							
0 (DLAB = 1)	Divisor Latch LSB Register (DLL)	Divisor Latch LSB							

5.2 Register Signal Definitions

5.2.1 IER - Interrupt Enable Register (Addr = 1, DLAB = 0)

The IER enables five types of interrupts that can separately assert the HINT output signal (Table 5-2). A selected interrupt can be enabled by setting the corresponding enable bit to a 1, or disabled by setting the corresponding enable bit to a 0. Disabling an interrupt in the IER prohibits setting the corresponding indication in the IIR and assertion of HINT. Disabling all interrupts (resetting IER0 - IER3 to a 0) inhibits setting of any Interrupt Identifier Register (IIR) bits and inhibits assertion of the HINT output. All other system functions operate normally, including the setting of the Line Status Register (LSR) and the Modem Status Register (MSR).

Bits 7-4 Not used.

Always 0.

Bit 3 Enable Modem Status Interrupt (EDSSI).

This bit, when a 1, enables assertion of the HINT output whenever the Delta CTS (MSR0), Delta DSR (MSR1), Delta TER (MSR2), or Delta DCD (MSR3) bit in the Modem Status Register (MSR) is a 1. This bit, when a 0, disables assertion of HINT due to setting of any of these four MSR bits.

Bit 2 Enable Receiver Line Status Interrupt (ELSI).

This bit, when a 1, enables assertion of the HINT output whenever the Overrun Error (LSR1), Parity Error (LSR2), Framing Error (LSR3), or Break Interrupt (LSR4) receiver status bit in the Line Status Register (LSR) changes state. This bit, when a 0, disables assertion of HINT due to change of the receiver LSR bits 1-4.

Bit 1 Enable Transmitter Holding Register Empty Interrupt (ETBEI).

This bit, when a 1, enables assertion of the HINT output when the Transmitter Empty bit in the Line Status Register (LSR5) is a 1. This bit, when a 0, disables assertion of HINT due to LSR5.

Bit 0 Enable Receiver Data Available Interrupt (ERBFI) and Character Timeout in FIFO Mode.

This bit, when a 1, enables assertion of the HINT output when the Receiver Data Ready bit in the Line Status Register (LSR0) is a1 or character timeout occurs in the FIFO mode. This bit, when a 0, disables assertion of HINT due to the LSR0 or character timeout.

5.2.2 FCR - FIFO Control Register (Addr = 2, Write Only)

The FCR is a write-only register used to enable FIFO mode, clear the RX FIFO and TX FIFO, enable DMA mode, and set the RX FIFO trigger level.

Bits 7-6 RX FIFO Trigger Level.

FCR7 and FCR6 set the trigger level for the RX FIFO (Receiver Data Available) interrupt.

FCR7	FCR6	RX FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bits 5-4 Not used.

Bit 3 DMA Mode Select.

When FIFO mode is selected (FCR0 = 1), FCR3 selects non-DMA operation (FCR3 = 0) or DMA operation (FCR3 = 1). When FIFO mode is not selected (FCR0 = 0), this bit is not used (the modem operates in non-DMA mode in 16450 operation).

DMA operation in FIFO mode.

RXRDY will be asserted when the number of characters in the RX FIFO is equal to or greater than the value in the RX FIFO Trigger Level (IIR0-IIR3 = 4h) or the received character timeout (IIR0-IIR3 = Ch) has occurred. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there are one or more empty (unfilled) locations in the TX FIFO. TXRDY will go inactive when the TX FIFO is completely full.

Non-DMA operation in FIFO mode.

RXRDY will be asserted when there are one or more characters in the RX FIFO. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there are no characters in the TX FIFO. TXRDY will go inactive when the first character is loaded into the TX FIFO Buffer.

Bit 2 TX FIFO Reset.

When FCR2 is a 1, all bytes in the TX FIFO are cleared. This bit is cleared automatically by the modem.

Bit 1 RX FIFO Reset.

When FCR1 is a 1, all bytes in the RX FIFO are cleared. This bit is cleared automatically by the modem.

Bit 0 FIFO Enable.

When FCR0 is a 0, 16450 mode is selected and all bits are cleared in both FIFOs. When FCR0 is a 1, FIFO mode (16550A mode) is selected and both FIFOs are enabled. FCR0 must be a 1 when other bits in the FCR are written or they will not be acted upon.

5.2.3 IIR - Interrupt Identifier Register (Addr = 2)

The Interrupt Identifier Register (IIR) identifies the existence and type of up to five prioritized pending interrupts. Four priority levels are set to assist interrupt processing in the host. The four levels, in order of decreasing priority, are: Highest: Receiver Line Status, 2: Receiver Data Available or Receiver Character Timeout, 3: TX Buffer Empty, and 4: Modem Status.

When the IIR is accessed, the modem freezes all interrupts and indicates the highest priority interrupt pending to the host. Any change occurring in interrupt conditions are not indicated until this access is complete.

Bits 7-6 FIFO Mode.

These two bits copy FCR0.

Bits 5-4 Not Used.

Always 0.

Bits 3-1 Highest Priority Pending Interrupt.

These three bits identify the highest priority pending interrupt (Table 5-2). Bit 3 is applicable only when FIFO mode is selected, otherwise bit 3 is a 0.

Bit 0 Interrupt Pending.

When this bit is a 0, an interrupt is pending; IIR bits 1-3 can be used to determine the source of the interrupt. When this bit is a1, an interrupt is not pending.

Table 5-2. Interrupt Sources and Reset Control

Interrupt Identification Register					Interrupt Set and Reset Functions		
Bit 3 (Note 1)	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error OE (LSR1), Parity Error (PE) (LSR2), Framing Error (FE) (LSR3), or Break Interrupt (BI) (LSR4)	Reading the LSR
0	1	0	0	2	Received Data Available	Received Data Available (LSR0) or RX FIFO Trigger Level (FCR6-FCR7) Reached[1]	Reading the RX Buffer or the RX FIFO drops below the Trigger Level
1	1	0	0	2	Character Time-out Indication [1]	The RX FIFO contains at least 1 character and no characters have been removed from or input to the RX FIFO during the last 4 character times.	Reading the RX Buffer
0	0	1	0	3	TX Buffer Empty	TX Buffer Empty	Reading the IIR or writing to the TX Buffer
0	0	0	0	4	Modem Status	Delta CTS (DCTS) (MSR0), Delta DSR (DDSR) (MSR1), Trailing Edge Ring Indicator (TERI) (MSR3), or Delta DCD (DCD) (MSR4)	Reading the MSR

Notes:
1. FIFO Mode only.

5.2.4 LCR - Line Control Register (Addr = 3)

The Line Control Register (LCR) specifies the format of the asynchronous data communications exchange.

Bit 7 **Divisor Latch Access Bit (DLAB).**

This bit must be set to a 1 to access the Divisor latch registers during a read or write operation. It must be reset to a 0 to access the Receiver Buffer, the Transmitter Buffer, or the Interrupt Enable Register.

Bit 6 **Set Break.**

When bit 6 is a 1, the transmit data is forced to the break condition, i.e., space (0) is sent. When bit 6 is a 0, break is not sent. The Set Break bit acts only on the transmit data and has no effect on the serial in logic.

Bit 5 **Stick Parity.**

When parity is enabled (LCR3 = 1) and stick parity is selected (LCR5 = 1), the parity bit is transmitted and checked by the receiver as a 0 if even parity is selected (LCR4 = 1) or as a 1 if odd parity is selected (LCR4 = 0). When stick parity is not selected (LCR3 = 0), parity is transmit and checked as determined by the LCR3 and LCR4 bits.

Bit 4 **Even Parity Select (EPS).**

When parity is enabled (LCR3 = 1) and stick parity is not selected (LCR5 = 0), the number of 1s transmitted or checked by the receiver in the data word bits and parity bit is either even (LCR4 = 1) or odd (LCR4 = 0).

Bit 3 **Enable Parity (PEN).**

When bit 3 is a 1, a parity bit is generated in the serial out (transmit) data stream and checked in the serial in (receive) data stream as determined by the LCR 4 and LCR5 bits. The parity bit is located between the last data bit and the first stop bit.

Bit 2 **Number of Stop Bits (STB).**

This bit specifies the number of stop bits in each serial out character. If bit 2 is a 0, one stop bit is generated regardless of word length. If bit 2 is a 1 and 5-bit word length is selected, one and one-half stop bits are generated. If bit 2 is a 1 and a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The serial in logic checks the first stop bit only, regardless of the number of stop bits selected.

Bits 1-0 **Word Length Select (WLS0 and WLS1).**

These two bits specify the number of bits in each serial in or serial out character. The encoding of bits 0 and 1 is:

Bit 1	Bit 0	Word Length
0	0	5 Bits (Not supported)
0	1	6 Bits (Not supported)
1	0	7 Bits
1	1	8 Bits

5.2.5 MCR - Modem Control Register (Addr = 4)

The Modem Control Register (MCR) controls the interface with the modem or data set.

Bit 7-5 **Not used.**

Always 0.

Bit 4 **Local Loopback.**

When this bit is set to a 1, the diagnostic mode is selected and the following occurs:

1. Data written to the Transmit Buffer is looped back to the Receiver Buffer.
2. The DTS (MCR0), RTS (MCR1), Out1 (MCR2), and Out2 (MCR3) modem control register bits are internally connected to the DSR (MSR5), CTS (MSR4), RI (MSR6), and DCD (MSR7) modem status register bits, respectively.

Bit 3 **Output 2.**

When this bit is a 1, HINT is enabled. When this bit is a 0, HINT is in the high impedance state.

Bit 2 **Output 1.**

This bit is used in local loopback (see MCR4).

Bit 1 **Request to Send (RTS).**

This bit controls the Request to Send (RTS) function. When this bit is a 1, RTS is on. When this bit is a 0, RTS is off.

Bit 0 **Data Terminal Ready (DTR).**

This bit controls the Data Terminal Ready (DTR) function. When this bit is a 1, DTR is on. When this bit is a 0, DTR is off.

5.2.6 LSR - Line Status Register (Addr = 5)

This 8-bit register provides status information to the host concerning data transfer.

Bit 7 **RX FIFO Error.**

In the 16450 mode, this bit is not used and is always 0.

In the FIFO mode, this bit is set if there are one or more characters in the RX FIFO with a parity error, framing error, or break indication detected. This bit is reset to a 0 when the host reads the LSR and none of the above conditions exist in the RX FIFO.

Bit 6 **Transmitter Empty (TEMT).**

This bit is set to a 1 whenever the TX Buffer (THR) and equivalent of the Transmitter Shift Register (TSR) are both empty. It is reset to a 0 whenever either the THR or the equivalent of the TSR contains a character.

In the FIFO mode, this bit is set to a 1 when ever the TX FIFO and the equivalent of the TSR are both empty.

Bit 5 **Transmitter Holding Register Empty (THRE) [TX Buffer Empty].**

This bit, when set, indicates that the TX Buffer is empty and the modem can accept a new character for transmission. In addition, this bit causes the modem to issue an interrupt to the host when the Transmit Holding Register Empty Interrupt Enable bit (IIR1) is set to 1. The THRE bit is set to a 1 when a character is transferred from the TX Buffer. The bit is reset to 0 when a byte is written into the TX Buffer by the host.

In the FIFO mode, this bit is set when the TX FIFO is empty; it is cleared when at least one byte is in the TX FIFO.

Bit 4 **Break Interrupt (BI).**

This bit is set to a 1 whenever the received data input is a space (logic 0) for longer than two full word lengths plus 3 bits. The BI bit is reset when the host reads the LSR.

Bit 3 **Framing Error (FE).**

This bit indicates that the received character did not have a valid stop bit. The FE bit is set to a 1 whenever the stop bit following the last data bit or parity bit is detected as a logic o (space). The FE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, the error indication is associated with the particular character in the FIFO it applies to; the FE bit is set to a 1 when this character is loaded into the RX Buffer.

Bit 2 **Parity Error (PE).**

This bit indicates that the received data character in the RX Buffer does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR4) and the Stick Parity bit (LCR5). The PE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, the error indication is associated with the particular character in the it applies to; the PE bit is set to a 1 when this character is loaded into the RX Buffer.

Bit 1 **Overrun Error (OE).**

This bit is set to a 1 whenever received data is loaded into the RX Buffer before the host has read the previous data from the RX Buffer. The OE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, if data continues to fill beyond the trigger level, an overrun condition will occur only if the RX FIFO is full and the next character has been completely received.

Bit 0 **Receiver Data Ready (DR).**

This bit is set to a 1 whenever a complete incoming character has been received and has been transferred into the RX Buffer. The DR bit is reset to a 0 when the host reads the RX Buffer.

In the FIFO mode, the DR bit is set when the number of received data bytes in the RX FIFO equals or exceeds the trigger level specified in FCR0-FCR1.

5.2.7 MSR - Modem Status Register (Addr = 6)

The Modem Status Register (MSR) reports current state and change information of the modem. Bits 4-7 supply current state and bits 0-3 supply change information. The change bits are set to a 1 whenever a control input from the modem changes state from the last MSR read by the host. Bits 0-3 are reset to 0 when the host reads the MSR or upon reset.

Whenever bits 0, 1, 2, or 3 are set to a 1, a Modem Status Interrupt (IIR0-IIR3 = 0) is generated.

Bit 7 **Data Carrier Detect (DCD).**

This bit indicates the logic state of the DCD# (RLSD#) output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the Out2 bit in the MCR (MCR3).

Bit 6 **Ring Indicator (RI).**

This bit indicates the logic state of the RI# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the Out1 bit in the MCR (MCR2).

Bit 5 **Data Set Ready (DSR).**

This bit indicates the logic state of the DSR# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the DTR bit in the MCR (MCR0).

Bit 4 **Clear to Send (CTS).**

This bit indicates the logic state of the CTS# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the RTS bit in the MCR (MCR1).

Bit 3 **Delta Data Carrier Detect (DDCD).**

This bit is set to a 1 when the DCD bit changes state since the MSR was last read by the host.

Bit 2 **Trailing Edge of Ring Indicator (TERI).**

This bit is set to a 1 when the RI bit changes from a 1 to a 0 state since the MSR was last read by the host.

Bit 1 **Delta Data Set Ready (DDSR).**

This bit is set to a 1 when the DSR bit has changed since the MSR was last read by the host.

Bit 0 **Delta Clear to Send (DCTS).**

This bit is set to a 1 when the CTS bit has changed since the MSR was last read by the host.

5.2.8 RBR - RX Buffer (Receiver Buffer Register) (Addr = 0, DLAB = 0)

The RX Buffer (RBR) is a read-only register at location 0 (with DLAB = 0). Bit 0 is the least significant bit of the data, and is the first bit received.

5.2.9 THR - TX Buffer (Transmitter Holding Register) (Addr = 0, DLAB = 0)

The TX Buffer (THR) is a write-only register at address 0 when DLAB = 0. Bit 0 is the least significant bit and the first bit sent.

5.2.10 Divisor Registers (Addr = 0 and 1, DLAB = 1)

The Divisor Latch LS (least significant byte) and Divisor Latch MS (most significant byte) are two read-write registers at locations 0 and 1 when DLAB = 1, respectively.

The baud rate is selected by loading each divisor latch with the appropriate hex value.

Programmable values corresponding to the desired baud rate are listed in Table 5-3.

5.2.11 SCR - Scratch Register (Addr = 7)

The Scratchpad Register is a read-write register at location 7. This register is not used by the modem and can be used by the host for temporary storage.

Table 5-3. Programmable Baud Rates

Divisor Latch (Hex)		Divisor (Decimal)	Baud Rate
MS	LS		
06	00	1536	75
04	17	1047	110
03	00	768	150
01	80	384	300
00	C0	192	600
00	60	96	1200
00	30	48	2400
00	18	24	4800
00	0C	12	9600
00	06	6	19200
00	04	4	28800
00	03	3	38400
00	02	2	57600
00	01	1	115200
00	00	NA	230400

5.3 Receiver FIFO Interrupt Operation

5.3.1 Receiver Data Available Interrupt

When the FIFO mode is enabled (FCR0 = 1) and receiver interrupt (RX Data Available) is enabled (IER0 = 1), receiver interrupt operation is as follows:

1. The Receiver Data Available Flag (LSR0) is set as soon as a received data character is available in the RX FIFO. LSR0 is cleared when the RX FIFO is empty.
2. The Receiver Data Available interrupt code (IIR0-IIR4 = 4h) is set whenever the number of received data bytes in the RX FIFO reaches the trigger level specified by FCR6-FCR7 bits; it is cleared whenever the number of received data bytes in the RX FIFO drops below the trigger level specified by FCR6-FCR7 bits.
3. The HINT interrupt is asserted whenever the number of received data bytes in the RX FIFO reaches the trigger level specified by FCR6-FCR7 bits. HINT interrupt is de-asserted when the number of received data bytes in the RX FIFO drops below the trigger level specified by FCR6-FCR7 bits.

5.3.2 Receiver Character Timeout Interrupts

When the FIFO mode is enabled (FCR0 = 1) and receiver interrupt (Receiver Data Available) is enabled (IER0 = 1), receiver character timeout interrupt operation is as follows:

1. A Receiver character timeout interrupt code (IIR0-IIR3 = Ch) is set if at least one received character is in the RX FIFO, the most recent received serial character was longer than four continuous character times ago (if 2 stop bits are specified, the second stop bit is included in this time period), and the most recent host read of the RX FIFO was longer than four continuous character times ago.

5.4 Transmitter FIFO Interrupt Operation

5.4.1 Transmitter Empty Interrupt

When the FIFO mode is enabled (FCR0 = 1) and transmitter interrupt (TX Buffer Empty) is enabled (IER0 = 1), transmitter interrupt operation is as follows:

1. The TX Buffer Empty interrupt code (IIR0-IIR3 = 2h) will occur when the TX Buffer is empty; it is cleared when the TX Buffer is written to (1 to 16 characters) or the IIR is read.
2. The TX Buffer Empty indications will be delayed 1 character time minus the last stop bit time whenever the following occur: THRE = 1 and there have not been at least two bytes at the same time in the TX FIFO Buffer since the last setting of THRE was set. The first transmitter interrupt after setting FCR0 will be immediate.

NOTES

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