Root [1]

Technical Sheet Only!
Please refer to the subsequent sheets for schematic

Power

File: power.kicad_sch

Sensor

File: Sensor.kicad_sch

System

File: System.kicad_sch

eFuse

File: efuse.kicad_sch

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Sheet: /
File: VoxLink.kicad_sch

Title: Root

Size: A4	Date: 2025-11-17	**Rev: 1.0**
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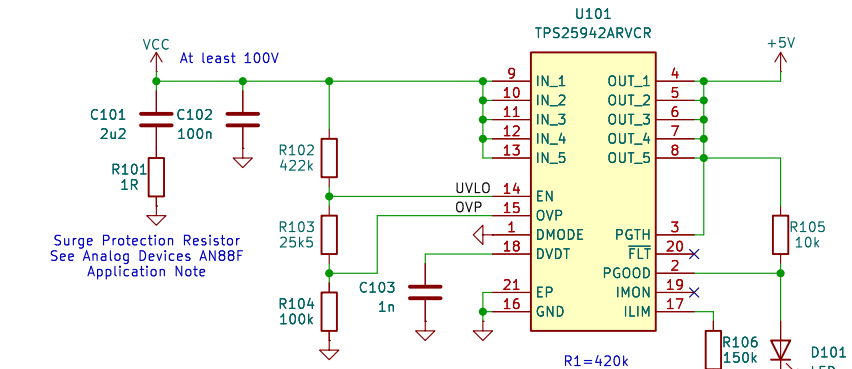
eFuse [1]

Power Protection



PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM} Current limit I_{LIM} for TPS25942[2] I_{FAULT} forTPS25944 [2] [3]	R_{ILIM} = 150 kΩ, (V_{IN} – V_{OUT}) = 1 V	0.53	0.58	0.63	A
	R_{ILIM} = 88.7 kΩ, (V_{IN} – V_{OUT}) = 1 V	0.9	0.99	1.07	
	R_{ILIM} = 42.2 kΩ, (V_{IN} – V_{OUT}) = 1 V	1.92	2.08	2.25	
	R_{ILIM} = 24.9 kΩ, (V_{IN} – V_{OUT}) = 1 V	3.25	3.53	3.81	
	R_{ILIM} = 20 kΩ, (V_{IN} – V_{OUT}) = 1 V	4.09	4.45	4.81	
	R_{ILIM} = 16.9 kΩ, (V_{IN} – V_{OUT}) = 1 V	4.78	5.2	5.62	
	R_{ILIM} = OPEN, open resistor current limit (single point failure test: UL60950)	0.35	0.45	0.55	
	R_{ILIM} = SHORT, shorted resistor current limit (single point failure test: UL60950)	0.55	0.67	0.8	
	DMODE = High; Non-ideal diode mode[1]		0.5 × I_{ILIM}		

ILIM sets the current imit of the eFuse.
Datasheet specifies 450mA if I_lim is left open.
The largest tested value of ILIM is 150kOhm (580mA)

I_mon is only used for external sensing

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Title: eFuse

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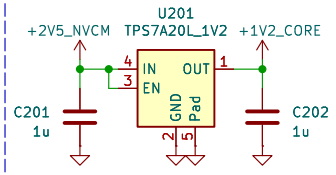
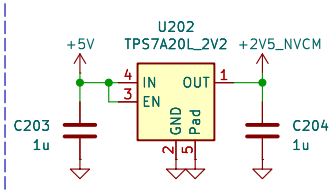
Power [2]

Core Supply Voltage



NVCM Supply



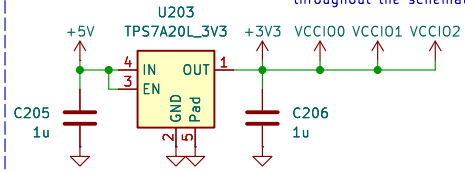
The NVCM regulator can be omitted and the VPP2V5 pin can be connected directly to 3V3 in order to save cost.

The pin can handle 3.6V.

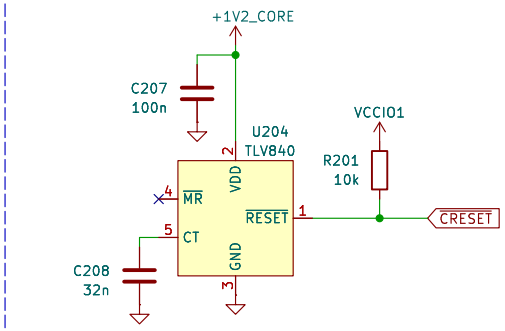
A diode can be used to drop the voltage before by roughly 0.7V

IO Supply

Multiple net names are used to indicate the I/O banks throughout the schematic



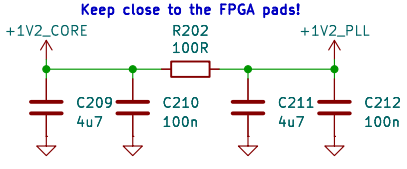
FPGA Power Delay

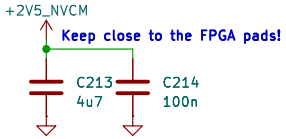


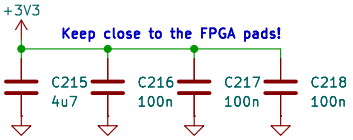
C [uF] = (T_delay − 80uS) / 618937
32nF = (20,000us − 80uS) / 618937

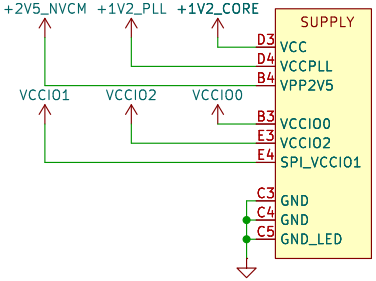
The FPGA wakes up after rougly 10ms, however, the memory takes 20ms to boot. We need to delay the FPGA startup, so that the flash memory is ready.

FPGA Power Input









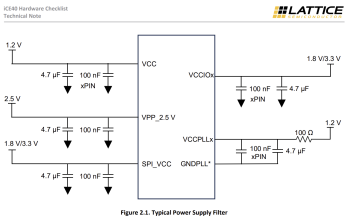


Figure 2.1. Typical Power Supply Filter

Filtering suggested by the manufacturer

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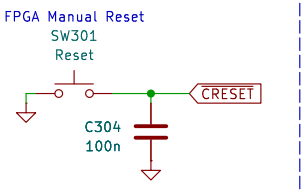
System [3]

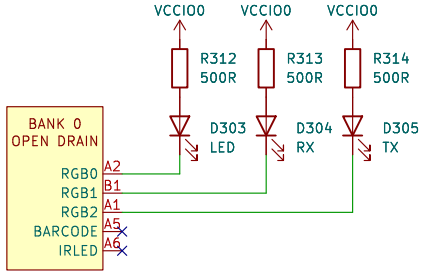
FPGA Manual Reset



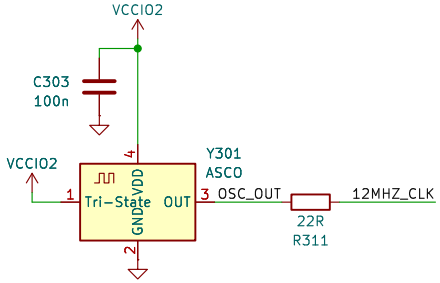
Open–Drain Outputs

Used for LED driving

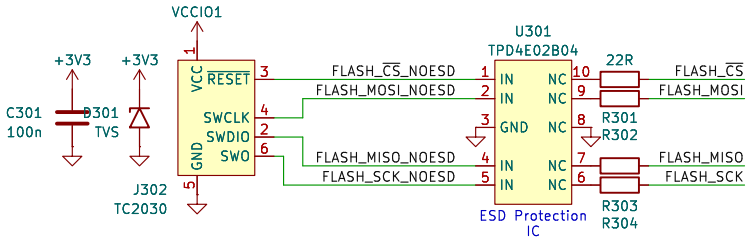
VCCIO0 = 3V3



External Oscillator



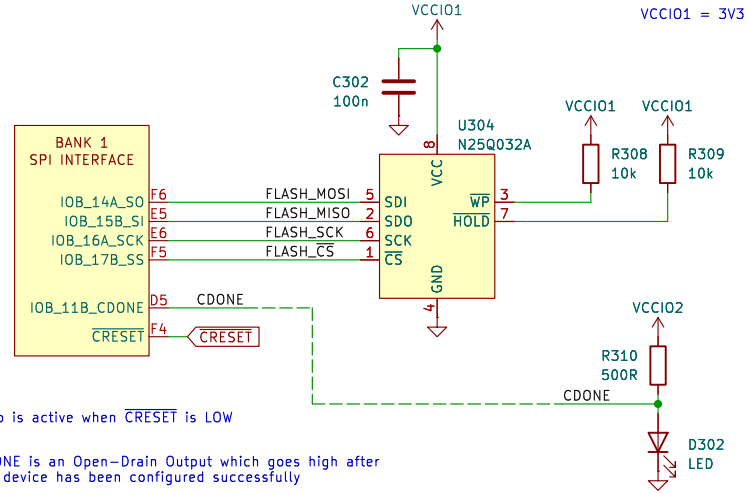
Tag Connect Programming Interface



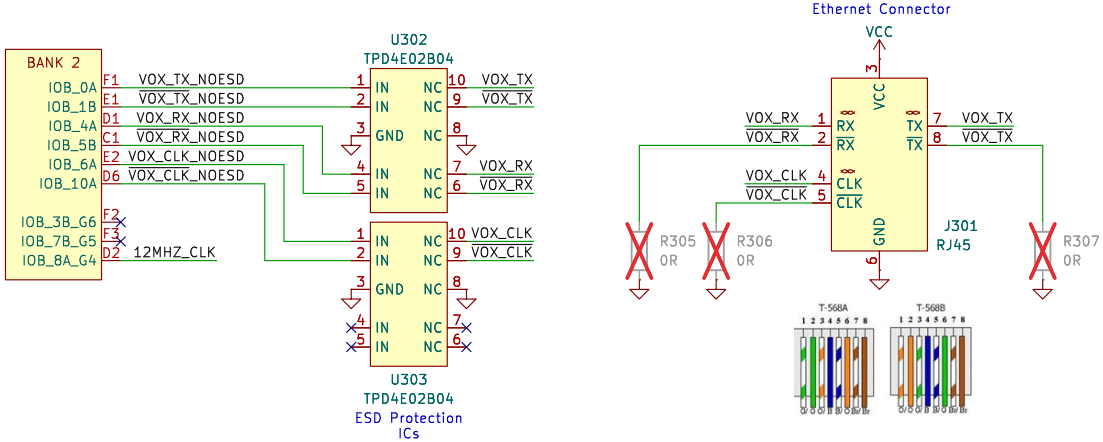
SPI Flash

Part choice may be subject to change in the next revision

VCCIO1 = 3V3



VoxLink Ethernet Connection



No Placement (NOP) – Used in case a differential driver would not work –> NEGATIVE can be tied to GND

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Sheet: /System/

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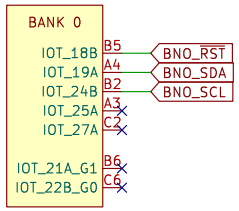
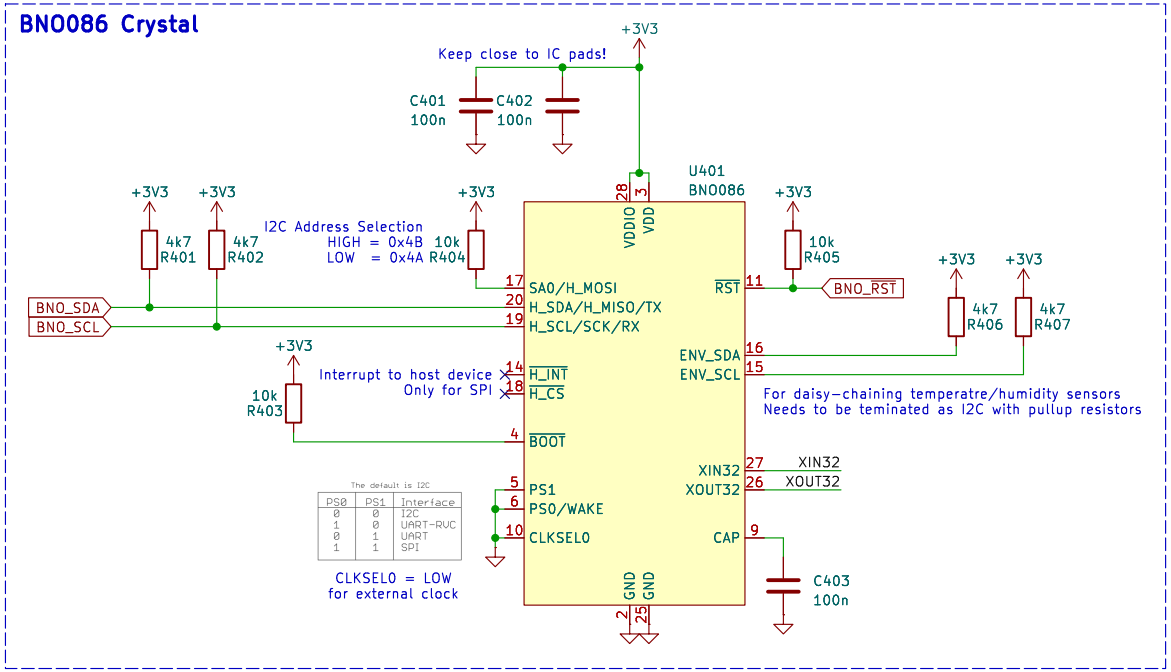
Sensor [4]

I2C Interface

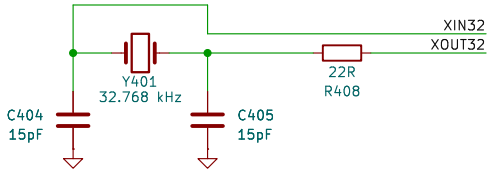


BNO086 Crystal



BNO086 Crystal

CEVA recommends using a crystal with tolerance 50ppm with 12.5pF capacitor loading.



(12.5pF Load Capacitance − 5pF Stray Capacitance) * 2 = 15pF Load Capacitors

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Sheet: /Sensor/ File: Sensor.kicad_sch		
Title: Sensor		
Size: A4	Date: 2025-11-18	**Rev: 1.0**
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