Root [0]

Technical Sheet Only!
Please refer to the subsequent sheets for schematic

Power

File: power.kicad_sch

Sensor

File: Sensor.kicad_sch

Connectivity

File: connectivity.kicad_sch

System

File: System.kicad_sch

eFuse

File: efuse.kicad_sch

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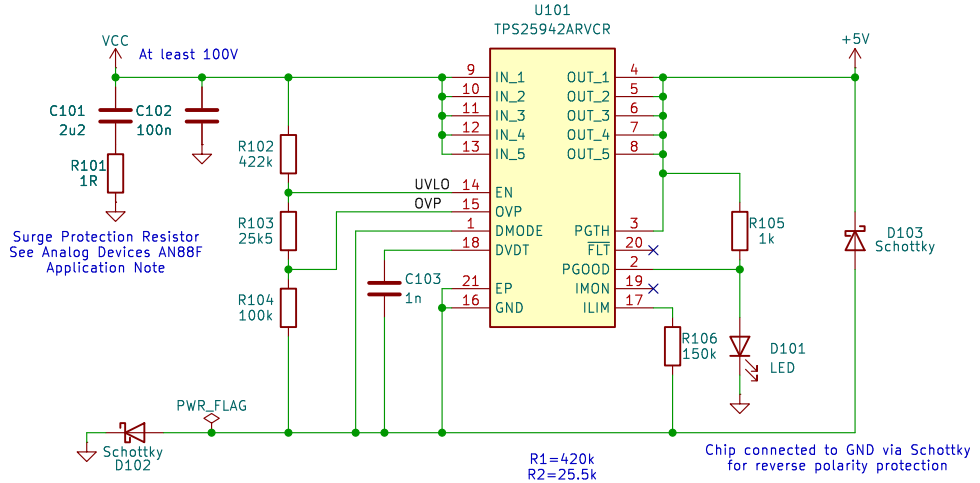
Sheet: / File: VoxSense.kicad_sch		
Title: VoxSense Sensor Board – Root		
Size: A4	Date: 2025-11-17	**Rev: 1.0**
KiCad E.D.A. 9.0.6		Id: 0/6

eFuse [1]

Power Protection



PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM} Current limit I_{LIM} for TPS25942[2] I_{FAULT} for TPS2594 [2][3]	R_{ILIM} = 150 kΩ, (V_{IN} – V_{OUT}) = 1 V	0.53	0.58	0.63	A
	R_{ILIM} = 88.7 kΩ, (V_{IN} – V_{OUT}) = 1 V	0.9	0.99	1.07	
	R_{ILIM} = 42.2 kΩ, (V_{IN} – V_{OUT}) = 1 V	1.92	2.08	2.25	
	R_{ILIM} = 24.9 kΩ, (V_{IN} – V_{OUT}) = 1 V	3.25	3.53	3.81	
	R_{ILIM} = 20 kΩ, (V_{IN} – V_{OUT}) = 1 V	4.09	4.45	4.81	
	R_{ILIM} = 16.9 kΩ, (V_{IN} – V_{OUT}) = 1 V	4.78	5.2	5.62	
	R_{ILIM} = OPEN, open resistor current limit (single point failure test: UL60950)	0.35	0.45	0.55	
	R_{ILIM} = SHORT, shorted resistor current limit (single point failure test: UL60950)	0.55	0.67	0.8	
	DMODE = High; Non-ideal diode mode[1]		0.5 × I_{ILIM}		

R1=420k
R2=25.5k
R3=100k
UVLO_Rising = 4.3V
UVLO_Falling = 4V
OVP_Rising = 5.4V
OVP_Falling = 5.01V

0.99*(R1+R2+R3)=5.4*R3
(R2+R3)/R3 = 5.4/4.3
R3=100k

ILIM sets the current imit of the eFuse.
Datasheet specifies 450mA if I_lim is left open.
The largest tested value of ILIM is 150kOhm (580mA)

I_mon is only used for external sensing

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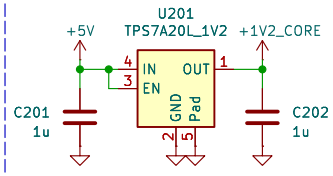
Sheet: /eFuse/
File: efuse.kicad_sch

Title: eFuse

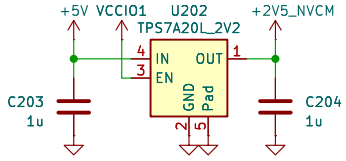
Size: A4	Date: 2025-12-04	**Rev: 1.0**
KiCad E.D.A. 9.0.6		Id: 1/6

Power [2]

Core Supply Voltage



NVCM Supply



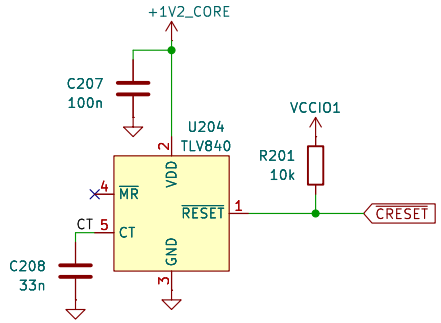
The NVCM regulator can be omitted and the VPP2V5 pin can be connected directly to 3V3 in order to save cost.

The pin can handle 3.6V.

A diode can be used to drop the voltage before by roughly 0.7V

FPGA Power Delay

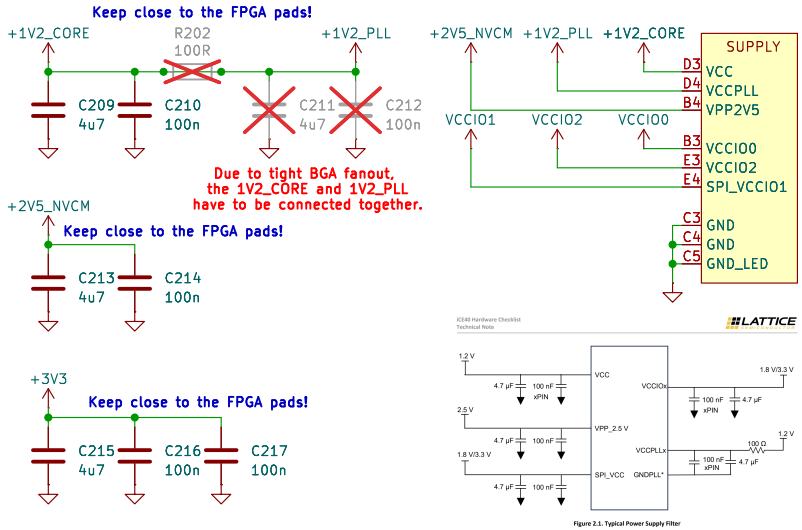
Note that $\overline{\text{CRESET}}$ is active LOW, meaning the FPGA is active when $\overline{\text{CRESET}}$ is HIGH. This requires a $\overline{\text{RESET}}$ variant of the TLV840 chip which active LOW, meaning it is the correct reset logic.



C [uF] = (T_delay [uS] − 80uS) / 618937
32nF = (20,000us − 80uS) / 618937

The FPGA wakes up after rougly 10us, however, the memory takes 150us to boot. We need to delay the FPGA startup, so that the flash memory is ready.

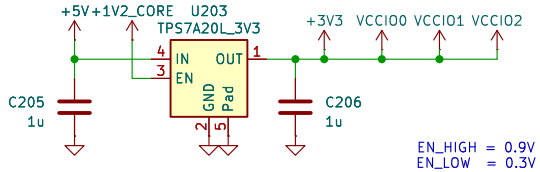
FPGA Power Input



Filtering suggested by the manufacturer

IO Supply

Multiple net names are used to indicate the I/O banks throughout the schematic



EN_HIGH = 0.9V
EN_LOW = 0.3V
EN_MAX = 6.5V

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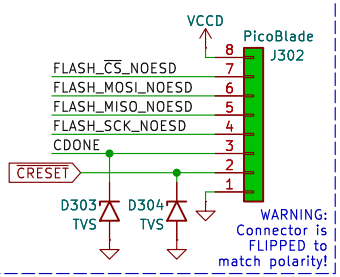
Sheet: /Power/
File: power.kicad_sch

Title: Power

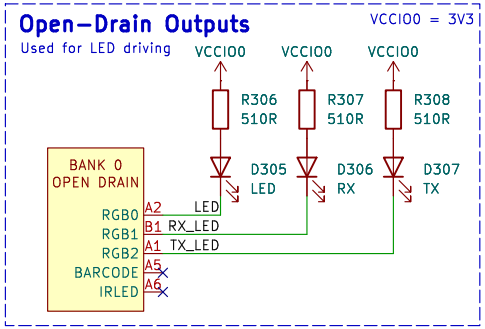
Size: A4	Date: 2025-11-09	**Rev: 1.0**
KiCad E.D.A. 9.0.6		Id: 2/6

System [3]

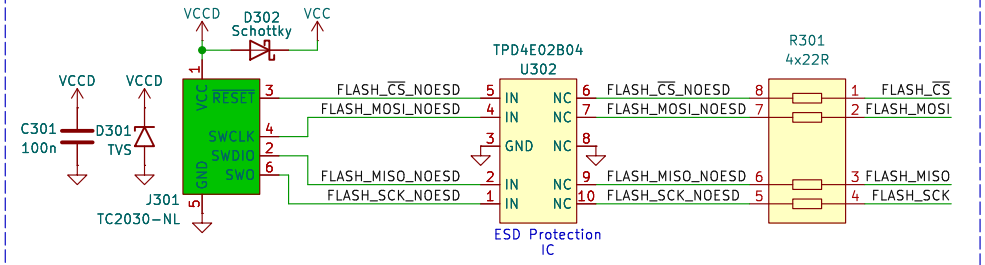
PicoBlade Programming Connector



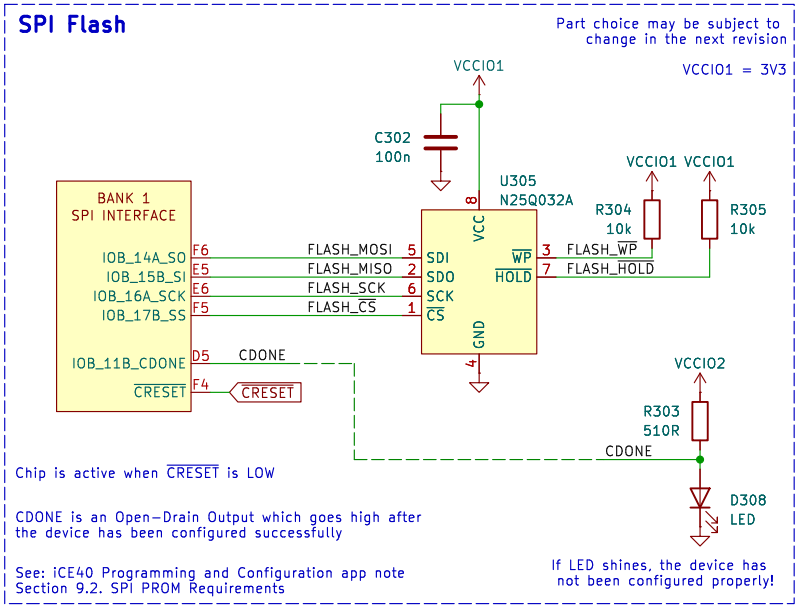
Open–Drain Outputs



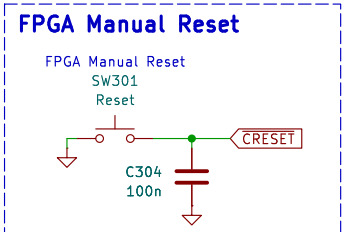
Tag Connect Programming Interface



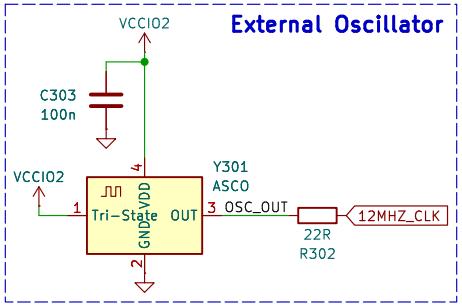
SPI Flash



FPGA Manual Reset



External Oscillator



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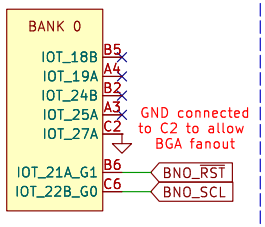
Sheet: /System/
File: System.kicad_sch

Title: System

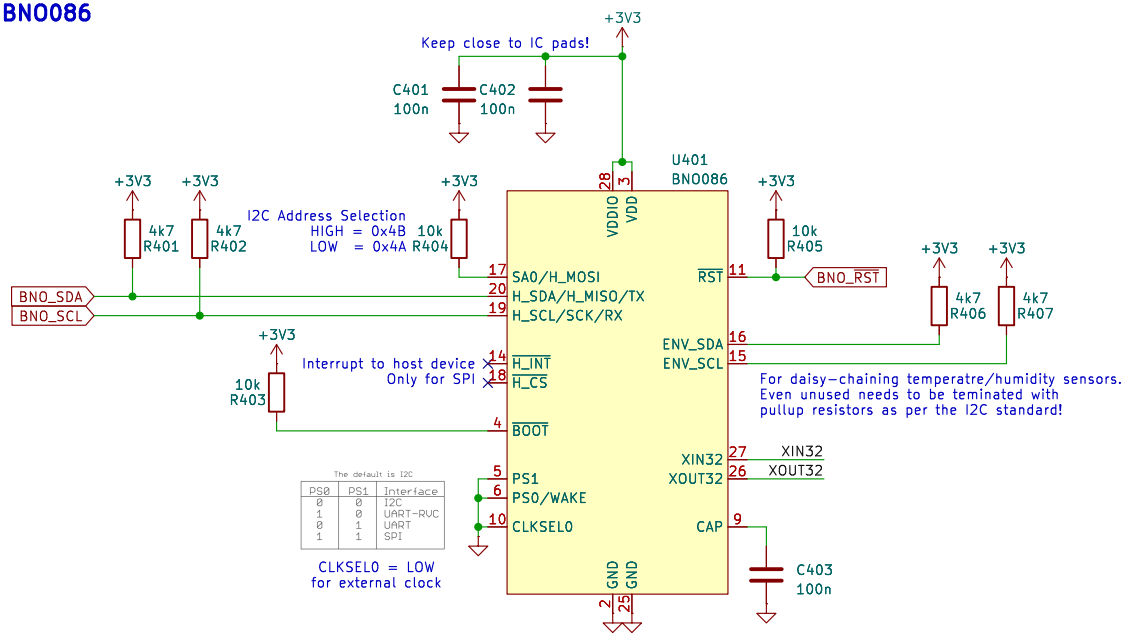
Size: A4	Date: 2025–11–17	**Rev: 1.0**
KiCad E.D.A. 9.0.6		Id: 3/6

Sensor [4]

I2C Interface

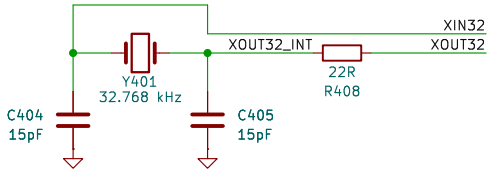


BNO086



BNO086 Crystal

CEVA recommends using a crystal with tolerance 50ppm with 12.5pF capacitor loading.



(12.5pF Load Capacitance − 5pF Stray Capacitance) * 2 = 15pF Load Capacitors

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Sheet: /Sensor/
File: Sensor.kicad_sch

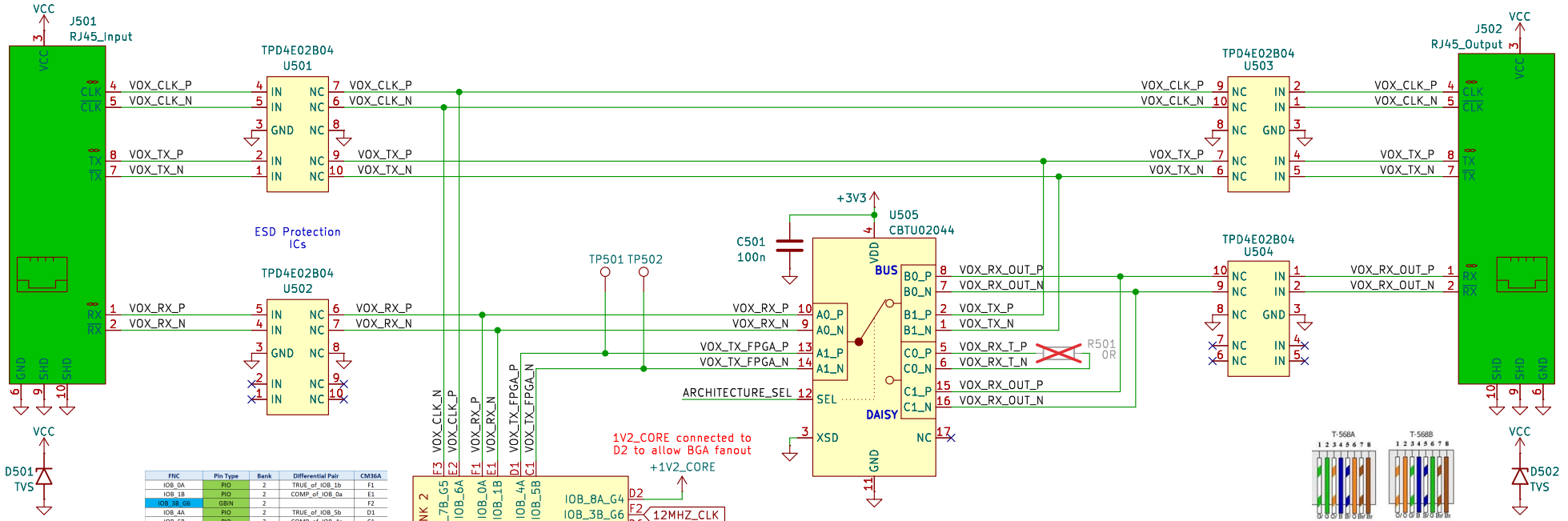
Title: Sensor

Size: A4	Date: 2025-11-18	**Rev: 1.0**
KiCad E.D.A. 9.0.6		Id: 4/6

Connectivity [5]

VoxLink Ethernet Connection + Bus / Daisy Chain Switch

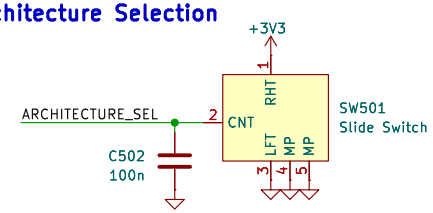
No Placement (NOP) – Used for the possibility of terminating the differential pairs to prevent reflections



FNC	Pin Type	Bank	Differential Pair	CM36A
IOB_0A	PIO	2	TRUE_of_IOB_1b	F1
IOB_1B	PIO	2	COMP_of_IOB_0a	E1
IOB_3B_G6	GBIN	2		F2
IOB_4A	PIO	2	TRUE_of_IOB_5b	D1
IOB_5B	PIO	2	COMP_of_IOB_4a	C1
IOB_6A	PIO	2	TRUE_of_IOB_7b_G5	E2
IOB_7B_G5	GBIN	2	COMP_of_IOB_6a	F3
IOB_8A_G4	GBIN	2		D2
IOB_10A	PIO	2	TRUE_of_IOB_11b	D6

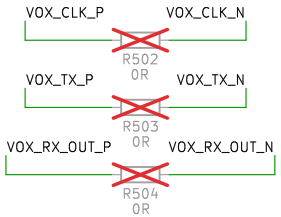
Table of differential comparator pin pairs

Architecture Selection



SEL = LOW –> A and B are conencted
SEL = HIGH –> A and C are conencted

Termination Resistors



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Sheet: /Connectivity/		
File: connectivity.kicad_sch		
Title: Connectivity		
Size: A4	Date: 2025-12-21	**Rev: 1.0**
KiCad E.D.A. 9.0.6		Id: 5/6