ECE 298A
Duties and Contributions

Design/Documentation:

- Function Design – Michelle and Noah
- Timing Diagrams – Michelle
- Block Diagram – Michelle
- I/O Table – Noah

Implementation:

- LFSR – Michelle
- WAIT State – Michelle
- 32Bit Memory – Michelle
- IDLE State – Michelle
- State Encoder & Decoder – Noah
- CHECK State – Noah
- DISPLAY State – Noah
- Integration – Michelle

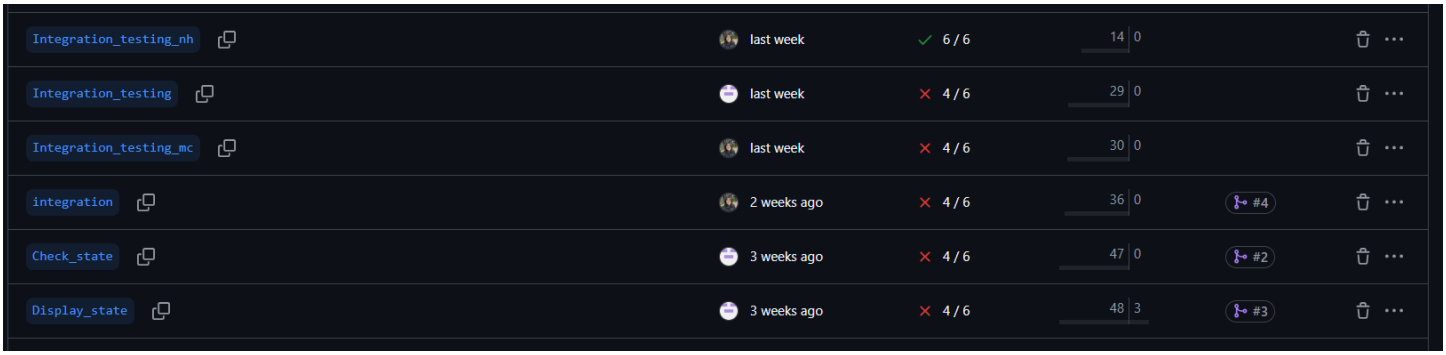
Testing:

- Each student conducted unit testing on their respective modules.
- Integration & Functional Testing – Michelle and Noah
- Static Timing Analysis – Michelle

Trello:
https://trello.com/b/HQXW0MiP/ece298a-simon-says

Git Branches:
(from previous IHP template)

(from current SKY130 template)



Functional Testing

The ‘test_simon.py’ file read user input values from vectors.csv. The test simulates the loading (or IDLE) portion of the game where the random colour sequence is generated and stored. The completion of each state is tested. The user inputs are used during the WAIT state and compares with the sequence stored in memory. The expected win / loss of the round is also tested.

```
FST info: dumpfile sim_build/tt_um_simonsays.fst opened for output.
   750.00ns INFO     cocotb.tt_um_simonsays
                                           Vector 1: mem=0x1 player=0xa5298a22 expect=PASS
  2550.00ns INFO     cocotb                 [ASSERT] rising edge complete_idle detected
 34550.00ns INFO     cocotb                 [ASSERT] rising edge complete_wait detected
 34650.00ns INFO     cocotb                 [ASSERT] rising edge complete_check detected
 35450.00ns INFO     cocotb.tt_um_simonsays
                                           Vector 2: mem=0x2 player=0x320c03c0 expect=PASS
 37250.00ns INFO     cocotb                 [ASSERT] rising edge complete_idle detected
 69250.00ns INFO     cocotb                 [ASSERT] rising edge complete_wait detected
 69350.00ns INFO     cocotb                 [ASSERT] rising edge complete_check detected
 70150.00ns INFO     cocotb.tt_um_simonsays
                                           Vector 3: mem=0x3 player=0x0531cc73 expect=PASS
 71950.00ns INFO     cocotb                 [ASSERT] rising edge complete_idle detected
103950.00ns INFO     cocotb                 [ASSERT] rising edge complete_wait detected
104050.00ns INFO     cocotb                 [ASSERT] rising edge complete_check detected
104850.00ns INFO     cocotb.tt_um_simonsays
                                           Vector 4: mem=0x4 player=0x01234567 expect=FAIL
106650.00ns INFO     cocotb                 [ASSERT] rising edge complete_idle detected
138650.00ns INFO     cocotb                 [ASSERT] rising edge complete_wait detected
138750.00ns INFO     cocotb                 [ASSERT] rising edge complete_check detected
138750.00ns INFO     cocotb.tt_um_simonsays ✅ All vectors passed
138750.00ns INFO     cocotb.regression      simon_system_test passed
138750.00ns INFO     cocotb.regression      ********************************************************************************************
                                           ** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                           ********************************************************************************************
                                           ** test_simon.simon_system_test   PASS      138750.00           0.12    1149890.70  **
                                           ********************************************************************************************
                                           ** TESTS=1 PASS=1 FAIL=0 SKIP=0             138750.00           0.20     699650.73  **
                                           ********************************************************************************************
```

Unit Testing

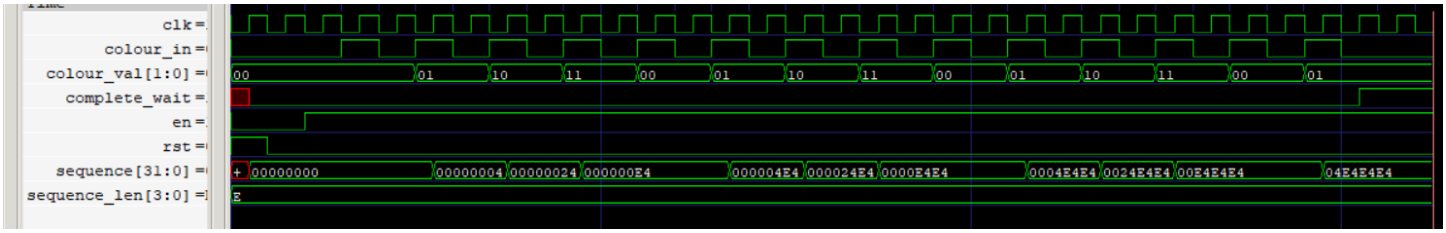
The functionality of each module was tested using Verilog testbenches located in a ‘Unit Tests’ folder in the test directory.

(Display_state module coco_tb testing)

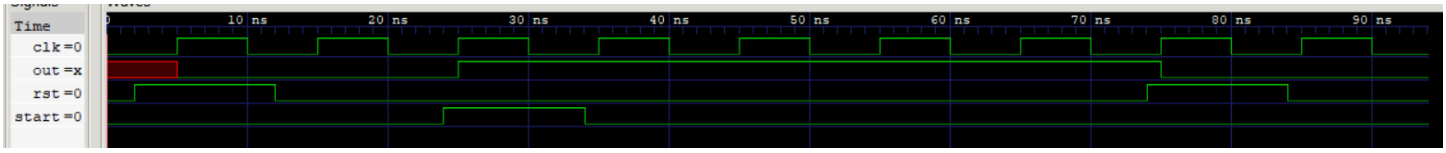
```
"make" -f Makefile results.xml
make[1]: Entering directory '/mnt/c/Users/noahh/VSCODE/School/ECE-298A/display_state_cocotb'
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s display_state         -g2012 -f sim_build/cmds.f  display_state.v
rm -f results.xml
MODULE=test_display_state    TESTCASE= TOPLEVEL=display_state         TOPLEVEL_LANG=verilog \
        /usr/bin/vvp -M /usr/local/lib/python3.10/dist-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:79   in set_program_name_in_venv        Did not detect Python virtual environment. U
sing system-wide Python interpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.9.2 from /usr/local/lib/python3.10/dist-packages/cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1754495292
     0.00ns INFO     cocotb.regression                  Found test test_display_state.display_state_basic
     0.00ns INFO     cocotb.regression                  running display_state_basic (1/1)
                                                          Run all vectors from vectors.csv.
150000.00ns WARNING  cocotb                             Bad data on line 1: ['pattern_hex', 'round_ctr', 'idle_cycles'] (invalid literal for int() with base 16:
'pattern_hex')
150000.00ns INFO     cocotb                             Vector 2: pattern=0x00000000 round=0 idle=2
750000.00ns INFO     cocotb                             Vector 3: pattern=0x00000001 round=0 idle=2
1350000.00ns INFO    cocotb                              Vector 4: pattern=0x00000002 round=0 idle=2
1950000.00ns INFO    cocotb                              Vector 5: pattern=0x00000003 round=0 idle=2
2550000.00ns INFO    cocotb                              Vector 6: pattern=0x00000004 round=1 idle=2
3250000.00ns INFO    cocotb                              Vector 7: pattern=0x00000001 round=1 idle=2
3950000.00ns INFO    cocotb                              Vector 8: pattern=0x0000000E round=1 idle=2
4650000.00ns INFO    cocotb                              Vector 9: pattern=0x0000000B round=1 idle=2
5350000.00ns INFO    cocotb                              Vector 10: pattern=0x000000E4 round=3 idle=2
6250000.00ns INFO    cocotb                              Vector 11: pattern=0x0000001B round=3 idle=2
7150000.00ns INFO    cocotb                              Vector 12: pattern=0x0000E4E4 round=7 idle=3
8550000.00ns INFO    cocotb                              Vector 13: pattern=0x0000CCCC round=7 idle=3
9950000.00ns INFO    cocotb                              Vector 14: pattern=0xE4E4E4E4 round=15 idle=4
12250000.00ns INFO    cocotb                              Vector 15: pattern=0xFFFFFFFF round=15 idle=4
14550000.00ns INFO    cocotb                              All CSV vectors passed.
14550000.00ns INFO    cocotb.regression                   display_state_basic passed
14550000.00ns INFO    cocotb.regression                   ****************************************************************************************************
                                                          ** TEST                                 STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                          ****************************************************************************************************
                                                          ** test_display_state.display_state_basic   PASS    14550000.00           0.02   690742764.05  **
                                                          ****************************************************************************************************
                                                          ** TESTS=1 PASS=1 FAIL=0 SKIP=0                    14550000.00           0.10   144319924.33  **
                                                          ****************************************************************************************************

make[1]: Leaving directory '/mnt/c/Users/noahh/VSCODE/School/ECE-298A/display_state_cocotb'
```

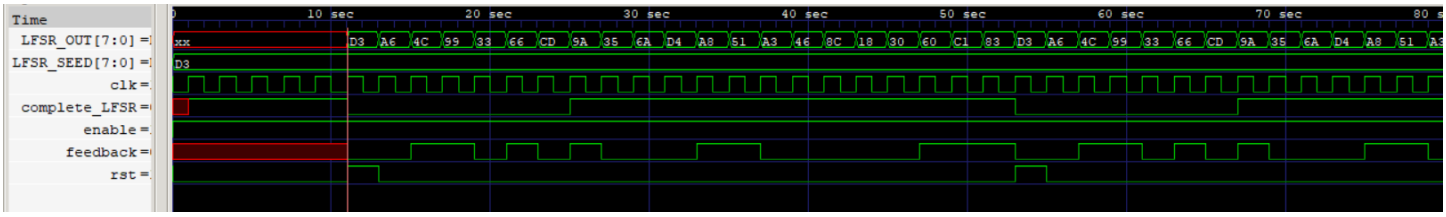
(Wait_state module Verilog testbench)



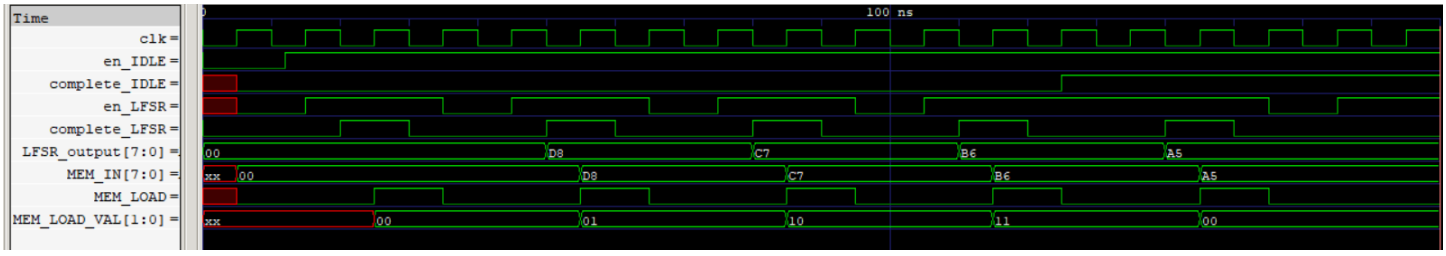
(start_reg module Verilog testbench)



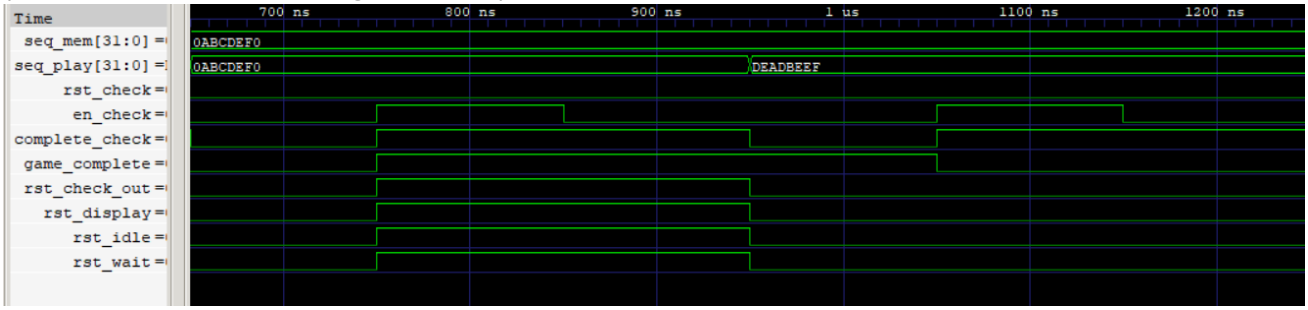
(LFSR module Verilog testbench)



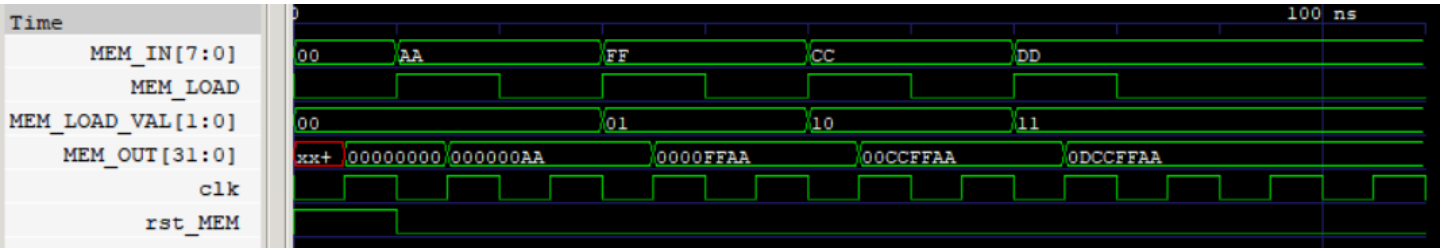
(Idle_state module Verilog testbench)



(Check_state module Verilog testbench)



(MEM module Verilog testbench)



Static Timing Analysis

```
Marker A
Clock clk
   0.52 source latency _0989_/CLK ^
  -0.54 target latency _0971_/CLK ^
  -0.10 clock uncertainty
   0.00 CRPR
--------------
  -0.13 hold skew

                                                        Not
Check type                          Total    Annotated   Annotated
-------------------------------------------------------------------
cell hold arcs                        128          0         128
-------------------------------------------------------------------
                                      128          0         128
Startpoint: _0985_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: uo_out[4] (output port clocked by clk)
Path Group: clk
Path Type: min
Corner: ff

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk (rise edge)
   0.29    0.29   clock network delay (propagated)
   0.00    0.29 ^ _0985_/CLK (sky130_fd_sc_hd__dfxtp_1)
   0.23    0.52 ^ _0985_/Q (sky130_fd_sc_hd__dfxtp_1)
   0.07    0.59 ^ _1080_/X (sky130_fd_sc_hd__buf_2)
   0.00    0.59 ^ uo_out[4] (out)
           0.59   data arrival time

   0.00    0.00   clock clk (rise edge)
   0.00    0.00   clock network delay (propagated)
   0.10    0.10   clock uncertainty
   0.00    0.10   clock reconvergence pessimism
   2.50    2.60   output external delay
           2.60   data required time
---------------------------------------------------------
           2.60   data required time
          -0.59   data arrival time
---------------------------------------------------------
          -2.01   slack (VIOLATED)
```

```
Startpoint: _0955_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _0970_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Corner: ss

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk (rise edge)
   0.53    0.53   clock network delay (propagated)
   0.00    0.53 ^ _0955_/CLK (sky130_fd_sc_hd__dfxtp_1)
   0.62    1.15 ^ _0955_/Q (sky130_fd_sc_hd__dfxtp_1)
   0.89    2.05 v _0587_/X (sky130_fd_sc_hd__or4bb_1)
   0.68    2.72 v _0595_/X (sky130_fd_sc_hd__or3_1)
   0.98    3.71 ^ _0664_/Y (sky130_fd_sc_hd__nor4_1)
   0.45    4.15 v _0668_/Y (sky130_fd_sc_hd__nand3_1)
   0.58    4.73 v _0674_/X (sky130_fd_sc_hd__o311a_1)
   0.00    4.73 v _0970_/D (sky130_fd_sc_hd__dfxtp_1)
           4.73   data arrival time

 100.00  100.00   clock clk (rise edge)
   0.52  100.52   clock network delay (propagated)
  -0.10  100.42   clock uncertainty
   0.00  100.42   clock reconvergence pessimism
         100.42 ^ _0970_/CLK (sky130_fd_sc_hd__dfxtp_1)
  -0.21  100.20   library setup time
         100.20   data required time
---------------------------------------------------------
         100.20   data required time
          -4.73   data arrival time
---------------------------------------------------------
          95.47   slack (MET)
```

```
Startpoint: _0955_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _0970_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Corner: tt

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk (rise edge)
   0.36    0.36   clock network delay (propagated)
   0.00    0.36 ^ _0955_/CLK (sky130_fd_sc_hd__dfxtp_1)
   0.38    0.73 ^ _0955_/Q (sky130_fd_sc_hd__dfxtp_1)
   0.48    1.22 v _0587_/X (sky130_fd_sc_hd__or4bb_1)
   0.37    1.59 v _0595_/X (sky130_fd_sc_hd__or3_1)
   0.54    2.14 ^ _0664_/Y (sky130_fd_sc_hd__nor4_1)
   0.21    2.35 v _0668_/Y (sky130_fd_sc_hd__nand3_1)
   0.32    2.66 v _0674_/X (sky130_fd_sc_hd__o311a_1)
   0.00    2.66 v _0970_/D (sky130_fd_sc_hd__dfxtp_1)
           2.66   data arrival time

 100.00  100.00   clock clk (rise edge)
   0.35  100.35   clock network delay (propagated)
  -0.10  100.25   clock uncertainty
   0.00  100.25   clock reconvergence pessimism
         100.25 ^ _0970_/CLK (sky130_fd_sc_hd__dfxtp_1)
  -0.11  100.14   library setup time
         100.14   data required time
---------------------------------------------------------
         100.14   data required time
          -2.66   data arrival time
---------------------------------------------------------
          97.48   slack (MET)
```

STA Pre Layout (sta_prepnr)

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of which reg to reg	Setup Worst Slack	Reg to Reg Paths	Setup TNS	Setup Vio Count	of which reg to reg	Max Cap Violatio…	Max Slew Violati…
Overall	0.0425	0.0425	0.0000	0	0	11.4656	N/A	0.0000	0	0	1	64
nom_tt_025C_1v80	0.1979	0.1979	0.0000	0	0	13.5272	N/A	0.0000	0	0	0	62
nom_ss_100C_1v60	0.6215	0.6215	0.0000	0	0	11.4656	N/A	0.0000	0	0	1	64
nom_ff_n40C_1v95	0.0425	0.0425	0.0000	0	0	14.3679	N/A	0.0000	0	0	0	62

STA Post Layout (sta_postpnr)

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of which reg to reg	Setup Worst Slack	Reg to Reg Paths	Setup TNS	Setup Vio Count	of which reg to reg	Max Cap Violatio…	Max Slew Violati…
Overall	0.1043	0.1043	0.0000	0	0	12.2697	N/A	0.0000	0	0	0	19
nom_tt_025C_1v80	0.3040	0.3040	0.0000	0	0	13.9526	N/A	0.0000	0	0	0	0
nom_ss_100C_1v60	0.8346	0.8346	0.0000	0	0	12.3530	N/A	0.0000	0	0	0	19
nom_ff_n40C_1v95	0.1056	0.1056	0.0000	0	0	14.6602	N/A	0.0000	0	0	0	0
min_tt_025C_1v80	0.3004	0.3004	0.0000	0	0	14.0032	N/A	0.0000	0	0	0	0
min_ss_100C_1v60	0.8284	0.8284	0.0000	0	0	12.4382	N/A	0.0000	0	0	0	5
min_ff_n40C_1v95	0.1043	0.1043	0.0000	0	0	14.6881	N/A	0.0000	0	0	0	0
max_tt_025C_1v80	0.3081	0.3081	0.0000	0	0	13.9070	N/A	0.0000	0	0	0	0
max_ss_100C_1v60	0.8416	0.8416	0.0000	0	0	12.2697	N/A	0.0000	0	0	0	19
max_ff_n40C_1v95	0.1072	0.1072	0.0000	0	0	14.6350	N/A	0.0000	0	0	0	0